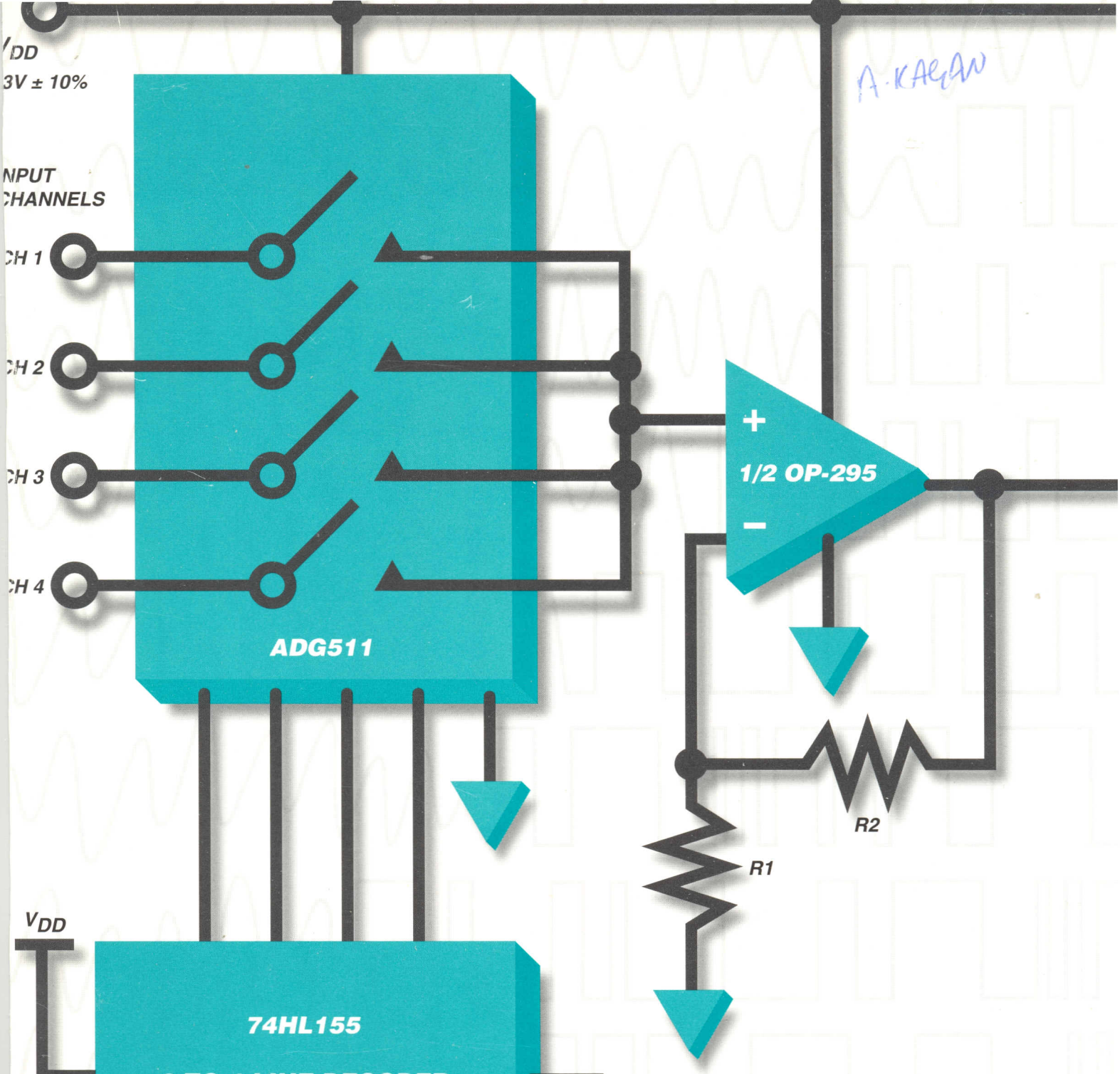


SYSTEM APPLICATIONS GUIDE

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Figure 1.28: Third bullet point, *Interference* is the correct spelling.

Figure 1.30: Title to bottom diagram, *Illustrates* is the correct spelling.

Figure 1.31: Second point under third bullet point, delete *and Wide as Practical.*

Figure 1.33: Title, *Eliminate* is the correct spelling. First column, third row, *Bifilar* should appear with no parentheses underneath *L-C.*

Figure 1.36: Remove the short across the 11.8kΩ resistor. A1 and A2 should be labeled *1/2 AD708.*

Figure 1.37: Add a 0.47µF capacitor between pin 6 and pin 8 of the AMP-04. The 0.1µF capacitor between pin 2 and pin 3 of the AMP-04 should be labeled C1. A1 and A2 should be labeled *1/2 OP-295.*

Figure 1.38: Add a note that R5 must be a 0.1%, low TCR resistor.

Page 1-32: The first sentence in the last paragraph should read: *Strain or flexure can be remotely sensed with the circuit in Figure 1.39.*

Figure 1.56: Add a capacitor C4 in parallel with R4. First bullet point should read: *C1, C2: Low-Inductance Capacitors.* Second bullet point should read: *Use Metal-Film Resistors for Low Noise and Parasitic Reactance.*

Figure 1.64: Third entry under second bullet point should read: *Low-Inductance capacitors.*

Figure 1.79: Fourth bullet point should read: *When in Doubt, Protect with External Diodes.*

Figure 1.83: Third bullet point should read: *Remember JFET Leakage Doubles for every 10°C Rise.*

Figure 1.85: *Disastrous* is the correct spelling in the second bullet point.

Figure 1.88: Label should read: *Horizontal Scale: 10µs/div.*

Figure 3.15: –IN should be grounded.

Figure 5.9: Title should read: *Low Reference Noise is Critical for High Accuracy.*

Figure 5.13: Title should read: *1Hz Low Pass Filter Reduces Noise to 5µV p-p.*

Figure 6.13: Fifth bullet point should read: *Further Digital Filtering Will Realize Figure 6.12 Values.*

Figure 6.19: Add a connection between the AV_{DD} pin of the AD7710 and the upper internal diode.

Page 6-19: The first two sentences should read: *The AD780 2.5V reference has a noise of 670nV rms in the range 0.1 to 10Hz. This gives 0.35µV rms noise in the 2.62Hz bandwidth...*

Figure 6.22: The first bullet point should read: *AD780 has 215 nV/ √Hz noise at 1Hz.* The equation in the second bullet point should read:

RMS Noise = (215nV/ √Hz)×√2.62Hz = 0.35µV rms.

Figure 6.34: The AD1849 Throughput should be *5,500 - 48,000* samples/sec.

Figure 7.5: The fourth bullet point should read: *Accuracy: 1°C for TCs and 0.2% for RTDs.* The seventh bullet point should read: *Output in Engineering Units (°C, V).*

Page 7-6: The last sentence in the first paragraph should read: *The pinout configuration for the AD1B60 is shown in Figure 7.6.*

Figure 7.7: The first bullet point should read: *Zero Compensation/Span Compensation.* The fourth bullet point should read: *Data Scaling (°C, V).* Delete the sixth bullet point.

Page 7-7: The second sentence should read: *The output data is represented directly in engineering units (for example, °C or V) using....*

Figure 7.9: Headings for the last column should read: *Accuracy/Resolution (Typ).*

Figure 7.11: Note should read: *R1 Recommended for RTD Applications Only.* 15nA Open TC current source should be 10nA.

Figure 7.14: Sixth bullet point should read: *16-bit Integer and 32-bit Floating Point Data Formats.*

Page 7-13: Last sentence of second paragraph should read: *If the state of the ACM pin is a logic "0," address and CRC values are not used.*

Page 7-14: Last sentence on page should read: *Whenever CS changes state, CLK must be at logic "1" to avoid metastability problems.*

Figure 7.20: Bottom waveform: *Signal Conversion* time label should be replaced with *Signal Conversion (Computation).*

Figure 7.21: Label for last column should read: *Conversions/Sec, K Type + Thermistor.*

Figure 7.25: Remove arrow pointing to the terminal which connects to pin 8 of the AC1226.

Figure 7.32: Add connection between F+ terminal and pin 38 (CH0) of the AD1B60.

Figure 7.33: Second bullet point should read: *R1 is recommended to protect against self-heating.*

Figure 7.36: Add *REFIN* to the input pin labels.

Figure 7.37: The title should read: *Protecting the 1B60 Analog Inputs From Overvoltage Conditions*. Under the first bullet point, replace *J202* with *J201.*

Figure 7.38: Change second bullet point to read: *C1, C2: 0.1µF Ceramic.* Change fourth bullet point to read: *C5, C6: 100µF Low ESR Electrolytic.* Remove polarity marks from C1 and C2 and add them to C5 and C6.

Figure 7.41: Change RS232 interface chip part number from *AD232* to *ADM232L.* Change capacitor between pin 16 and pin 2 of ADM232L to 1µF. Change capacitor between pin 6 of ADM232L and ground to 1µF.

Figure 7.49: First bullet point should read: *Single Polynomial (Used in AD1B60).*

Page 7-48: The second sentence in the second paragraph should read: *If single-precision IEEE mathematics is used, the polynomial is for practical purposes limited to 9th order or less.*

Page 9-11: In the third sentence in the second paragraph, change *10MHz* to *5MHz.*

Figure 9.13: Change the label on the third order IMD intercept to read: *+36dBm @ 5MHz.*

Figure 10.23: Second bullet point should read: *Equalization of Source Resistances Generally Reduces Effects of Input Bias Currents.* In the last bullet point, remove the word *Levels.*

Figure 10.23: Fifth bullet point should read: *Difficult to Use as Integrators.* In the last bullet point, remove the word *Levels.*

Figure 11.4: Remove asterisk and corresponding note regarding R_F.

Figure 11.27: Change R_{B1} and R_{B2} to 10k.

Figure 11.40: Add bullet point: *Assume 22 Gauge Teflon Insulated Wire, $e_r = 2$, $d = 0.024"$, $h = 0.1"$.* Remove *±40%* from last bullet point.

Figure 15.10: Replace with the following corrected figure.

SIMPLIFIED DIGITAL RECEIVER USING BASEBAND SAMPLING

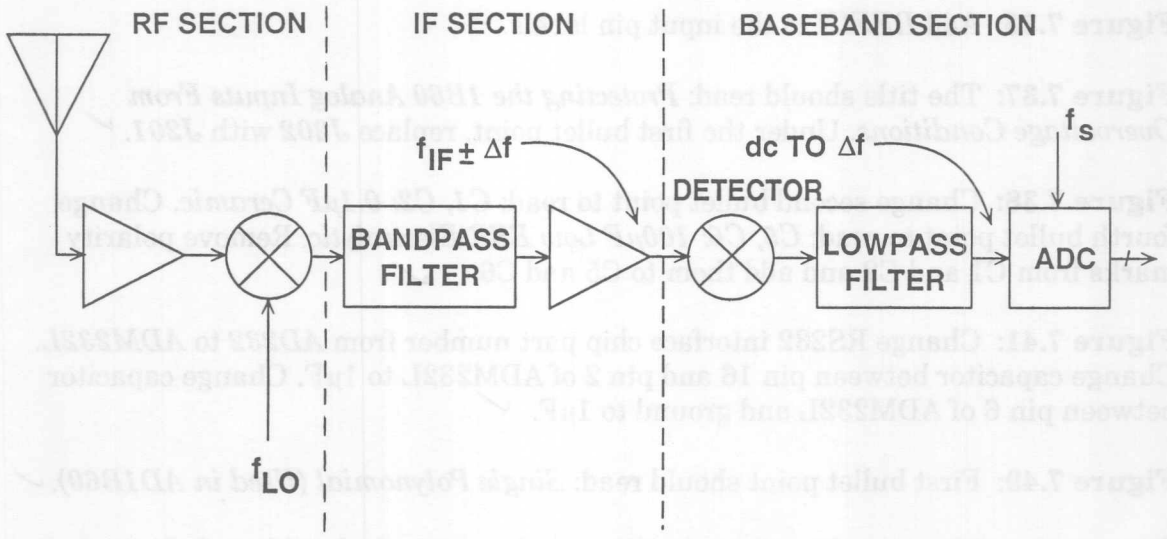


Figure 15.11: Replace with the following corrected figure.

SIMPLIFIED DIGITAL RECEIVER USING IF SAMPLING

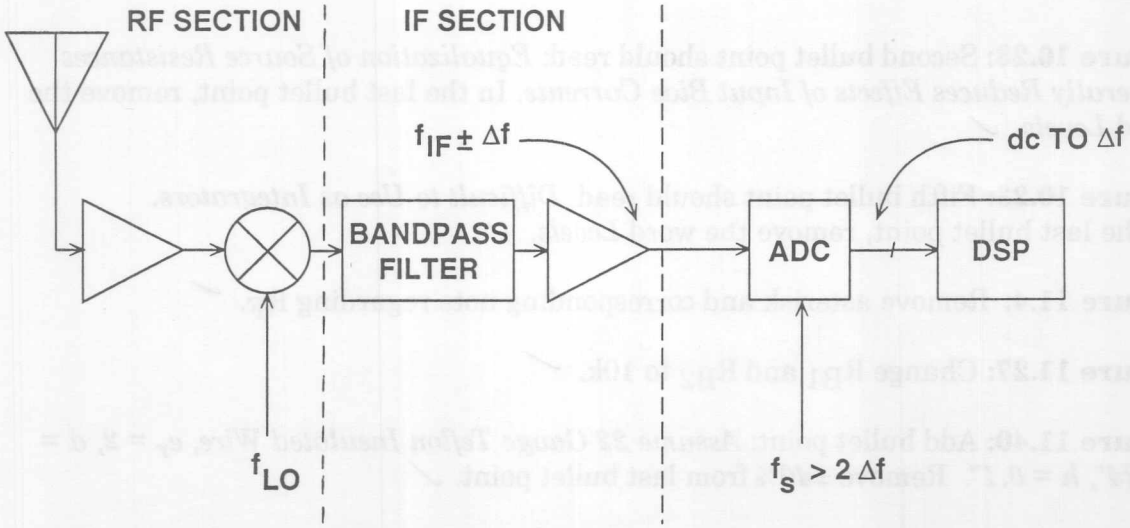


Figure 15.28: Title should read: *Replacing Integrators with Bandpass Filters Gives a Bandpass Sigma-Delta ADC.* In the bottom diagram, *Bandpass Modulator* should be replaced with *Bandpass Filter,* and *Digital Lowpass Filter and Decimator* should be replaced with *Digital Bandpass Filter and Decimator.*

Figure 16.1: The ground connection symbol for the *Error Waveform* signal BNC should not be touching the *Latch.*

Figure 18.28: In the lower portion of the diagram, the *16-bit Sigma-Delta ADC* should be changed to a *16-bit Sigma Delta DAC.*

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PUBLISHED BY PRENTICE HALL

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- **Digital Signal Processing Applications Using the ADSP-2100 Family**
- **Digital Signal Processing in VLSI**
- **DSP Laboratory Experiments Using the ADSP-2101**
- **ADSP-2100 Family User's Manual**

PUBLISHED BY ANALOG DEVICES

- **System Applications Guide**
- **Amplifier Applications Guide**
- **Mixed Signal Design Seminar Notes**
- **High-Speed Design Seminar Notes**
- **Nonlinear Circuits Handbook**
- **Transducer Interfacing Handbook**
- **Synchro & Resolver Conversion**
- **THE BEST OF *Analog Dialogue*, 1967-1991**

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Walt Kester
1993

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SECTION 1

PRECISION SENSOR SIGNAL CONDITIONING AND TRANSMISSION

James Wong, Joe Buxton, Adolfo Garcia, James Bryant

PRECISION SIGNALS AND SYSTEM ERROR SOURCES

Managing the total error budget in a complex high resolution precision system is extremely difficult. Every component in the system must be examined as a potential source of error.

Figure 1.1 shows accuracy (resolution) expressed as a percentage, ppm, and voltage (assuming a 10V fullscale signal range).

LEAST SIGNIFICANT BIT WEIGHTS FOR VARIOUS RESOLUTIONS

RESOLUTION	% FULLSCALE	PPM FULLSCALE	LSB WEIGHT (10V FS)
12-bits	0.0244%	244 ppm	2.44mV
16-bits	0.0015%	15 ppm	152μV
18-bits	0.00038%	3.8 ppm	38μV
20-bits	0.000095%	0.95 ppm	9.5μV
22-bits	0.000024%	0.238 ppm	2.38μV

Figure 1.1

Consider the industry-standard 741 or LM348 op amps which have an input offset voltage specification of 6mV. In a 12-bit system, this corresponds to over 2 LSBs absolute error (assuming no system calibration).

The precision OP-07 has an offset voltage specification of 150μV which is equivalent to 1 LSB absolute error in a 16-bit system. However, the OP-07 offset drift over temperature of 1.8μV/°C produces an additional 108μV

error over a 60°C temperature change (25°C to 85°C). The resulting total error over temperature becomes almost 2 LSBs.

For 18-bit accuracy, even the ultra-low offset voltage OP-177 (its best grade has 10μV initial offset and 18μV total Vos drift), barely makes the 1 LSB error limit of 38μV.

For absolute accuracy at the 18-bit level and beyond, chopper stabilized amplifiers may be used to meet the DC offset and drift requirements at the expense of increased noise levels due to the chopping action. Additional filtering must be employed to take full advantage of choppers, and they are generally more noisy than bipolar op amps for bandwidths above 0.1Hz.

More and more data acquisition systems which operate at resolutions of 16-bits or greater are being designed with auto-zeroing circuits or with periodic self-calibration in order to maintain absolute accuracy.

EFFECTS OF OP AMP OFFSET AND DRIFT ON SYSTEM ACCURACY

■ 741 Amplifer Has Offset Voltage of 6mV:	2 LSBs at 12-bits
■ OP-07 Has 25°C Offset Voltage of 150μV:	1 LSB at 16-bits
■ OP-07 Has Tempco of 1.8μV/°C:	1 LSB at 16-bits, ΔT = 60°C
■ OP-177 (Best Grade) Has 25°C Offset of 10μV:	1/4 LSB at 18-bits
■ OP-177 (Best Grade) Has Total Vos Drift of 18μV:	1/2 LSB at 18-bits

Figure 1.2

Besides evaluating the effects of electrical components on total error, mechanical and environmental issues must also be considered when designing precision systems. For example, the parasitic thermo-electric (bi-metallic) junction between copper and Kovar has a 18μV/°C temperature coefficient. Therefore, a 1°C temperature gradient across a PC board can generate as much as 2 LSBs error in a 20-bit system.

OTHER CONSIDERATIONS FOR HIGH ACCURACY SYSTEMS

- Chopper Stabilized Op Amps
- Auto-Zero and/or Self-Calibration
- Noise
- Mechanical Parasitic Thermoelectric Junctions

Figure 1.3

The effects of noise must also be considered in high-accuracy systems. Performance at the 22-bit level is often limited by noise. For example, the noise of the OP-177 in a 100Hz bandwidth is approximately 1μV p-p, 1/2 LSB at 22-bits. Indeed, even the tempco of the world's best reference (1ppm/°C) introduces a temperature drift of 4 LSBs/°C at 22-bits.

Clearly some extraordinary methods are necessary to achieve high levels of absolute accuracy. Some form of auto-calibration may be correct offset and gain scaling errors. Averaging data over long intervals minimizes random noise. However, these techniques often result in added cost and complexity.

In any event, all error sources (component-related and physical) must be well understood in order to successfully design precision systems. Figure 1.4 shows a list of common error sources and the approximate levels at which they become significant.

ERROR SOURCES AFFECT ABSOLUTE ACCURACY IN PRECISION SYSTEMS

ERROR SOURCE	12 Bits	14 Bits	16 Bits	18 Bits	20 Bits	22 Bits
Vos	X	X	X	X	X	X
Vos Drift			X	X	X	X
Ios			X	X	X	X
Ios Drift			X	X	X	X
Avol		X	X	X	X	X
CMRR				X	X	X
PSRR				X	X	X
Amplifier Noise				X	X	X
Resistor Tolerance	X	X	X	X	X	X
Resistor Tempco			X	X	X	X
Parasitic Tempco				X	X	X
Ground Noise	X	X	X	X	X	X
Layout Effects	X	X	X	X	X	X
Long Term Drift					X	X
Circuit Self-Heating			X	X	X	X

Figure 1.4

In a high precision system, all sources of error must be understood and evaluated. In the following sections of this seminar, we shall examine the various elements in the signal path from the transducer to the ADC. The error sources associated with each portion will be examined and appropriate remedies for them will be suggested.

SENSOR OUTPUT SIGNAL CONDITIONING EXAMPLES

There are resistive, capacitive, piezoelectric, and other types of sensors for different applications. There is no one universal interface design that can accommodate all sensor types. Within the resistive class of sensors, for example, resistances vary over a wide range, and biasing requirements differ depending on the individual sensor.

LOW IMPEDANCE, LOW VOLTAGE TRANSDUCERS

- RTD: 100Ω
- Thermocouple: Low Resistance, 10µV/°C to 50µV/°C Output Tempco
- Load-Cell, Strain Gauge: 350Ω to 10kΩ Bridge. Up to 100mV Fullscale Output
- Dynamic Microphone: 150Ω to 1500Ω, up to 50 - 100mV Fullscale Output

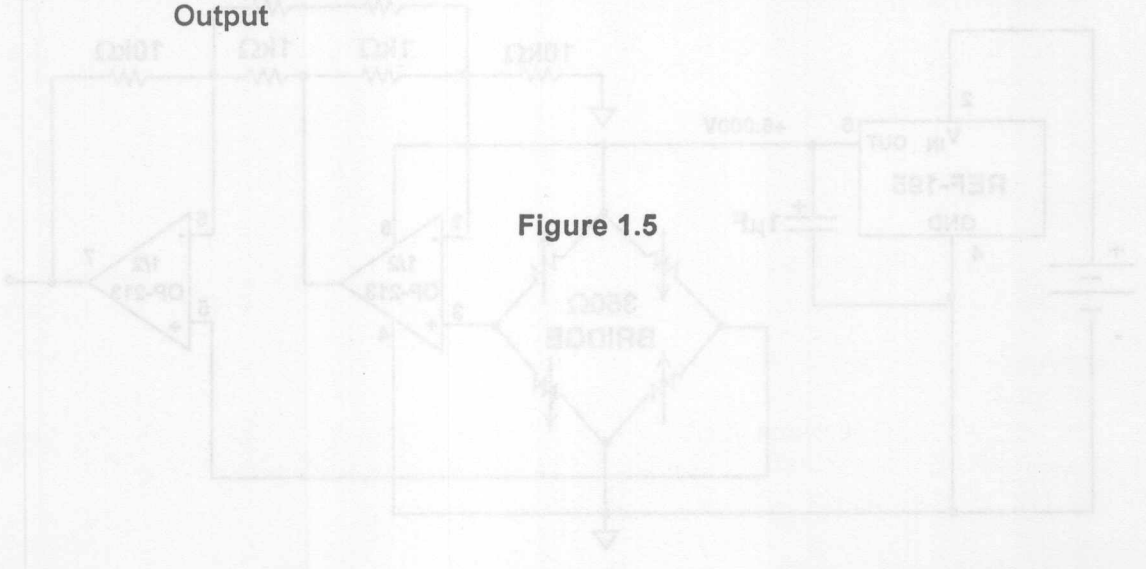


Figure 1.5

HIGH IMPEDANCE TRANSDUCERS

- Piezoelectric: 50kΩ to >10MΩ, µV to mV Output
- Photo-detector: >10MΩ, nA to µA Output
- Capacitive: >100MΩ

Figure 1.6

The following examples illustrate some very low level applications.

A PRECISION WEIGHT-SCALE AMPLIFIER

A precision weigh-scale transducer is usually configured as a 350Ω bridge. Figure 1.7 shows a load-cell amplifier that is powered from a single supply. The excitation voltage to the bridge must be precise and stable, otherwise it introduces an error in the measurement. In this circuit, a precision 5V reference is used as the bridge drive. The REF-195 reference can supply more than 30mA to a load, so it can drive the 350Ω bridge without the need of a buffer.

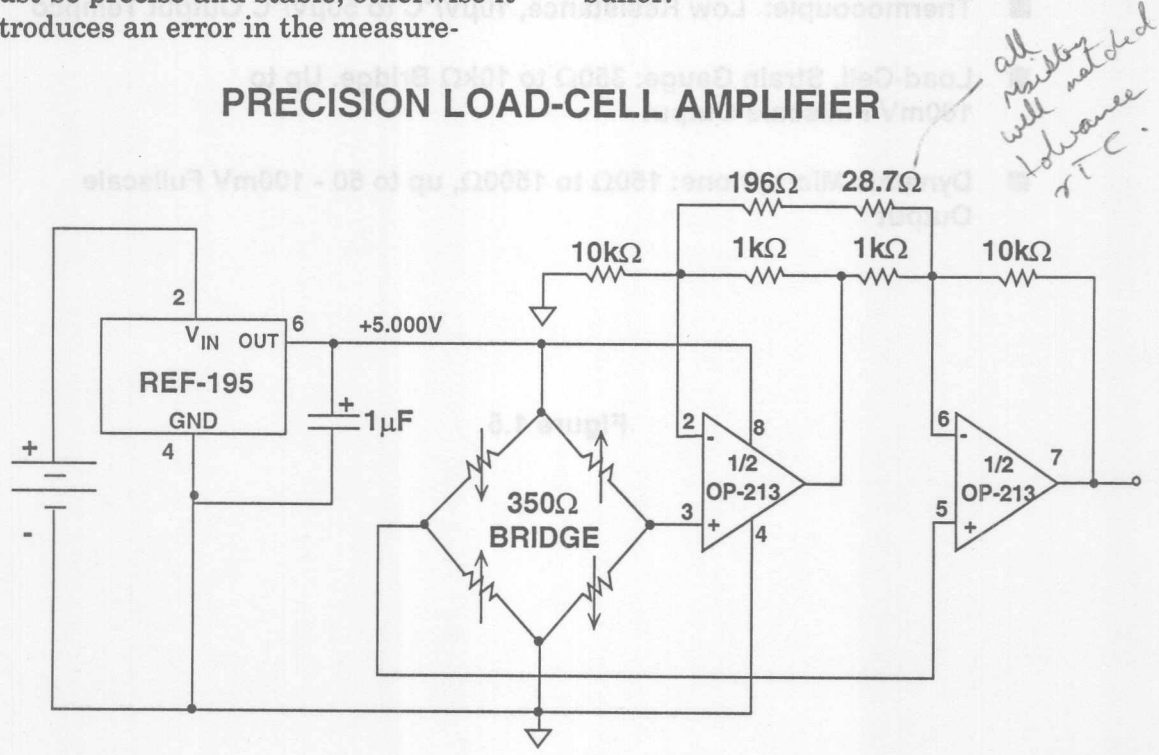


Figure 1.7

The bridge signal is amplified by the two OP-213 op amps connected as an instrumentation amplifier. The resistor network sets the gain according to the formula:

$$G = 1 + \frac{10k\Omega}{1k\Omega} + \frac{20k\Omega}{196\Omega + 28.7\Omega} = 100$$

For optimum common-mode rejection, the resistor ratios must be precise. High tolerance resistors (±0.5% or better) should be used.

For zero bridge signal, the amplifier will swing to within 2.5mV of 0V. This is the minimum output limit of the OP-213. Therefore, if an offset adjustment is required, one should start the adjustment from a positive voltage and adjust

downward until the output stops changing. This is the point where the amplifier limits the swing. Because of the single supply design, the amplifier cannot sense signals which have negative polarity.

THE TMP-01 TEMPERATURE SENSOR/CONTROLLER

The TMP-01 is a new device that simplifies the job of designing a temperature controller circuit. As the block diagram in Figure 1.8 shows, the TMP-01 combines a temperature sensor with two comparators in order to provide a voltage output that is proportional to temperature, and also to include open collector outputs which signal if the temperature has exceeded a high set point or dropped below a low set point. In addition, a built in hysteresis generator adjusts the comparators' trip points by a programmable amount to ensure that the outputs do not oscillate. The core of the TMP-01 is a temperature sensor and 2.5V bandgap reference. The temperature sensor output is 5mV/K, resulting in an output voltage of 1.49V at 25°C. The amount of hysteresis and the comparator trip points are determined by three external resistors, R1, R2, and R3. The formulae for choosing these resistors are given in the TMP-01 data sheet.

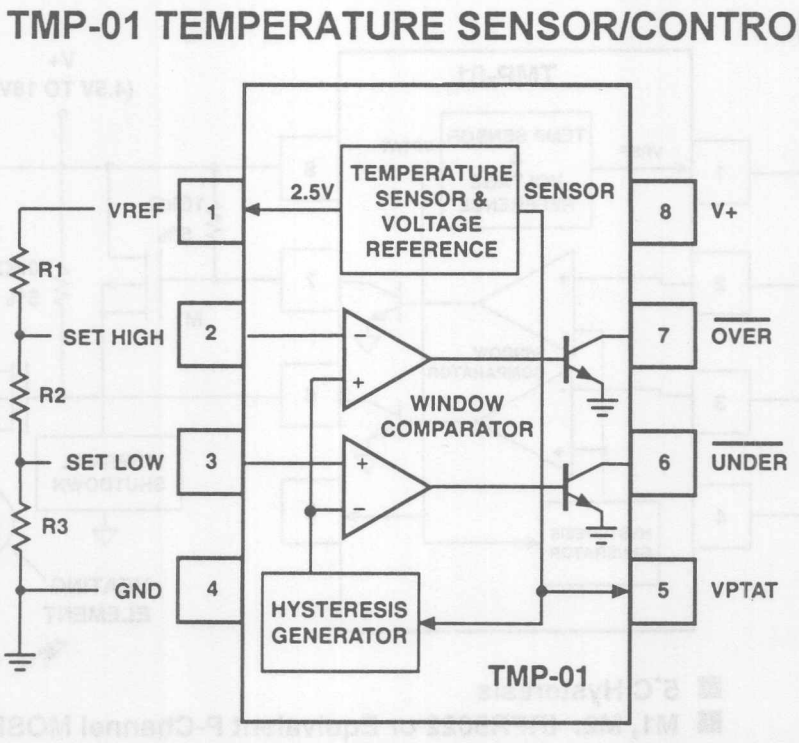
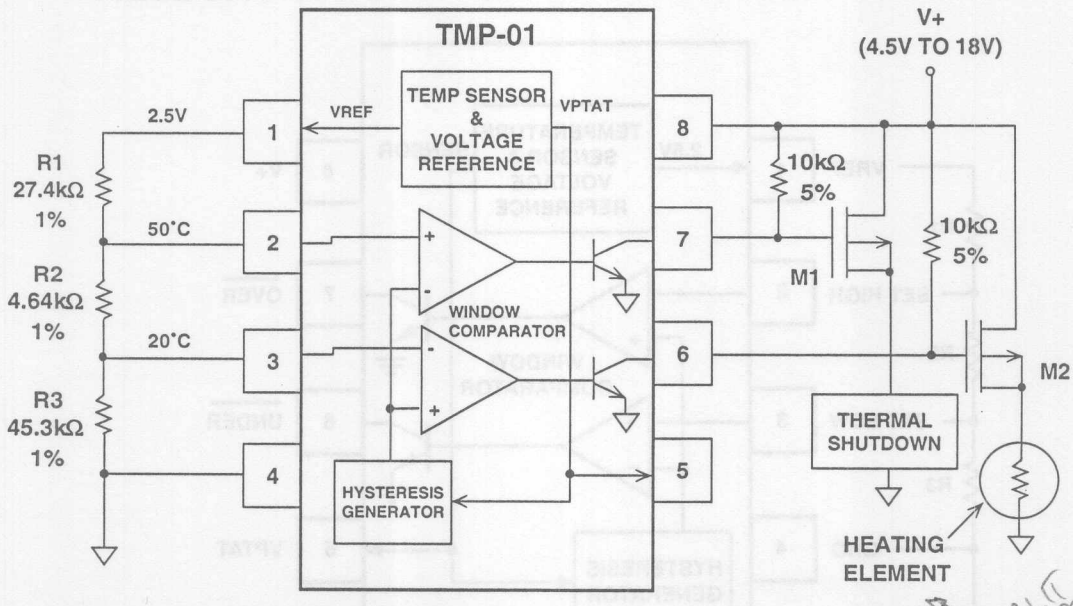


Figure 1.8

The versatility of the TMP-01 is illustrated in the temperature controller shown in Figure 1.9. In this case, the open collector outputs control a heating element and a thermal shutdown circuit to ensure that a piece of equipment is maintained within a predetermined temperature range. In this case, R1-R3 are chosen to give a low set point of 20°C and a high set point of 50°C, and 5°C of hysteresis. Thus when the temperature of the TMP-01 drops below 20°C, the negative input of the comparator has a higher voltage than the positive input, causing the open collector output at pin 6 to turn on. This brings the gate of the p-channel MOSFET, M2, low, turning on the transistor and allowing current to flow through the heating element. The heating element stays on until the temperature rises above 25°C (the set point plus the hysteresis), when the output transistor turns off M2 off. The same process occurs when the temperature rises above the high set point, except that here some type of thermal shutdown or cooling circuit is activated. Additionally, the temperature output pin of the TMP-01 can be connected to an ADC to continually monitor the system temperature. Overall, the TMP-01 combines a high degree of functionality with an easily used, space saving 8-pin dip or SOIC package.

HIGH/LOW SETPOINTS CONTROL CIRCUIT TEMPERATURE



- 5°C Hysteresis
- M1, M2: IRFR9022 or Equivalent P-Channel MOSFETs

Figure 1.9

SINGLE SUPPLY LINEARIZED RTD AMPLIFIER

Linearization of transducer outputs is more difficult when there is only one supply available. Figure 1.10 shows a single supply circuit to correct the nonlinear behavior of a Platinum Resistor Temperature Detector (RTD) device. The RTD operates in one leg of a full bridge circuit that is excited by a constant current source established by 1/2 of an OP-295 dual op amp. The bridge current is regulated by servoing the bridge current flowing into resistor RSENSE and comparing with a 200μV reference voltage derived from the REF-43.

PRECISION SINGLE SUPPLY RTD AMPLIFIER WITH LINEARIZATION

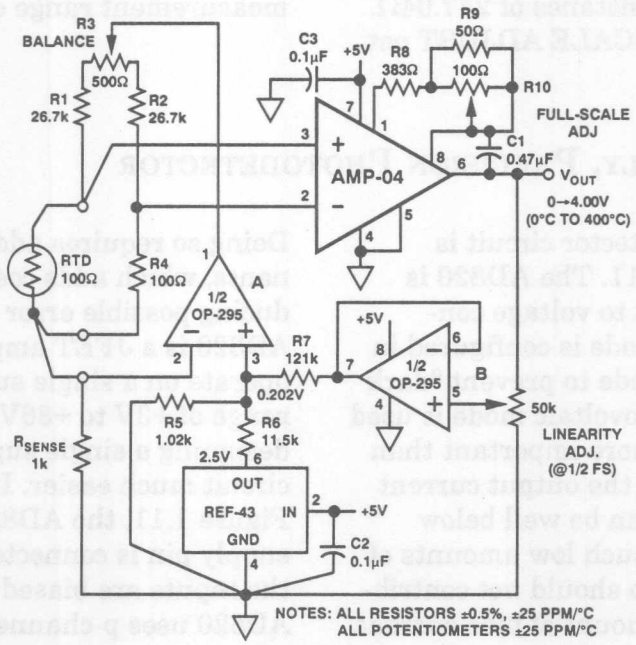


Figure 1.10

The temperature-dependent resistance change is amplified by the instrumentation amplifier AMP-04. Scaling is such that for 0°C the amplifier output is 0V, and at 400°C the amplifier output is +4.00V.

The RTD has an inherent curvature in its resistance-versus-temperature transfer function. If uncorrected, the sensor's nonlinearity would produce a 20°C error over the 400°C temperature range. This nonlinearity can be corrected by providing a small amount of positive feedback to the reference voltage, which increases the bridge current at high temperatures. The amount of positive feedback is sufficiently small as not to cause a stability problem in the circuit.

Calibration is an interactive three-step procedure. First set the FULL-SCALE and LINEARITY potentiometers to the

middle of their adjustment ranges. The first calibration is made with the zero adjust, and it should be made at a voltage other than zero since zero-volts is the negative voltage limit of the circuit and is indistinguishable from a zero-volt signal. A convenient zero calibration point is +5°C. The procedure is to substitute a known, stable 101.95Ω resistor in place of the RTD and then adjust the ZERO ADJUST potentiometer for 0.050V at the output.

Next substitute the full-scale (400°C) equivalent RTD resistance of 247.04Ω. Adjust the FULL-SCALE ADJUST pot for a 4.000V at the output. Then substitute the resistance corresponding to half-scale (200°C), or 175.84Ω. Adjust the LINEARITY ADJUST pot for a 2.000V output. Since the FULL-SCALE and LINEARITY adjustments are interactive it is necessary to repeat the calibration routine once or twice until no further adjustment is necessary.

Once calibrated, the amplifier is accurate to better than ±0.5°C within the 0°C to 400°C measurement range. If a higher supply voltage is available, the measurement range can be increased.

A SINGLE SUPPLY, PRECISION PHOTODETECTOR

A common photodetector circuit is shown in Figure 1.11. The AD820 is used as the current to voltage converter. The photodiode is configured in the photovoltaic mode to prevent "dark current." The photovoltaic mode is used when accuracy is more important than speed. In this case, the output current of the photodiode can be well below 100pA. To resolve such low amounts of current, the op amp should not contribute a significant amount of bias current. compared to the photodiode. For this reason JFET op amps are commonly used as the current to voltage converters in such applications.

JFET amplifiers are usually designed to operate with dual supplies. As a result, to build a single supply photodetector, the inputs need to be biased within the common mode range of the amplifier. Doing so requires additional components, which adds cost as well as introducing possible error sources. The AD820 is a JFET amplifier designed to operate on a single supply over the range of +3V to +36V, which makes designing a single supply photodetector circuit much easier. In the circuit in Figure 1.11, the AD820's negative supply pin is connected to ground, and the inputs are biased at ground. The AD820 uses p-channel JFETs, which allows the gate to operate at the negative supply potential while still maintaining the input stage in its linear region. This particular circuit uses a 100MΩ resistor to convert the current output of the photodiode to a voltage. Care must be taken to minimize leakage paths at the inverting input node of the op amp. (Section 3 of Reference 1.)

SINGLE SUPPLY, PRECISION PHOTODETECTOR

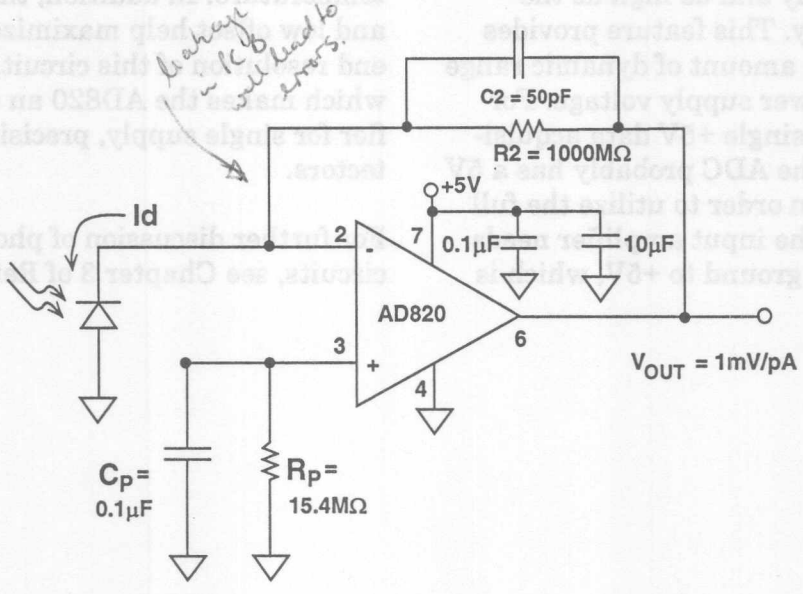


Figure 1.11

AD820 SINGLE SUPPLY FET INPUT OP AMP FEATURES

- Single Supply Operation: +3V to +36V
- Dual Supply Operation: ±1.5V to ±18V
- Output Swings Rail to Rail
- Low Power: 600µA Supply Current Maximum
- Input Offset Voltage: 200µV Maximum
- Input Bias Current: 25pA Maximum
- Low Noise: 13nV/√Hz at 10kHz
- Unity Gain Bandwidth: 1.8MHz
- Slew Rate: 3V/µs

Figure 1.12

Other features of the AD820 are listed in Figure 1.12. Another advantage of the AD820 is that its output stage can swing from rail-to-rail. In other words, the output can swing as low as the negative supply and as high as the positive supply. This feature provides the maximum amount of dynamic range for a given power supply voltage. For example, in a single +5V data acquisition system, the ADC probably has a 5V input range. In order to utilize the full input swing, the input amplifier needs to swing from ground to +5V, which is exactly what the AD820 can do. The low end accuracy of the photodetector circuit is limited mainly by the bias current of the amplifier. The AD820 has a very low 25pA maximum at room temperature. In addition, the low noise and low offset help maximize the low end resolution of this circuit, all of which makes the AD820 an ideal amplifier for single supply, precision photodetectors.

For further discussion of photodiode circuits, see Chapter 3 of Reference 1.

REMOTE SENSOR APPLICATION PROBLEMS

When a sensor is located an appreciable distance away from its electronics, noise pickup or ground loop problems frequently occur. The measurement system's circuits may be exposed to potentially damaging electrical levels. Protection circuits must be provided to prevent catastrophic failures. It is important to understand how these problems arise in order to deal with them effectively. This chapter discusses various shielding, filtering, and input protection techniques which can prove helpful in the design of a system.

SHIELDING LONG CABLES AGAINST NOISE PICKUP

A cable that is more than a few inches long may act as an antenna, picking up extraneous noise from radio frequency (RF) sources or other electromagnetic (EM) sources. In a high noise environment, it is often necessary to shield the cable. However, shielding alone is not sufficient to eliminate noise pickup. One must also ground the shield properly. It is not always clear where to ground the shield. Grounding at the wrong place not only renders the shield ineffective, it may also introduce unwanted ground current loops.

To study this problem, the precision RTD amplifier circuit shown in Figure 1.15 was used as the basis for a series

REMOTE SENSING: AN ENGINEER'S NIGHTMARE

- RF Noise Pickup
- EMI Noise Pickup
- Where to Ground Shields to Avoid Ground Loops
- Wire Resistance Introduces Errors

Figure 1.13

AN IMPROPERLY GROUNDED CABLE SHIELD IS A POTENTIAL NOISE GENERATOR

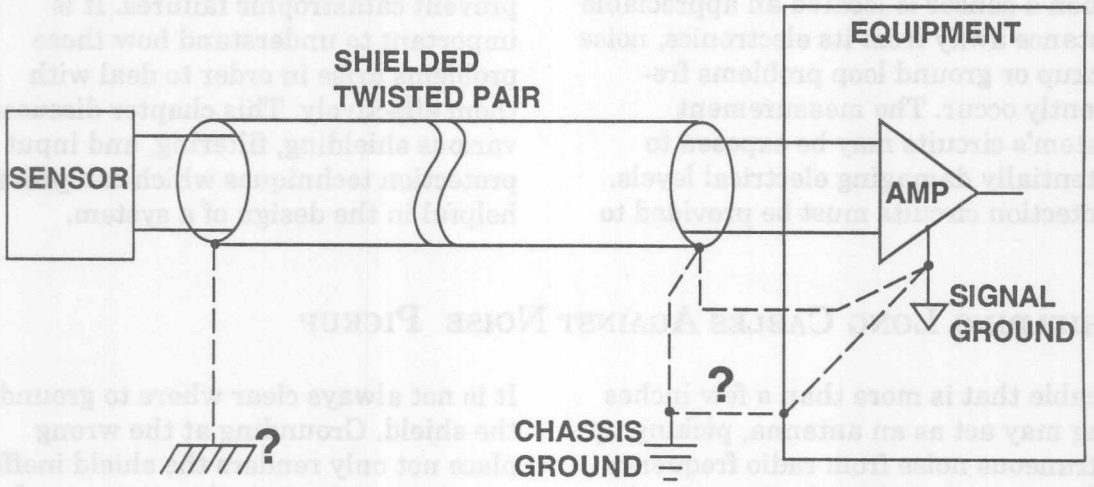


Figure 1.14

EXPERIMENT: A 100Ω RTD LOCATED 10 FEET FROM INSTRUMENT

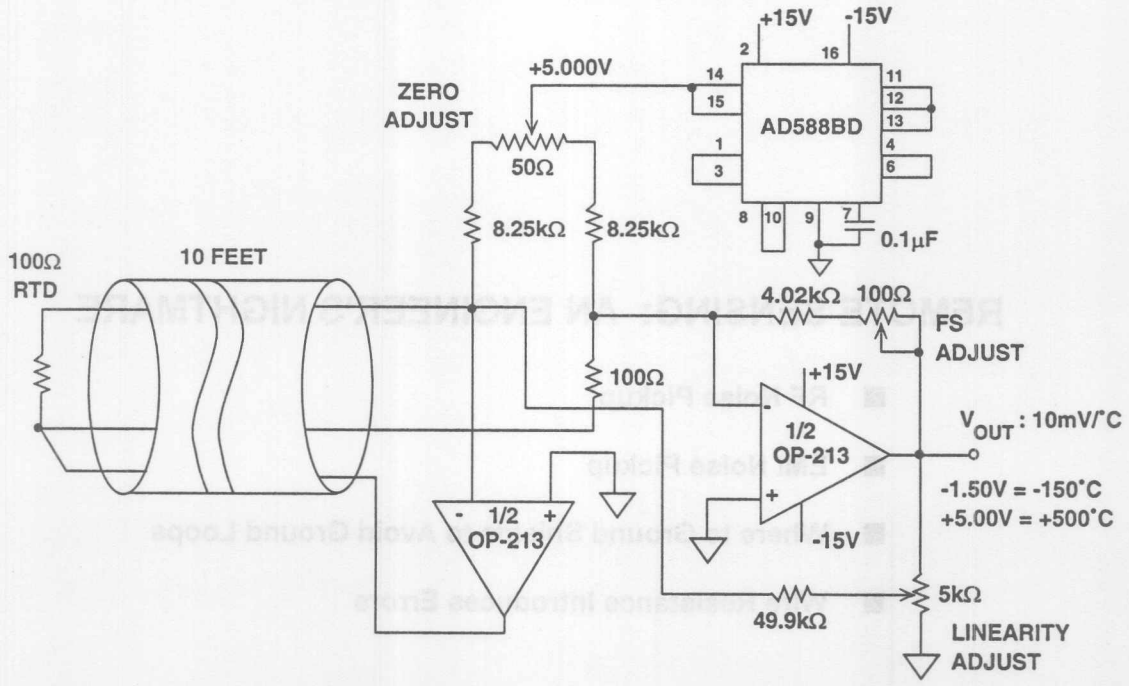
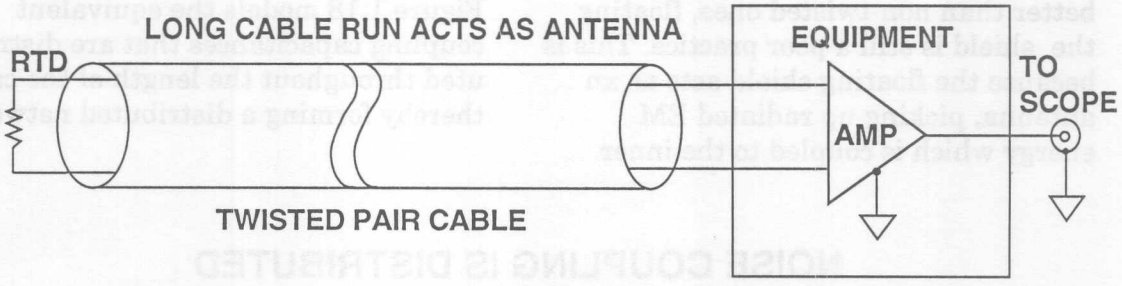


Figure 1.15

of experiments. The remote 100Ω RTD was connected to the amplifier circuit using 10 feet of four-wire cable (2 twisted pairs twisted inside a shield). Measurements were made with the shield grounded at various places along the length of the cable.

EXPERIMENT 1: UNSHIELDED, OR SHIELD LEFT FLOATING



VERTICAL SCALE: 2mV/div.
HORIZONTAL SCALE: 10ms/div.

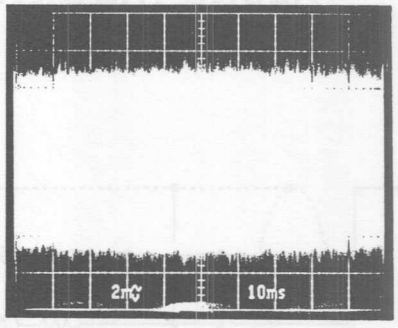


Figure 1.16

FLOATING SHIELD COUPLES ELECTROMAGNETIC ENERGY TO CENTER CONDUCTORS

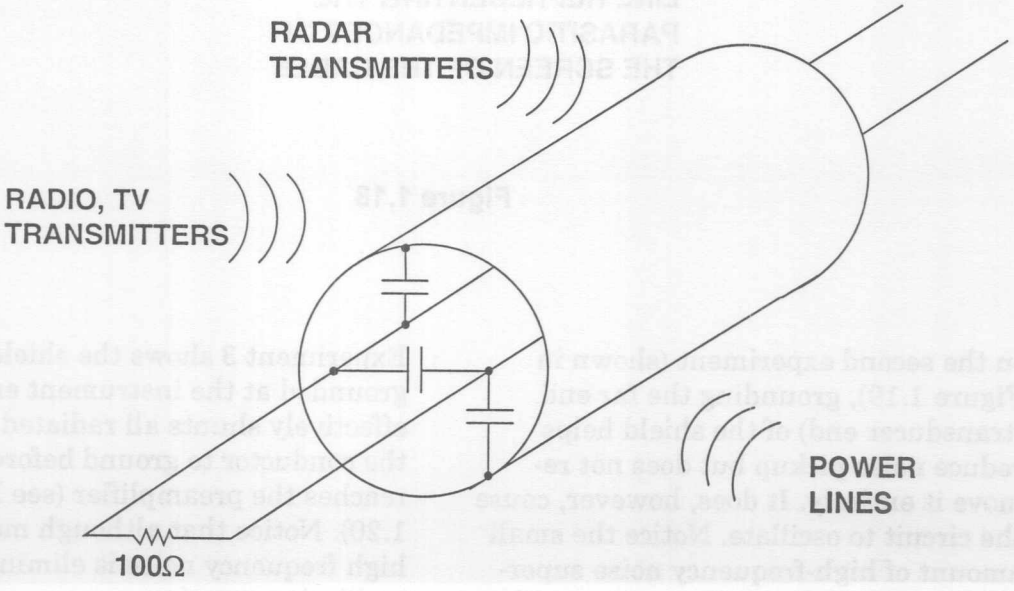


Figure 1.17

In the first experiment, the shield was left floating. A large amount of noise was recorded at the output of the amplifier (refer to Figure 1.16). Even though twisted pair wires are generally much better than non-twisted ones, floating the shield is still a poor practice. This is because the floating shield acts as an antenna, picking up radiated EM energy which is coupled to the inner conductors. Figure 1.17 shows how the shield forms a capacitance which couples the signals to the center conductors.

Figure 1.18 models the equivalent coupling capacitances that are distributed throughout the length of the cable, thereby forming a distributed network.

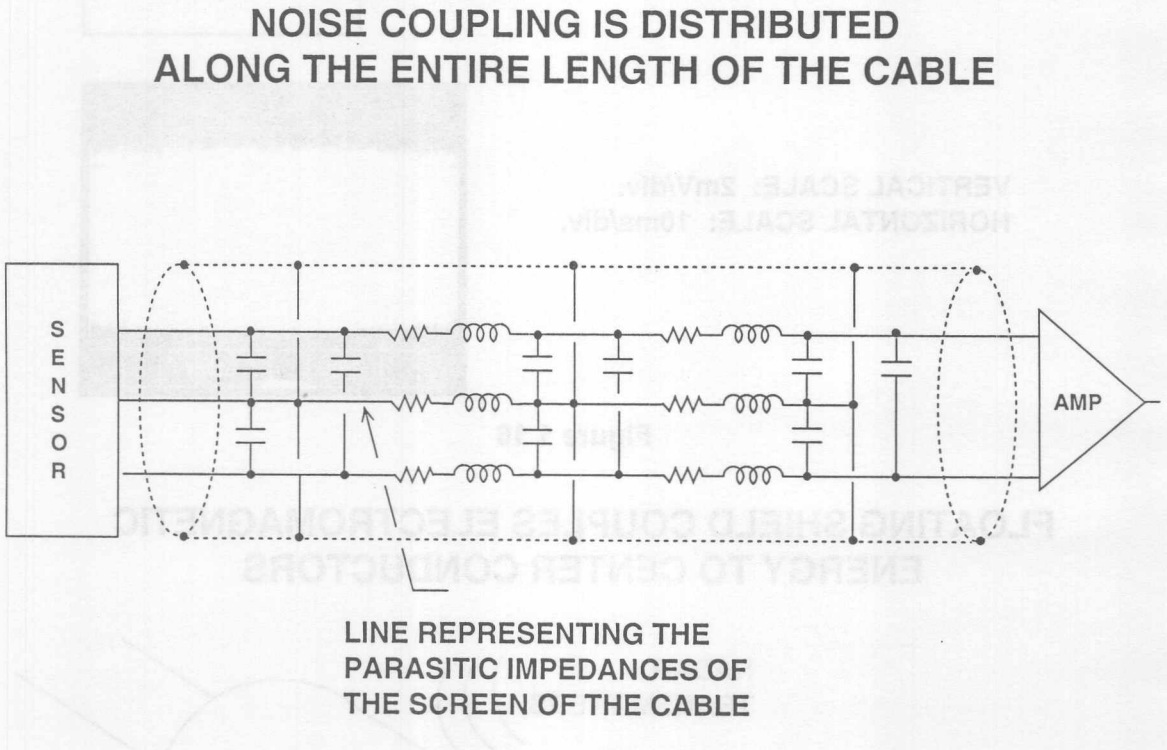


Figure 1.18

In the second experiment (shown in Figure 1.19), grounding the far end (transducer end) of the shield helps reduce noise pickup but does not remove it entirely. It does, however, cause the circuit to oscillate. Notice the small amount of high-frequency noise superimposed on the lower frequency oscillation.

Experiment 3 shows the shield grounded at the instrument end. This effectively shunts all radiated noise in the conductor to ground before it reaches the preamplifier (see Figure 1.20). Notice that although most of the high frequency noise is eliminated the oscillation remains.

EXPERIMENT 2: GROUNDING SHIELD AT FAR END

Problem: Oscillation and RF Noise Coupling at Near End

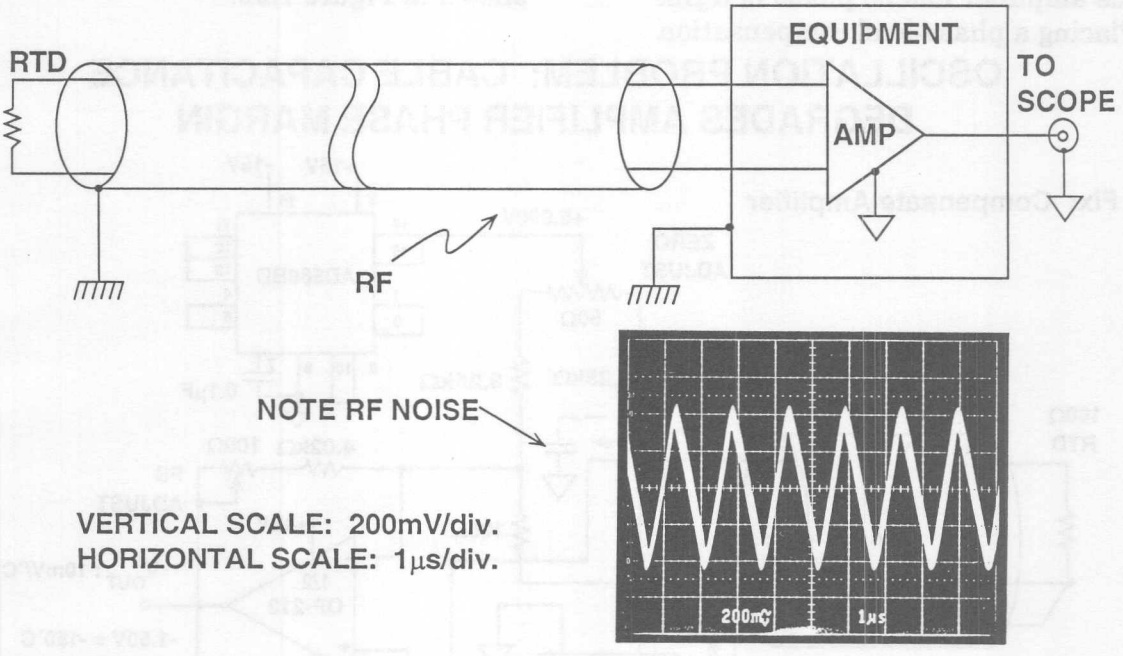


Figure 1.19

EXPERIMENT 3: SHIELD GROUNDED AT NEAR END

Result: RF Noise Eliminated, but Cable Capacitance Induces Oscillation

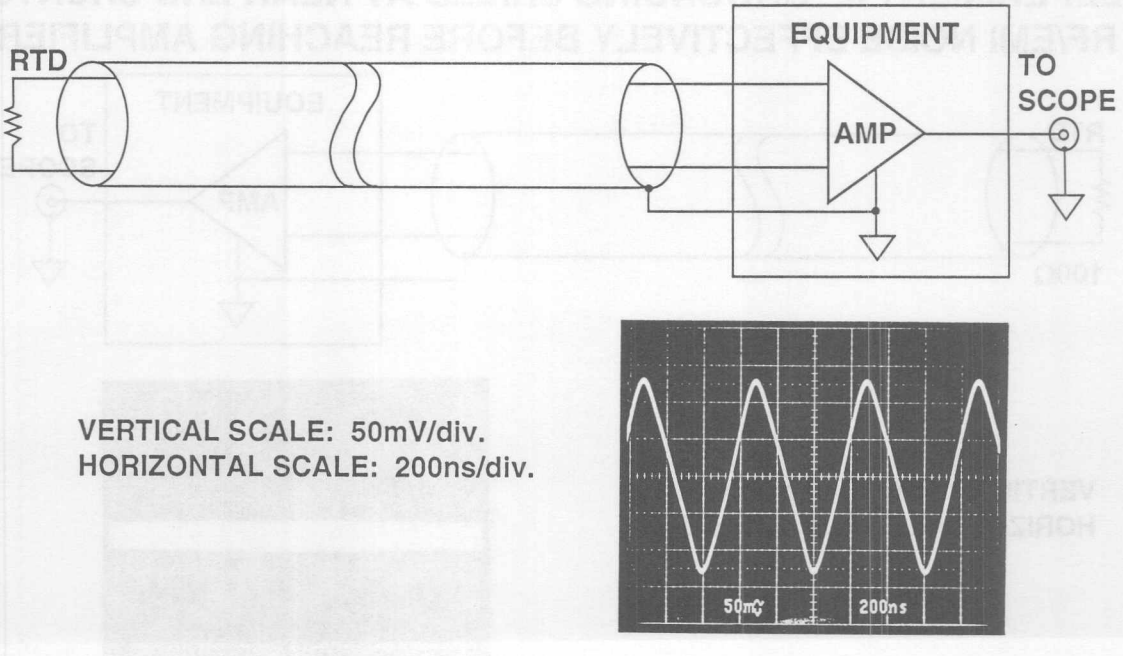


Figure 1.20

The oscillation is caused by cable capacitance which appears at the summing junction of the bridge biasing amplifier (refer to Figure 1.21) and increases the phase-lag. Consequently the amplifier has no phase margin. Placing a phase-lead compensation network around the feedback of the bridge biasing amplifier restores the phase margin of the amplifier and therefore stabilizes it. The result is lower noise and restored stability as shown in Figure 1.22.

OSCILLATION PROBLEM: CABLE CAPACITANCE DEGRADES AMPLIFIER PHASE MARGIN

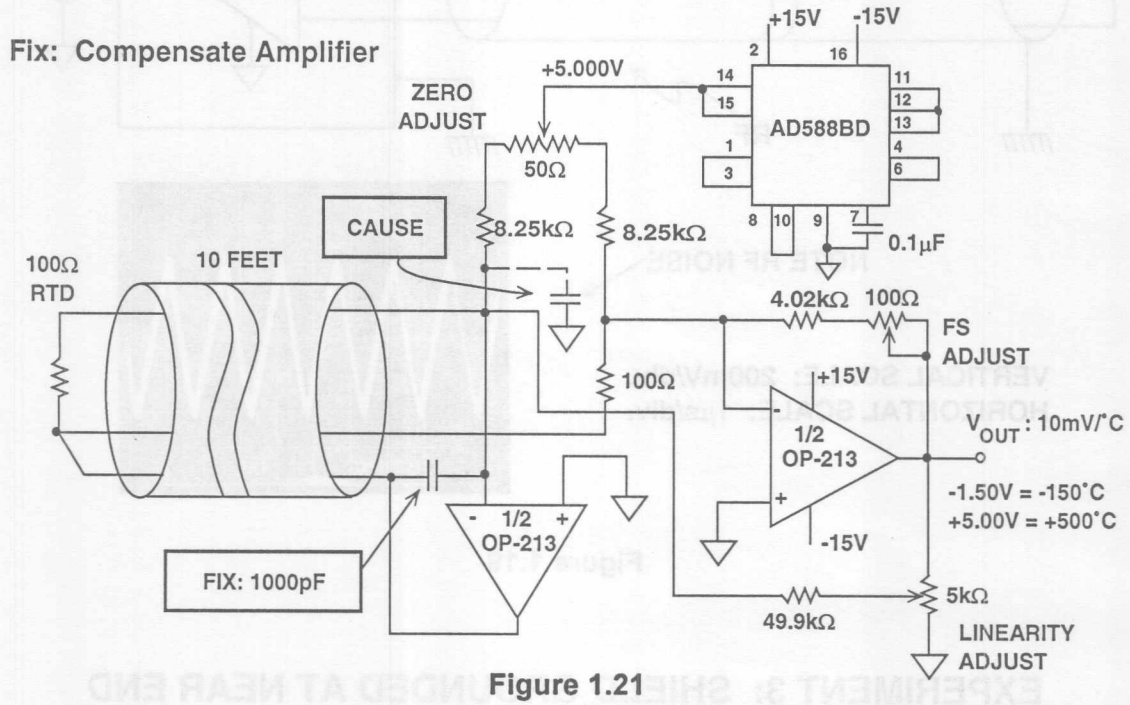
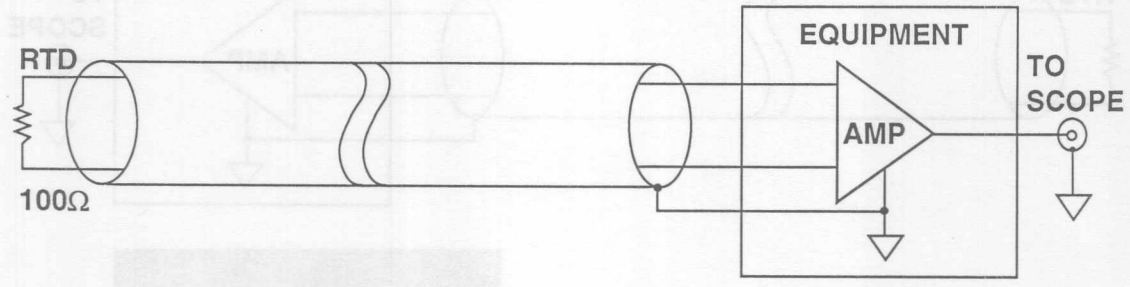


Figure 1.21

EXPERIMENT 4: GROUNDING SHIELD AT NEAR END SHUNTS RF/EMI NOISE EFFECTIVELY BEFORE REACHING AMPLIFIER



VERTICAL SCALE: 2mV/div.
HORIZONTAL SCALE: 10ms/div.

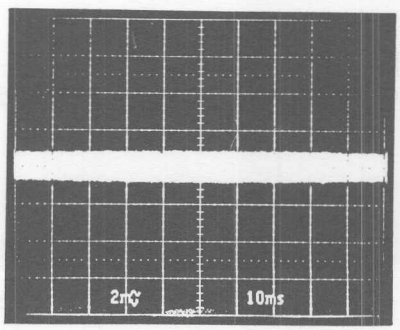
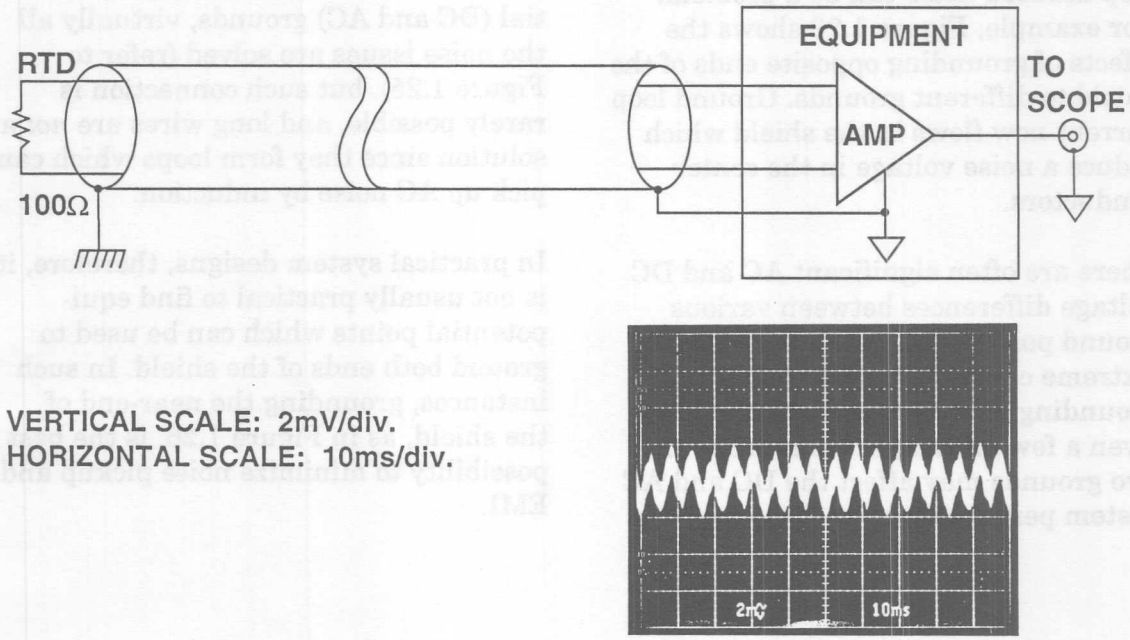


Figure 1.22

EXPERIMENT 5: AVOID DIFFERENT GROUNDS AT OPPOSITE ENDS OF THE SHIELD TO PREVENT GROUND LOOPS



VERTICAL SCALE: 2mV/div.
HORIZONTAL SCALE: 10ms/div.

Figure 1.23

SIGNAL GROUND AND EARTH GROUND HAVE DIFFERENT POTENTIALS WHICH MAY INDUCE GROUND LOOP CURRENT

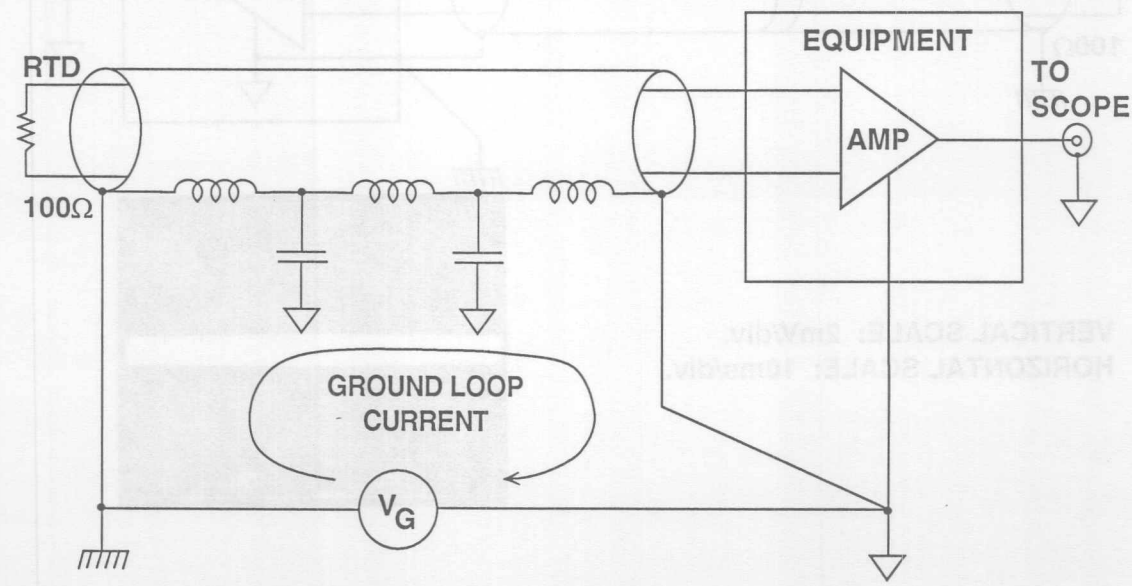


Figure 1.24

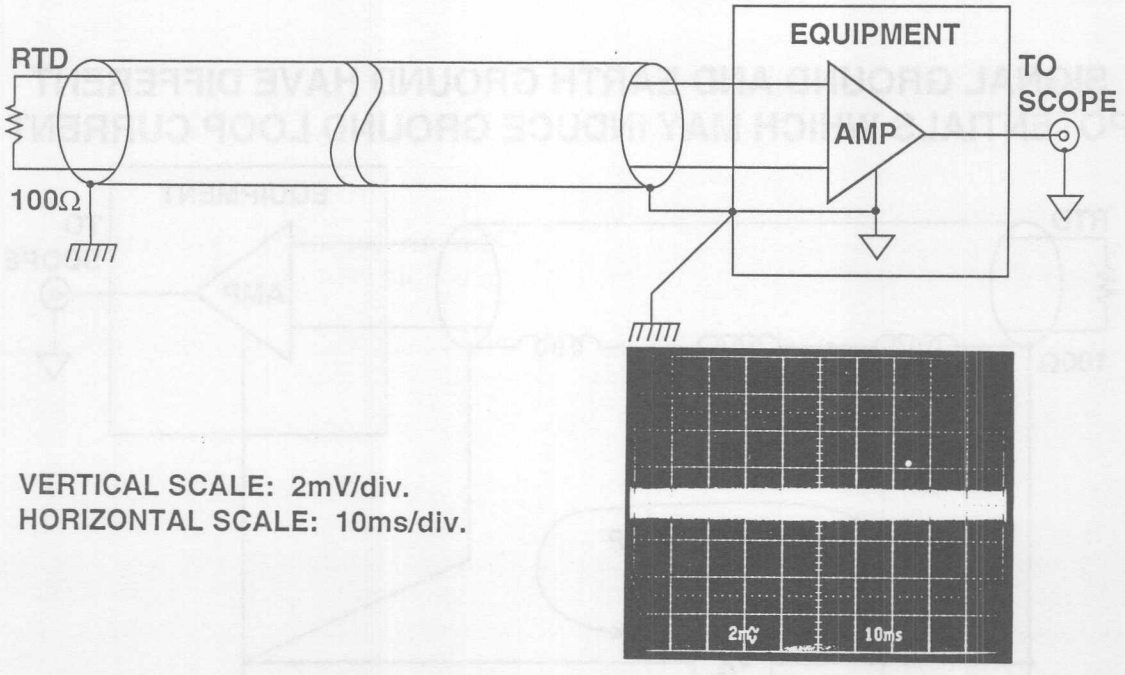
Without care in shield design, ground-loop induced noise can be a problem. For example, Figure 1.23 shows the effects of grounding opposite ends of the shield to different grounds. Ground loop current now flows in the shield which induce a noise voltage in the center conductors.

There are often significant AC and DC voltage differences between various ground points in a system's chassis. Extreme care is necessary when grounding a cable shield at both ends. Even a few millivolts difference in the two grounds may affect the DC and AC system performance.

In experiment 6, if the two ends of the shield can be connected to equi-potential (DC and AC) grounds, virtually all the noise issues are solved (refer to Figure 1.25), but such connection is rarely possible, and long wires are *not* a solution since they form loops which can pick up AC noise by induction.

In practical system designs, therefore, it is not usually practical to find equi-potential points which can be used to ground both ends of the shield. In such instances, grounding the near-end of the shield, as in Figure 1.26, is the best possibility to minimize noise pickup and EMI.

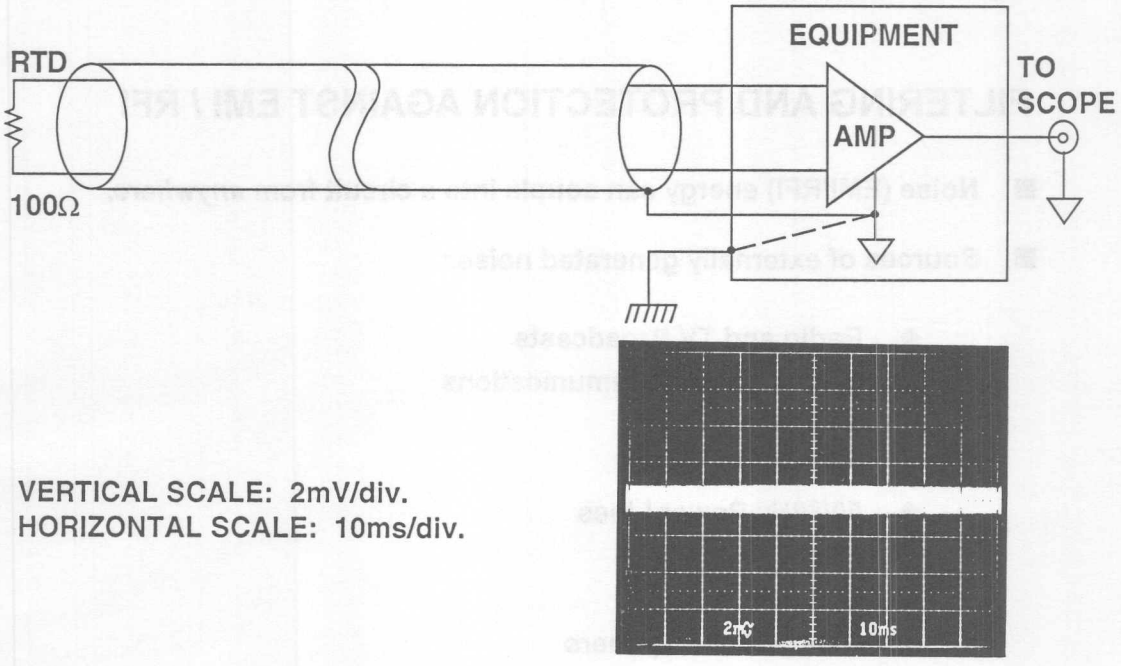
EXPERIMENT 6: TRY TO GROUND THE SHIELD AT BOTH ENDS TO THE SAME POTENTIAL TO KEEP NOISE LOW



VERTICAL SCALE: 2mV/div.
HORIZONTAL SCALE: 10ms/div.

Figure 1.25

EXPERIMENT 7: WHERE EQUI-POTENTIAL GROUNDS ARE NOT POSSIBLE, GROUND SHIELD ONLY AT THE NEAR END



VERTICAL SCALE: 2mV/div.
HORIZONTAL SCALE: 10ms/div.

Figure 1.26

FILTERING AND PROTECTION AGAINST EMI/RFI

Circuit accuracy is affected by nearby electrical activity. This electrical activity may generate noise and is referred to as EMI (electromagnetic interference) or RFI (radio frequency interference). In this section, EMI will refer to both electromagnetic and radio frequency interference. EMI can be caused by:

1. Interference due to conduction (common-impedance),
2. Interference due to capacitive or inductive coupling (near-field interference), and
3. Electromagnetic radiation (far-field interference).

There are countless ways in which noise can couple into a sensitive circuit to ruin its accuracy. There are many types of noise sources, and some are listed in Figure 1.27.

Noise Coupling Mechanisms

RF energy may enter wherever there is an impedance mismatch or discontinuity in a system. In general this occurs at the interface where cables carrying sensitive analog signals are connected to PC boards, and through power supply leads. Improperly connected cables or poor supply filtering schemes are perfect conduits for interference. Figure 1.28 shows some of the ways noise can enter into a circuit.

FILTERING AND PROTECTION AGAINST EMI / RFI

- Noise (EMI/RFI) energy can couple into a circuit from *anywhere.*
- Sources of externally generated noise:
  - Radio and TV Broadcasts
  - Mobile Radio Communications
  - Ignition
  - Lightning
  - 50/60Hz Power Lines
  - Electric Motors
  - Computers
  - Garage Door Openers
  - Telemetry Equipment

Figure 1.27

HOW IS INTERFERENCE COUPLED?

- Impedance mismatches and discontinuities
- Common-mode impedance mismatches → Differential Signals
- Capacitively Coupled (Electric Field Interfence)
  - dV/dt → Mutual Capacitance → Noise Current
  - Example: 1V/ns produces 1mA/pF
- Inductively Coupled (Magnetic Field)
  - di/dt → Mutual Inductance → Noise Voltage
  - Example: 1mA/ns produces 1mV/nH

Figure 1.28

Conducted noise may be encountered when two or more currents share a common path (impedance). This common path is often a high impedance "ground" connection. If two circuits share this path, noise currents from one will produce noise voltages in the other. In Reference 5, A. Rich outlines steps which may be taken to identify potential sources of interference.

There is a capacitance between any two conductors separated by a dielectric (air and vacuum are dielectrics, as well as all solid or liquid insulators). If there is a change of voltage on one conductor there will be change of charge on the other, and a "displacement current" will flow in the dielectric. Where capacitance or dV/dT is high, noise is easily coupled by this mechanism. (1V/ns gives rise to displacement currents of 1 mA/pF.)

If changing magnetic flux from current flowing in one circuit threads another circuit, it will induce an emf in the second circuit. Such "mutual inductance" can be a troublesome source of noise coupling from circuits with high values of dI/dT. (In a mutual inductance of 1nH, a changing current of 1A/ns will induce an emf of 1V.)

Reducing Common-Impedance Noise

Steps to be taken to eliminate or reduce noise due to the sharing of impedances are outlined in Figure 1.29.

SOLUTIONS TO EXTERNALLY-INDUCED INTERFERENCE

- Common-Impedance Noise
  - Decouple IC power supply leads at LF and HF
  - Reduce the common impedance
  - Eliminate shared paths
- Techniques
  - Tantalum electrolytic (LF) and ceramic (HF) bypass capacitors
  - Ground and Power Planes
  - Reconfigure the system design

Figure 1.29

Power supplies are an example of impedance shared among several circuits. Voltage sources may exhibit low output impedances or may not — especially over frequency. Furthermore the wiring used to distribute the power is inductive and resistive and may also form a ground loop.

The use of power and ground planes also reduces the impedance of power distribution circuits. These dedicated layers of conductors in a PCB are continuous and offer the lowest practical resistance and inductance. However, they are not perfect conductors, and there are some applications where reducing the common impedance using this method is not sufficient, and others where it is uneconomic.

Power supply impedance at individual ICs should be reduced by proper AC decoupling. A capacitor is connected between the supply pins of the IC which has low reactance at all frequencies present in the IC's supply current. Monolithic ceramic capacitors with short (and therefore low-inductance) leads are excellent for HF decoupling, but do not have sufficiently low reactance at lower frequencies, while tantalum electrolytic capacitors have excellent LF and MF performance but are somewhat inductive at HF. Every supply pin of every IC should be decoupled at HF with a 10-100 nF ceramic capacitor within 1-2 mm of the supply pin, but it may only be necessary to use one 10-22 μF tantalum capacitor for every few ICs, provided the length of conductor to it is no more than 3-5 cm. For more details on decoupling see Paul Brokaw's articles (References 4 & 7).

In some applications where low-level signals encounter high levels of common-impedance noise it will not be possible to prevent interference and the system architecture may need to be changed. Possible changes include:

1. Transmitting signals in differential form
2. Amplifying signals to higher levels
3. Converting signals into currents
4. Converting signals directly into digital form.

NOISE INDUCED BY NEAR-FIELD INTERFERENCE

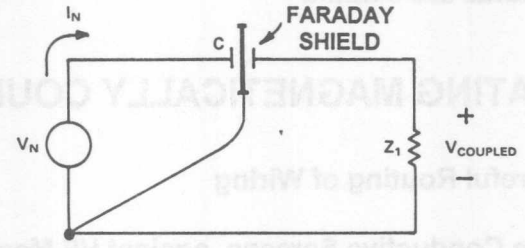
Crosstalk is the second commonest form of interference. In the vicinity of the noise source, interference is not transmitted as an electromagnetic wave, and the term "crosstalk" may apply to inductively or capacitively coupled signals.

Reducing Capacitively-Coupled Noise

Capacitively-coupled noise may be reduced by reducing the capacity (by increased separation of conductors), but is most easily cured by shielding. A grounded conducting shield (known as a "Faraday Shield") between the signal source and the affected node will eliminate capacitively-coupled noise by routing the displacement current directly to ground (Figure 1.30). It is *essential* that a Faraday Shield is grounded: a floating or open-circuit shield almost invariably increases capacitively-coupled noise.

FARADAY SHIELDING

FARADAY SHIELD INTERRUPTS THE COUPLING ELECTRIC FIELD



EQUIVALENT CIRCUIT ILLISTRATES HOW A FARADAY SHIELD CAUSES THE NOISE CURRENTS TO RETURN TO THEIR SOURCE WITHOUT FLOWING THROUGH Z_1

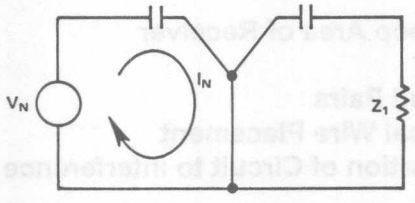


Figure 1.30

For a brief review of shielding consult the appendix, for more details consult Ott (Reference 2) and Morrison (Reference 3).

ELIMINATING CAPACITIVELY COUPLED NOISE

- Reduce Noise Sources of High dV/dt
- Proper Grounding Schemes for Cable Shields
- Reduce Stray Capacitance
  - Equalize Input Lead Lengths
  - Keep Traces Short
  - Use Signal-Ground-Signal Routing Schemes
- Use Grounded Conductive Faraday Shields to Protect Against Electric Fields

Figure 1.31

Reducing Magnetically-Coupled Noise

Methods to eliminate interference caused by magnetic fields are summarized in Figure 1.32.

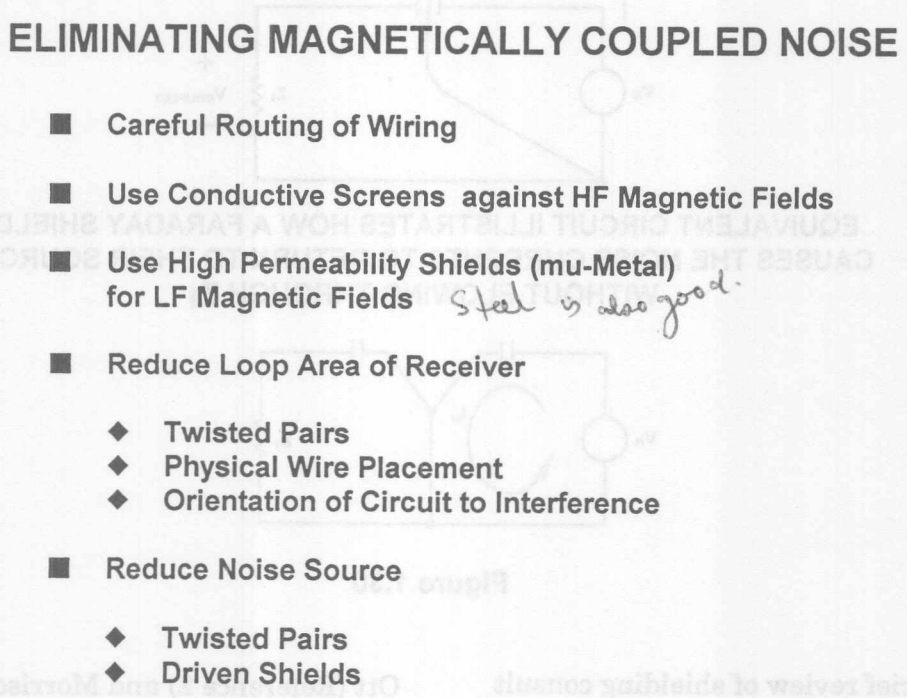


Figure 1.32

To illustrate the effect of magnetically-coupled noise, consider a circuit with a closed-loop area A cm^2 operating in a magnetic field with an rms flux density value of B gauss. The noise voltage induced in this circuit can be expressed by the following equation:

$$V_n = 2 \pi f B A \cos\theta \times 10^{-8} V.$$

In this equation, f represents the frequency of the magnetic field and θ represents the angle of the magnetic field B to the circuit with loop area A. The magnetic field coupling can be reduced by reducing the circuit loop area, the magnetic field intensity, or the angle of incidence. To reduce the circuit loop area requires arranging the circuit conductors closer together.

Twisting the conductors together reduces the net area of the loop, which has the effect of canceling any magnetic field pickup because the sum of positive and negative incremental loop areas is ideally equal to zero. Reducing the magnetic field directly may be difficult. However, since magnetic field intensity is inversely proportional to the cube of the distance from the source, physically moving the affected circuit away from the magnetic field has a very great effect in reducing the induced noise voltage. Finally, if the circuit is placed perpendicular to the magnetic field, pickup is minimized. If the circuit's conductors are in parallel to the magnetic field the induced noise is maximized because the angle of incidence is zero.

There are also techniques that can be used to reduce the amount of magnetic-field interference at its source. In the previous paragraph, the conductors of the receiver circuit were twisted together to cancel the induced magnetic field along the wires. If the source of the magnetic field is large currents flowing through nearby conductors, these wires can be twisted together to reduce the net magnetic field. Another technique is to use the shield of a cable as a return. If the shield current is equal to the current in the center conductor the net external magnetic field is zero.

Shields and cans are not nearly as effective against magnetic fields as against electric fields, but can be useful on occasion. At low frequencies magnetic shields using high-permeability material such a Mu-metal can provide modest attenuation of magnetic fields. At high frequencies simple conductive shields are quite effective provided that the thickness of the shield is greater than the skin depth (at the frequency involved) of the conductor used. (For copper the skin depth is $6.6/\sqrt{f}$ cm, where f is in Hz).

Passive Components: Your Arsenal Against EMI

Passive components, such as resistors, capacitors, and inductors, are powerful tools for reducing externally induced interference when used properly. Figure 1.33 summarizes the more popular low-pass filters for minimizing EMI.

USING PASSIVE COMPONENTS TO ELIMINATE EMI

LP FILTER TYPE	ADVANTAGES	DISADVANTAGE
R-C	Noise Voltage → Heat Inexpensive	Thermal Noise $I_B R$ Drop
L-C (Bifilar) Bifilar	No Thermal Noise No IR Drop Inexpensive	e_n across L Nonlinear Core Effects
Pi (C - L - C)	Packaged Filters Low Resistance Feedthru Capacitors Low Insertion Loss High Attenuation	Expensive Nonlinear Core Effects

Figure 1.33

Simple R-C networks make efficient and inexpensive low-pass filters. The noise is converted to heat which is dissipated in the resistor. The fixed resistor does, however, produce thermal noise and, if used in the input leads of an instrumentation amplifier, can generate input-bias-current induced offset voltage. These issues affect the design of high-precision, low-noise stages.

In applications where signal and return conductors are not well-coupled magnetically, a common-mode choke can be used to increase their mutual inductance. A common-mode choke can be constructed by winding several turns of both conductors together through a high-permeability (> 2000) ferrite bead. The magnetic properties of the ferrite allow differential-mode currents to pass unimpeded while suppressing common-mode currents. Capacitors can be used before and after the choke to provide additional common-mode and differential-mode filtering, respectively. The common-mode choke is cheap and produces no thermal noise and no bias current-induced offsets. However, there is a field around the core. A metallic shield surrounding the core may be necessary to prevent coupling with other circuits. Also high-current levels should be avoided in the core as they may saturate the ferrite.

The third method for passive filtering takes the form of packaged π-networks (C-L-C). These packaged filters are completely self-contained and include feedthrough capacitors at the input and the output as well as a shield to prevent the inductor's magnetic field from radiating noise. These expensive networks offer high levels of attenuation and wide operating frequency ranges, but the filters must be selected so that for the operating current levels involved the ferrite does not saturate.

An example of shielding and filtering techniques against EMI is illustrated in Figure 1.34. In this circuit, an instrumentation amplifier is used to amplify low-level signals in the presence of high EMI. The entire circuit is enclosed in a rigid metallic shield made of copper. The layout emphasizes symmetry in the input circuit to maintain high CMR. Packaged EMI data-line and power-line filters are used to prevent EMI being carried by the conductors.

EXAMPLE DEMONSTRATING SHIELDING AND FILTERING TECHNIQUES

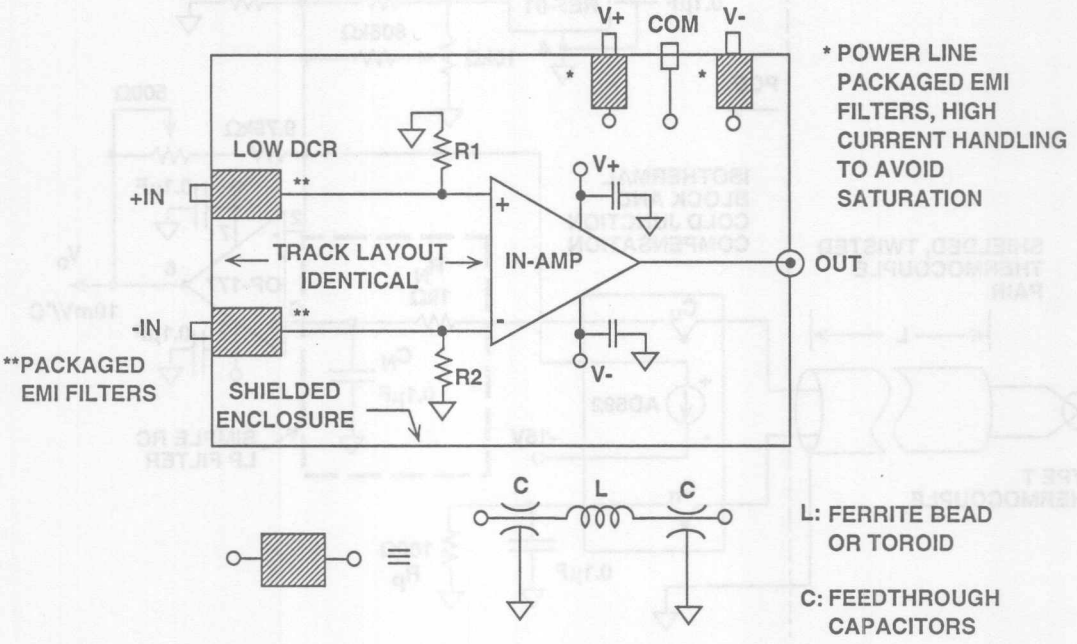


Figure 1.34

Application Circuits: EMI Reduction at Work

The circuits illustrated in Figures 1.35 through 1.39 demonstrate some of the principles outlined in this section. Each circuit use a different sensor to give the user some concrete ideas instead of theoretical remedies on how to handle interference.

The circuit illustrated in Figure 1.35 is designed to provide a 10 mV/°C output for a remotely-located Type T thermocouple. The accuracy of the circuit is ±0.4°C over a measurement temperature range of 0°C to 100°C. The circuit uses a grounded thermocouple to minimize noise pickup on long leads.

In the middle of the circuit is a low-pass filter, comprising R_N and C_N, whose function is to filter any noise along the thermocouple wires above 1.6kHz. The filter cutoff can be set lower by increasing C_N. (Although larger values for R_N might be used at the input of the OP-177, they would cause input bias-current induced offset and drift effects.) A resistor, R_P, is used in series with exposed thermocouples as protection in the event of contact with some high voltage. Otherwise, the thermocouple would be short circuited to ground and would certainly be destroyed. A capacitor connected across R_P serves to contain interference within the wires of the thermocouple cable.

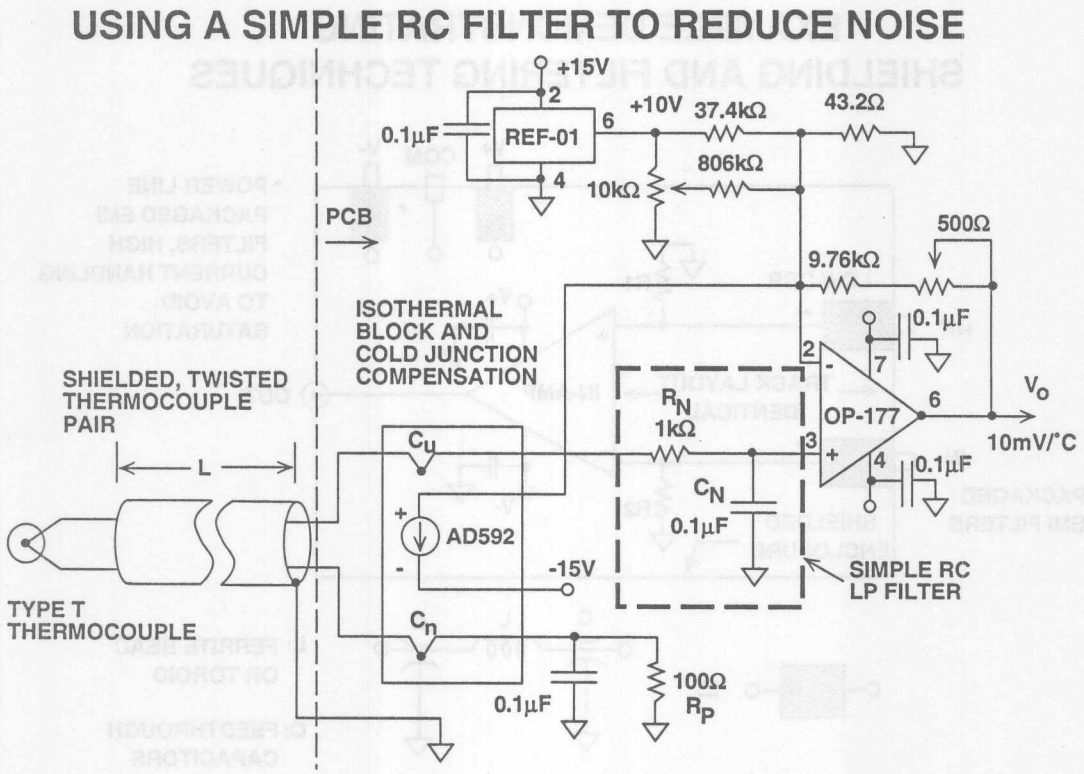


Figure 1.35

The circuit shown in Figure 1.36 (see Reference 8) illustrates a linearized thermistor in the feedback of an op amp to provide a 100mV/°C output over a temperature range of $0°C \leq T_A \leq 100°C$. Over temperature, the linearized thermistor network ranges from 2.7kΩ at 0°C to 1 kΩ at 100°C. A 1µF capacitor is connected across the thermistor network to form a low-pass filter with cutoff frequencies between 58Hz and 150Hz. (The cutoff frequency moves as the thermistor resistance changes over temperature.) Another technique to avoid EMI is to limit the signal bandwidth. In this circuit, C2 is used across R4 and P2 and sets a low-pass cutoff at 8.5 Hz.

Figure 1.37 shows a linearized RTD amplifier that is powered by a single +5V supply. The RTD is excited by a 100µA constant current which is regulated by A1. The 0.202V reference used to generate the constant current is provided by the REF-43 and resistors R4 and R5. The AMP-04 is scaled to give 10mV/°C output. When properly calibrated, the circuit achieves better than ±0.5°C accuracy within a temperature measurement range of 0°C to 400°C. Capacitor C3 performs two functions: it stabilizes the loop around A1 and provides a low-pass cutoff frequency of 800kHz. C1 works directly with the RTD and R3 to form a low-pass filter at 8kHz to prevent any noise from appearing at the inputs of the AMP-04.

USING CAPACITORS TO FILTER NOISE AND LIMIT BANDWIDTH

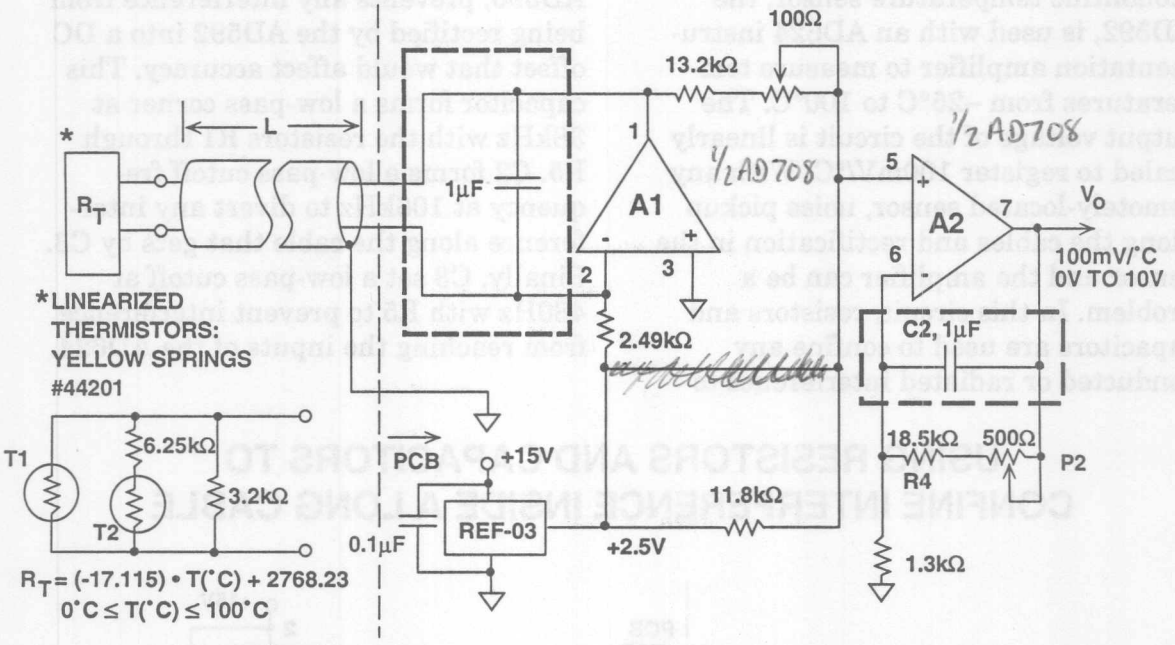


Figure 1.36

USING A CAPACITOR WITH AN RTD TO FILTER THE INSTRUMENTATION AMPLIFIER OUTPUT

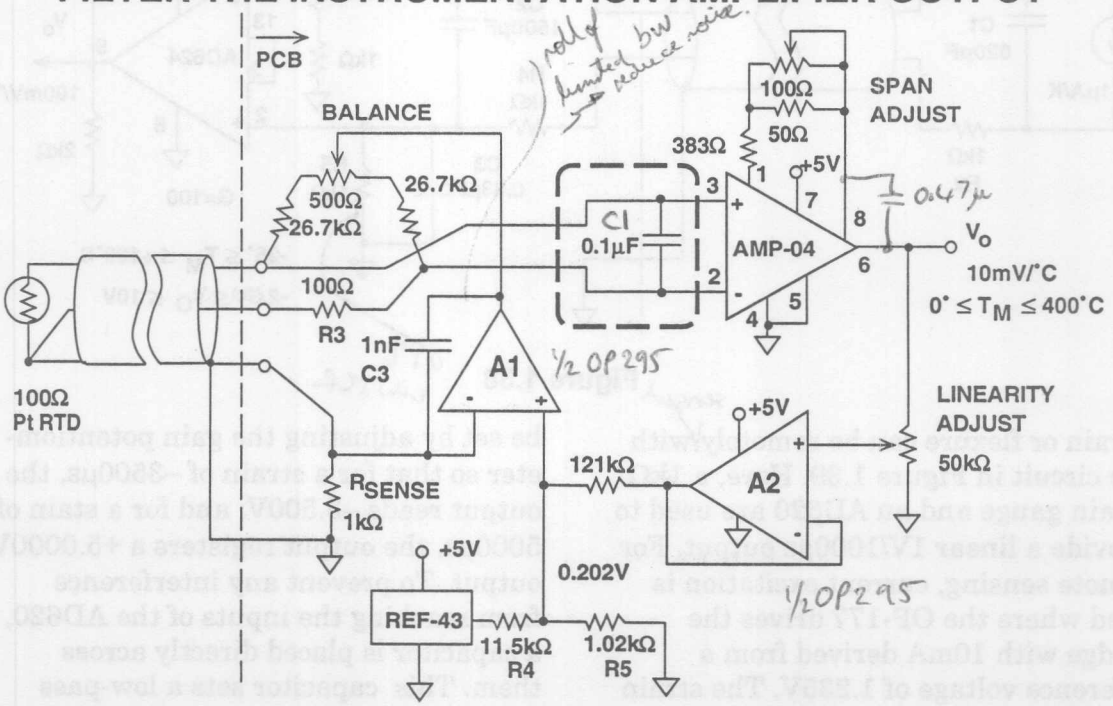


Figure 1.37

In the example illustrated in Figure 1.38 (Reference 9), a two-terminal, monolithic temperature sensor, the AD592, is used with an AD624 instrumentation amplifier to measure temperatures from –25°C to 100°C. The output voltage of the circuit is linearly scaled to register 100mV/°C. With any remotely-located sensor, noise pickup along the cables and rectification in the sensor and the amplifier can be a problem. In this circuit, resistors and capacitors are used to confine any conducted or radiated interference to the boundaries of the shielded cable. C1, which is connected across the AD590, prevents any interference from being rectified by the AD592 into a DC offset that would affect accuracy. This capacitor forms a low-pass corner at 38kHz with the resistors R1 through R5. C2 forms a low-pass cutoff frequency at 106kHz to divert any interference along the cable that gets by C3. Finally, C3 set a low-pass cutoff at 480Hz with R5 to prevent interference from reaching the inputs of the AD624.

USING RESISTORS AND CAPACITORS TO CONFINE INTERFERENCE INSIDE A LONG CABLE

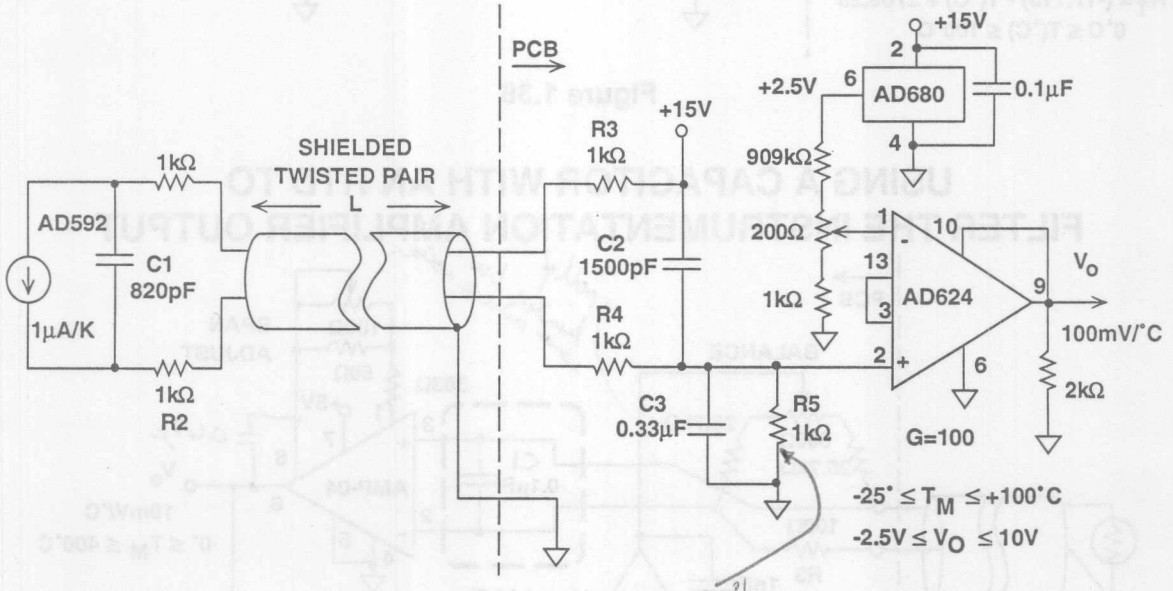


Figure 1.38

Strain or flexure can be remotely sensed with the circuit in Figure 1.39. Here, a 1kΩ strain gauge and an AD620 are used to provide a linear 1V/1000µε output. For remote sensing, current excitation is used where the OP-177 drives the bridge with 10mA derived from a reference voltage of 1.235V. The strain gauge has an output of 10.25mV per 1000µε. Full-scale strain voltage may be set by adjusting the gain potentiometer so that for a strain of –3500µε, the output reads –3.500V; and for a stain of 5000µε, the output registers a +5.0000V output. To prevent any interference from reaching the inputs of the AD620, a capacitor is placed directly across them. This capacitor sets a low-pass corner at 1.6kHz in conjunction with the strain gauge's resistance.

USING A CAPACITOR AND A STRAIN GAUGE'S RESISTANCE TO FILTER NOISE BEFORE AMPLIFICATION

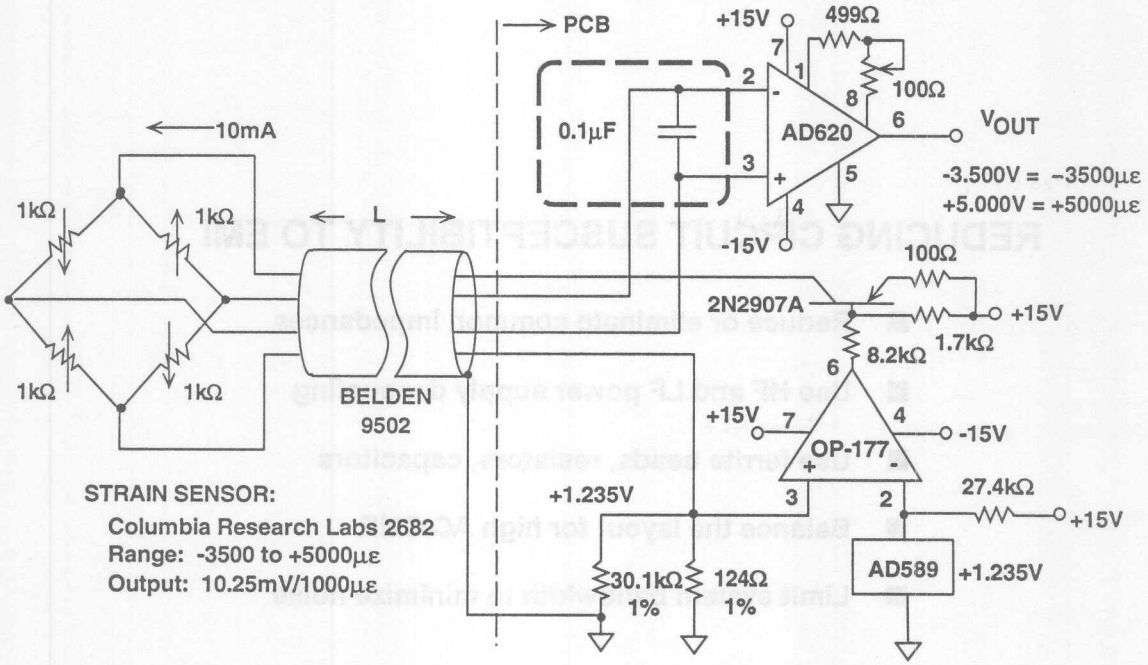


Figure 1.39

Reducing Susceptibility to EMI

The examples shown above and the techniques illustrated earlier in this section outline the procedures that can be used to reduce or eliminate electromagnetic interference. A summary of possible measures is given in Figures 1.40 and 1.41.

REDUCING SYSTEM SUSCEPTIBILITY TO EMI

- Always assume that interference exists!
- Use conducting enclosures against electric and HF magnetic fields
- Use mu-Metal/steel enclosures against LF magnetic fields
- Implement cable shields effectively
- Use feedthru capacitors and packaged pi-filters

Figure 1.40

REDUCING CIRCUIT SUSCEPTIBILITY TO EMI

- Reduce or eliminate common impedances
- Use HF and LF power supply decoupling
- Use ferrite beads, resistors, capacitors
- Balance the layout for high AC CMR
- Limit system bandwidth to minimize noise

Figure 1.41

Appendix: A Review of Shielding

A lump of metal between an interference source and a sensitive circuit will reduce interference. But why? More detailed (and more mathematical) discussions will be found in References 1 through 11, but this appendix is intended to highlight some basic principles for the engineer who is troubled by interference and thinks a screen might help.

We have seen in the main text that interference can be conducted into a sensitive circuit and that this effect can be minimized by appropriate filters. We have also seen that interference can be coupled by electric, magnetic and electro-magnetic fields. Shields attenuate these fields and may be considered as "field attenuators".

When the interference source is close to its victim ("near field" conditions) the field will be electric or magnetic, depending on circumstances, and when it is far away ("far field" conditions) it will be electro-magnetic ("far away" in these circumstances is usually defined as $\geq 0.16\lambda$ where λ is the wavelength of the interference, or $\geq c/2\pi f$, where f is the frequency of the interference and c is the velocity of light).

The characteristic impedance of free space (the far field case) is 377Ω and the field strength is proportional to the inverse square of the distance from its source. In the near field the interference source may produce a predominantly magnetic field, which is generally "low impedance" (this is not a rigorous definition but is sufficient to enable one to understand the action of conducting screens), or may produce an electric field, which is "high impedance". Both of these fields are "dipole fields" which

have the property of being proportional to the inverse *cube* of the distance from their source, so it is evident that simply increasing the separation between an interference source and its victim may avoid the necessity for a screen. This is a powerful argument against the trend to minimize the size of all electronic assemblies - a small increase in the size of a noise-critical PCB can often have a major beneficial effect on its overall noise performance.

The simplest attenuator consists of two impedances, Z1 and Z2, arranged as in Figure 1.42. The larger the ratio Z1:Z2, the greater the attenuation. A shield is an attenuator of this type: Z1 is the "source impedance" of the field and Z2 the impedance of the shield.

A SHIELD IS AN ATTENUATOR

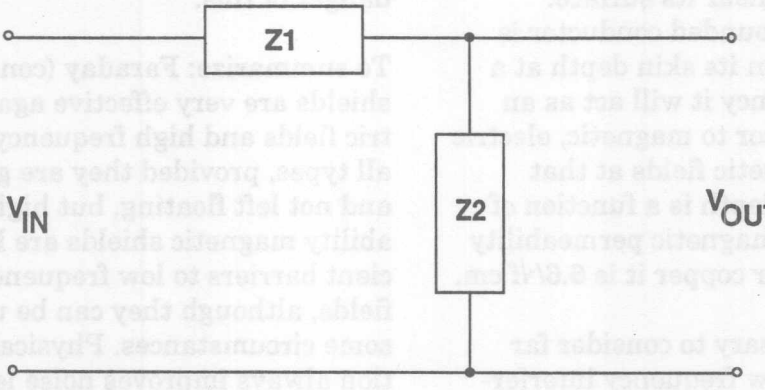


Figure 1.42

Where electric fields are involved the impedance of a shield consisting of a piece of grounded conductor (a "Faraday Shield" or a "Faraday Cage") is low, and the source impedance of the electric field is high. It follows that the attenuation, and hence the efficiency of shielding, is high in this case. Faraday shields are almost invariably very efficient at eliminating the interference effects due to electric fields - but they must be connected to ground or some other low impedance, or they will increase, rather than attenuate, the noise coupling. Failure to ground Faraday shields is one of the commonest engineering oversights leading to poor interference protection.

Magnetic fields have low "source impedance" and shields of high-permitivity magnetic material, such a mu-metal, have relatively large impedance to magnetic fields. Magnetic shields are

therefore much less efficient at suppressing low frequency magnetic field interference than Faraday shields are at limiting electric fields (most magnetic shields are conductors, however, and, if grounded, will act as very satisfactory Faraday shields, whatever their deficiencies as magnetic shields).

At high frequencies Faraday shields are quite effective at attenuating magnetic fields as well as electric fields. This is due to the "skin effect": a high frequency magnetic field induces eddy currents near the surface of a conductor which prevent it from penetrating to any great depth. HF currents in a conductor, accordingly, flow only in the thin "skin layer" near its surface. Therefore, if a grounded conductor is much thicker than its skin depth at a particular frequency it will act as an efficient attenuator to magnetic, electric and electro-magnetic fields at that frequency. Skin depth is a function of bulk resistivity, magnetic permeability and frequency: for copper it is $6.6/\sqrt{f}$ cm.

It is rarely necessary to consider far field effects for low frequency interference since we will rarely be concerned with sources more than a hundred meters away and at any frequency below 500 kHz a hundred meters is "near field"! The skin depth in copper for 500 kHz signals is about 0.1 mm (0.004") so a copper can with a wall more than 0.25 mm thick will be quite an efficient shield at this frequency.

Electromagnetic-radiation can enter a shield through any hole larger than about 0.1λ, so at very high frequencies hole sizes must be considered. At any frequency a conductor entering a shielded volume can admit interference if it is not grounded to the shield, so filters must be used where there is any danger of this.

To summarize: Faraday (conductive) shields are very effective against electric fields and high frequency fields of all types, provided they are grounded and not left floating, but high permeability magnetic shields are less efficient barriers to low frequency magnetic fields, although they can be useful in some circumstances. Physical separation always improves noise isolation.

INPUT-STAGE RFI RECTIFICATION SENSITIVITY

A well-known, but poorly understood phenomenon in analog integrated circuits is RF rectification, specifically in instrumentation amplifiers and operational amplifiers. While amplifying very small signals these devices can rectify unwanted high frequency signals. The result is dc errors which appear at the output in addition to the wanted sensor signal. Unwanted out-of-band signals enter sensitive circuits through the circuit's conductors. These conductors, which lead into and out of the circuit, provide a direct path for interference to couple into a circuit. These conductors pick up noise through capacitive, inductive, or radiation coupling as discussed elsewhere. Regardless of the type of interference, the unwanted signal is a voltage which appears in series with the inputs. How devices rectify signals and methods for preventing RFI rectification will be discussed in this section.

All instrumentation and operational amplifier input stages comprise emitter-coupled (BJT) or source-coupled (FET) differential pairs with resistive or current-source loading. Depending on the quiescent current level in the devices and the frequency of the interference, these differential pairs can behave as high-frequency detectors. As will be shown, this detection process produces spectral components at the harmonics of the interference as well at dc! It is the dc component that shifts the bias levels of to produce errors, which can lead to system inaccuracies.

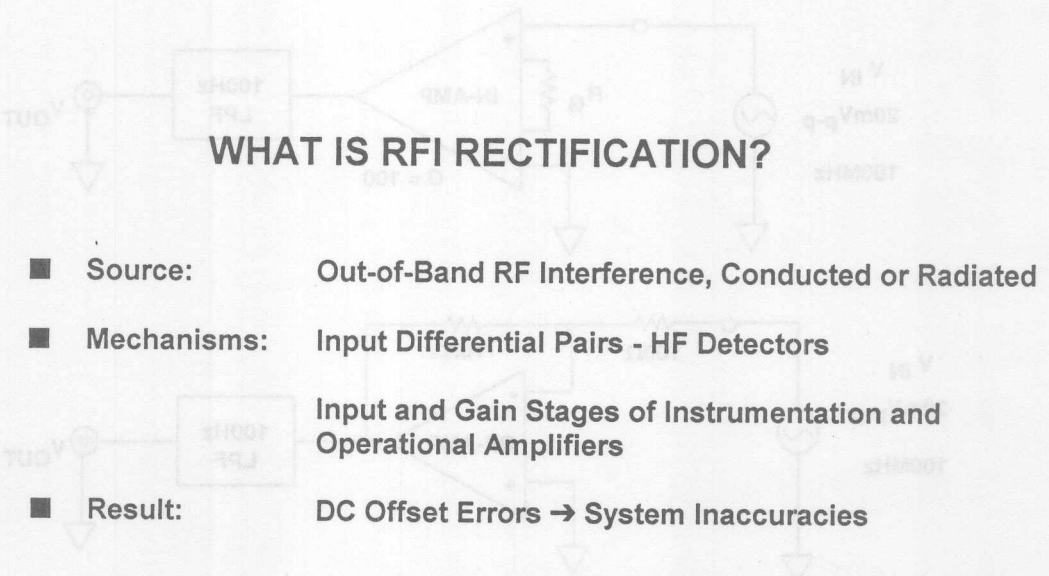


Figure 1.43

The effect of rectification on instrumentation and operational amplifiers may be evaluated with the circuits in Figure 1.44. Amplifiers are configured for a gain of 100, and the outputs connected to a 100-Hz low-pass filter to prevent other unwanted signals from interfering with the measurement. A $20mV_{p-p}$ signal at 100MHz is the stimulus and was chosen to be well above the frequency limits of the circuits under test. Outputs are monitored with a 300MHz oscilloscope and measurements made with a digital voltmeter. Five instrumentation amplifiers, and 17 single and 12 dual operational amplifiers have been tested. Devices of both bipolar and FET technologies were evaluated to determine any patterns in RFI rectification.

Based on the data which is summarized in Figures 1.46, 1.47, and 1.48, two patterns appeared. First, device susceptibility to rectification appears to be inversely proportional to supply current; that is, devices biased at low quiescent supply currents exhibited the largest amount of output voltage shift. Second, ICs with JFET-input differential pairs appeared to be less susceptible to rectification than BJT input stages.

RFI RECTIFICATION TEST CONFIGURATION

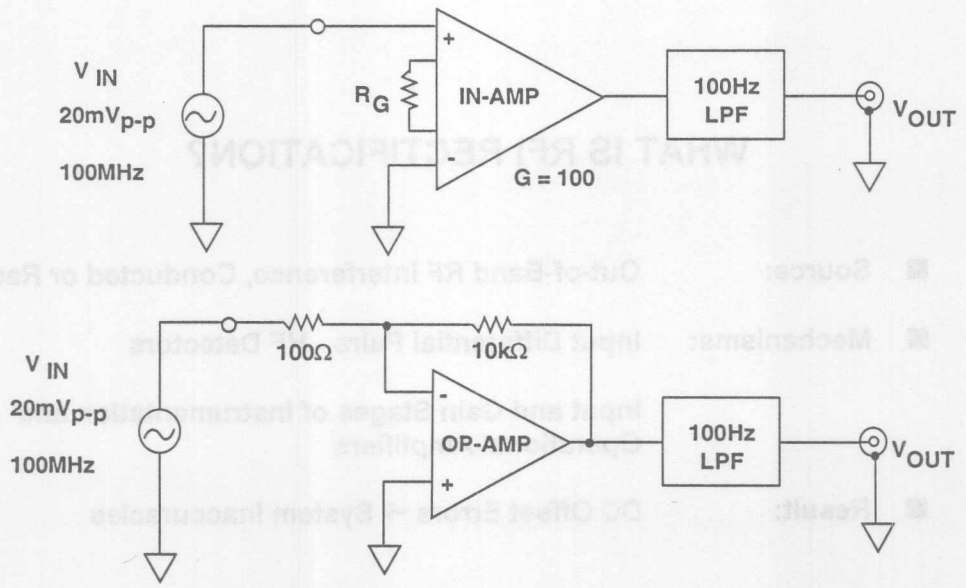


Figure 1.44

OBSERVATIONS

- Correlation: Rectification sensitivity to supply current
- JFET-Input Devices: Lower sensitivity to rectification

Figure 1.45

INSTRUMENTATION AMPLIFIERS

DEVICE	I_{SY}	ΔV_O
AMP-04	0.9mA	22mV
AD620	1.3mA	6mV
AMP-02	5mA	0.65mV
AD625	5mA	21.5mV
AMP-01	5mA	0.5mV

Figure 1.46

In Figure 1.46, all five instrumentation amplifiers use BJTs in their input stages. The AMP-04, biased at 900μA quiescent supply current, exhibited the largest output voltage shift of the group. The AMP-01, biased at a quiescent supply current of 5 mA, exhibited the least amount of error. The AD625, although biased at a supply current of 5mA, exhibited a larger output shift when compared to the AMP-01. One possible explanation for this large discrepancy could be that super-β transistors (used in the input stage of the AMP-01) exhibit a lower susceptibility to rectification than standard-process BJTs.

The results for single operational amplifiers are summarized in Figure 1.47. A clear pattern in the data is that FET-input operational amplifiers consistently exhibit a lower susceptibility than BJT-input operational amplifiers. Some FET-input devices, such as the OP-80, the OP-42, and the AD845, exhibited no observable shift in their output voltages. Of the bipolar-input operational amplifiers, the amount of output shift decreased with increasing supply current. Of this group, only the AD797 showed no observable output voltage shift.

Results of the dual operational amplifiers are illustrated in Figure 1.48. Again, the pattern is repeated in that the FET-input devices exhibited little or no observable shift in their output voltages, regardless of quiescent supply current. The OP-200 and OP-297 both exhibited very little output voltage shift. This may be due to their use of in super-β transistors *and* input bias current cancellation.

OPERATIONAL AMPLIFIERS -- SINGLES

DEVICE	I_{SY}	ΔV_O
OP-90	0.03mA	4mV
OP-20	0.095mA	58mV
OP-80 (CMOS)	0.33mA	N/C
AD705 (Super-β)	0.6mA	10mV
OP-97 (Super-β)	0.6mA	13mV
AD795	1.5mA	2mV
OP-177	2mA	2.5mV
AD707	3mA	2mV

DEVICE	I_{SY}	ΔV_O
AD711 (FET)	3.4mA	0.6mV
AD645 (FET)	3.5mA	0.3mV
AD744 (FET)	5mA	0.5mV
OP-27	6mA	2mV
OP-42 (FET)	6.5mA	N/C
AD829	7mA	3mV
AD797	9.5mA	N/C
AD743 (FET)	10mA	0.1mV
AD845 (FET)	12mA	N/C

N/C = No Change

Figure 1.47

OPERATIONAL AMPLIFIERS -- DUALS

DEVICE	I_{SY}	ΔV_O
OP-290	0.02mA	4mV
OP-295	0.175mA	3mV
OP-282 (FET)	0.25mA	1mV
OP-297 (Super-β)	0.63mA	0.14mV
OP-200 (Super-β)	0.73mA	0.19mV
OP-213	2mA	6mV
OP-275	2.5mA	6mV
AD708	2.8mA	2mV
AD712 (FET)	3.4mA	0.3mV
OP-249 (FET)	3.5mA	N/C
AD746 (FET)	5mA	0.3mV
AD827	7mA	N/C

N/C = No Change

Figure 1.48

Based on these data and from the fundamental differences between BJTs and FETs, we can summarize what we know. Bipolar transistor action is controlled by a forward-biased p-n junction (the base-emitter junction) whose I-V characteristic is exponential and quite nonlinear. FET behavior, on the other hand, is controlled by voltages applied to a reverse-biased p-n junction diode (the gate-source junction). The I-V characteristic of FETs is a square-law, and, thus more linear than that of BJTs.

In the case of low current devices, transistors in the circuit are biased below their peak f_T collector currents. Although the devices are constructed on processes whose device f_Ts can operate at hundreds of MHz, charge transit times through the devices increase at low quiescent collector currents. RF rectification in these devices is also exacerbated by the impedance levels used. In low-power operational amplifiers, impedance levels are on the order of hundreds to thousands of kΩs whereas in moderate supply-current designs the impedance levels might be no more than a few kΩ. These factors combine to affect a device's sensitivity to RF rectification.

OBSERVATIONS

- Devices with bipolar input transistors do rectify
  - Forward-Biased Base-Emitter Junctions
  - Exponential I-V Transfer Characteristic
- Devices with FET input transistors are less sensitive
  - Reverse-Biased p-n Junctions
  - Square Law I-V Transfer Characteristic
- Low I_{sy} Devices versus High I_{sy} Devices
  - Low I_{sy} → Higher Sensitivity
  - Low I_C (Q1, Q2) → Longer Transit Times
  - Low I_{sy} → Higher Internal Z Levels

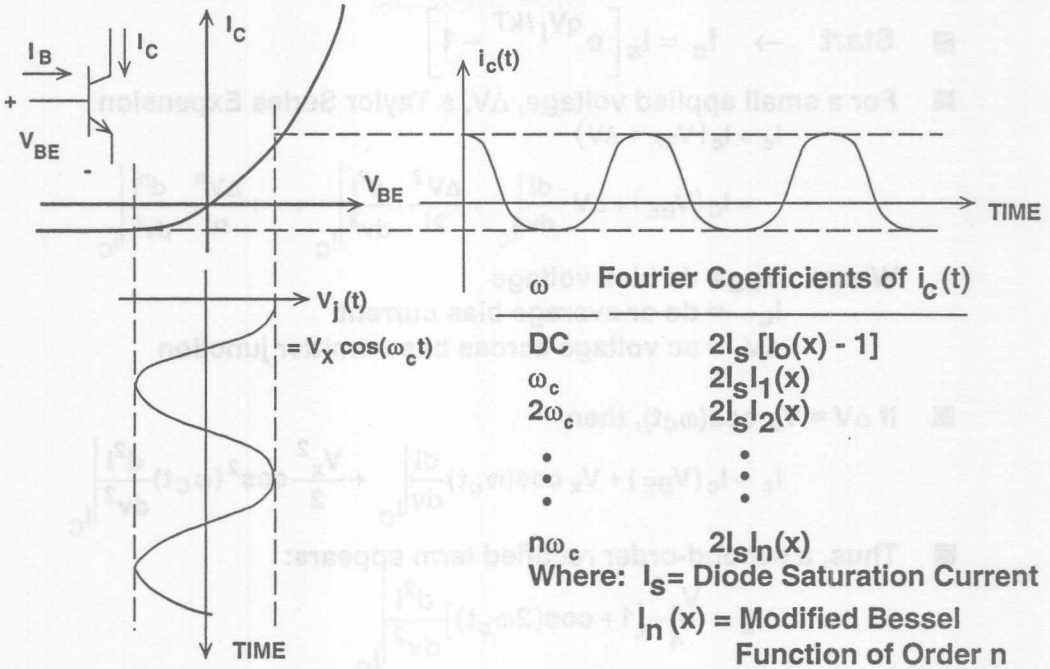
Figure 1.49

RFI Rectification: An Analytical Approach

These experiments have demonstrated that BJT-input devices exhibit a greater amount of output voltage shift on exposure to RFI than devices with FET inputs. In this section, an analytical approach will be taken to explain the phenomenon.

RF circuit designers have long known that p-n junction diodes are extremely efficient rectifiers because of their nonlinear I-V characteristics. Figure 1.50 illustrates the base-emitter junction diode I-V characteristic of an NPN bipolar transistor whose collector current, $i_c(t)$, as a function of the applied voltage, $V_j(t)$, is superimposed. The spectral components of the Fourier analysis of the current output for an HF sinewave input reveals that, as the device is biased closer to its "knee," device nonlinearity increases. This, in turn, makes the detection process more efficient. This is especially true in low-power operational amplifiers where the transistor is biased at very low collector currents.

HF MODULATION OF THE BASE-EMITTER JUNCTION CAUSES RECTIFICATION



ω	Fourier Coefficients of $i_c(t)$
DC	$2I_S [I_0(x) - 1]$
ω_c	$2I_S I_1(x)$
$2\omega_c$	$2I_S I_2(x)$
•	•
•	•
•	•
$n\omega_c$	$2I_S I_n(x)$

Where: I_S = Diode Saturation Current

$I_n(x)$ = Modified Bessel Function of Order n

$x = V_X/V_T$

Figure 1.50

Rectification analysis of an NPN transistor's collector current is shown in Figure 1.51. The analysis begins with the transistor's I_C–V_{BE} characteristic equation. If a small voltage, given by $\Delta V = V_X \cos(\omega_c t)$, is applied to the device, then a Taylor series expansion of the collector current around the operating point (I_C @ V_{BE}) produces three dominant spectral components (terms above the second order are neglected). These spectral components are the quiescent collector current, I_C, a linear term at the input frequency, $\cos(\omega_c t)$, and a quadratic term at the input frequency, $\cos^2(\omega_c t)$. The linear spectral component is either filtered (hopefully) or rectified by other gain stages within the device. It is the quadratic term that contains the primary rectified information.

RECTIFICATION ANALYSIS CONTINUED

- Start $\rightarrow$ $i_c = I_s\left[e^{qV_j/kT} - 1\right]$
- For a small applied voltage, ΔV, a Taylor Series Expansion

$$i_c = i_c(V_{BE} + \Delta V)$$

$$= I_C(V_{BE}) + \Delta V \cdot \frac{di}{dv}\bigg|_{I_C} + \frac{\Delta V^2}{2!} \cdot \frac{d^2i}{dv^2}\bigg|_{I_C} + \cdots + \frac{\Delta V^n}{n!} \cdot \frac{d^ni}{dv^n}\bigg|_{I_C}$$

Where V_{BE} = dc bias voltage
I_C = dc or average bias current
ΔV = ac voltage across base-emitter junction

- If $\Delta V = V_X \cos(\omega_C t)$, then

$$i_c = I_c(V_{BE}) + V_x \cos(\omega_c t)\frac{di}{dv}\bigg|_{I_C} + \frac{V_x^2}{2}\cos^2(\omega_C t)\frac{d^2i}{dv^2}\bigg|_{I_C}$$

- Thus, a second-order rectified term appears:

$$\Delta i_c = \frac{V_x^2}{4}\left[1 + \cos(2\omega_c t)\right]\frac{d^2i}{dv^2}\bigg|_{I_C}$$

Figure 1.51

The second-order term can be simplified by using the following trigonometric identity:

$$\cos^2(\omega_c t) = \frac{1}{2}\left[1 + \cos(2\omega_c t)\right] \qquad \text{Eq. 1.1}$$

Substituting the right-hand side of Eq. 1.1 into the expression for the second-order term yields:

$$\Delta i_c = \frac{V_x^2}{4}\left[1 + \cos(2\omega_c t)\right]\frac{d^2i}{dv^2}\bigg|_{I_C} \qquad \text{Eq. 1.2}$$

Eq. 1.2 reveals that the original quadratic second-order term can be simplified into a frequency-dependent term, Δi_c(AC), at twice the input frequency and a dc term, Δi_c(DC), as shown in Figure 1.52. The dc term can be further simplified by evaluating the second derivative of the collector current with respect to the base-emitter voltage at the quiescent collector current. The result of this operation yields the final form for the rectified DC term:

$$\Delta i_C(DC) = \left(\frac{V_X}{V_T}\right)^2 \cdot \frac{I_C}{4} \qquad \text{Eq. 1.3}$$

THE CHANGE IN A BJT's COLLECTOR CURRENT HAS TWO COMPONENTS

- AC Component @ $2\omega_C$:

$$\Delta I_c(AC) = \frac{V_x^2}{4}\cos(2\omega_c t)\left.\frac{d^2i}{dv^2}\right|_{I_C}$$

- DC Component:

$$\Delta I_c(DC) = \frac{V_x^2}{4}\cdot\left.\frac{d^2i}{dv^2}\right|_{I_C}$$

$$= \frac{V_X^2}{4}\cdot\frac{I_S \exp[V_{BE}/V_T]}{V_T^2}$$

$$\Delta i_C(DC) = \left(\frac{V_X}{V_T}\right)^2\cdot\frac{I_C}{4}$$

- DC Component is Operating Point Dependent!

Figure 1.52

The result in Eq. 1.3 shows that the dc component of the second-order term is directly proportional to the square of the noise amplitude of the HF noise and, more importantly, to the quiescent collector current of the transistor. To illustrate the effect of transistor operating point on rectification, Figure 1.53 shows the change in the dc collector current of an NPN transistor when a $20mV_{p\text{-}p}$, high-frequency signal impinges upon it.

RFI RECTIFICATION VERSUS BJT OPERATING POINT $T_A = 25°C$

Quiescent Collector Current, I_C	Rectified Collector Current, Δi_C
1 µA	38 nA
10 µA	380 nA
100 µA	3.8 µA
1 mA	38 µA

Figure 1.53

To reduce the amount of rectified collector current is therefore a matter of reducing the quiescent current or the magnitude of the interference. Since the input stages of instrumentation and operational amplifiers do not often provide access for adjusting quiescent collector currents, reducing the level of noise is the best policy. For example, reducing the amplitude of the interference by 50% produces a 75% reduction in the rectified collector current.

A similar approach can be used for the rectification analysis of a FET's drain current as a function of a small HF voltage applied to its gate. The results of evaluating the second-order rectified term for the FET's drain current are summarized in Figure 1.54. Like the BJT, the FET's second-order term has an ac and a dc component. The simplified expression for the dc term of the rectified drain current is given in Eq. 1.4, where the rectified dc drain current is directly proportional to the square of the amplitude of the offending signal. However, Eq. 1.4 reveals an important difference between the amount of rectification produced by BJTs and FETs. Whereas in a BJT the change in collector current has a direct relationship to its quiescent collector current level, the change in a FET's drain current is proportional to its drain current at zero gate-source voltage, I_{DSS}, and inversely proportional to the square of its channel pinch-off voltage, V_P — parameters that are geometry- and process-dependent. Typically, FETs used in the input stages of instrumentation and operational amplifiers are biased such that their quiescent drain current is approximately $0.5 \bullet I_{DSS}$. Therefore, the change in a FET's drain current is independent of its quiescent drain current; hence, independent of the operating point.

$$\Delta i_D(DC) = \left(\frac{Vx}{Vp}\right)^2 \bullet \frac{I_{DSS}}{2} \qquad \text{Eq. 1.4}$$

A quantitative comparison of second-order rectified dc terms between BJTs and FETs is illustrated in Figure 1.55. In this example, a bipolar transistor with a unit emitter area of $576\mu m^2$ is compared to a unit-area JFET designed for an I_{DSS} of $20\mu A$ and a channel pinch-off voltage of 2V. Each device is biased at $10\mu A$ and operated at $T_A = 25°C$. Using these parameters, Eq. 1.3 and Eq. 1.4 yield the result that, under identical quiescent current levels, the change in collector current in bipolar transistors is ≈1500 times greater than the change in a JFET's drain current.

Although the rectified dc term for BJTs and FETs is directly proportional to either the BJT's quiescent collector current or the FET's I_{DSS}, no access to the internal circuitry is provided to adjust the operating point of the differential pair at the input of IC op amps and instrumentation amplifiers. However, the analysis showed that, regardless of the amplifier type used, RFI rectification is directly proportional to the *square of the magnitude* of the applied interference. Therefore, to minimize rectification the interference should be reduced or eliminated. The most direct way to reduce or eliminate unwanted noise is through filtering.

ANALYSIS FOR JFETs YIELDS SIMILAR RESULTS

- Start $\rightarrow i_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$
- $\Delta i_D(AC) = \frac{V_X^2}{4}\cos(2\omega_C t)\left.\frac{d^2 i_D}{dV_{GS}^2}\right|_{I_D}$
- $\Delta i_D(DC) = \frac{V_X^2}{4}\cdot\left.\frac{d^2 i_D}{dV_{GS}^2}\right|_{I_D} = \frac{V_X^2}{4}\cdot\frac{2I_{DSS}}{V_P^2}$
- $\Delta i_D(DC) = \left(\frac{V_X}{V_P}\right)^2\cdot\frac{I_{DSS}}{2}$
- Rectified Term Dependent upon I_{DSS} and V_p, not Operating Point

Figure 1.54

COMPARISON: Δi_C (BJT) VERSUS Δi_D (FET)

- Bipolar Transistor:

  Emitter Area = 576 μm^2

  I_C = 10 µA

  V_T = 25.68mV @ 25°C

  $\Delta i_C = \left(\frac{V_X}{V_T}\right)^2\cdot\frac{I_C}{4}$

  $= \frac{V_X^2}{264}$

- JFET

  I_{DSS} = 20 µA (Z/ L = 1)

  V_P = 2V

  I_D = 10 µA

  $\Delta i_D = \left(\frac{V_X}{V_P}\right)^2\cdot\frac{I_{DSS}}{2}$

  $= \frac{V_X^2}{400\times10^3}$

- BJTs are about 1500 times more sensitive than JFETs

Figure 1.55

Reducing RFI Rectification in Operational Amplifiers

Figure 1.56 shows low-pass filters used to reduce or eliminate unwanted interference. For the inverting circuit configuration on the left, the input resistor was split into two equal halves with the common point bypassed to ground by C1. The input resistor should be split into equal halves to prevent large values of C1 from appearing directly across the operational amplifier's input terminals. High capacitance at the input of some operational amplifiers can lead to loop instability. This is especially true for high-speed amplifiers. In general, the input filter's cutoff frequency should be no greater than 100 times the signal bandwidth to ensure that the circuit responds quickly enough to a step change in the input signal. For non-inverting amplifier configurations, the R1-C1 combination form the input filter that prevents noise from coupling directly into the amplifier's noninverting input. C2 limits the bandwidth (and hence wideband noise) of an amplifier but does not greatly assist in preventing rectification since it is unlikely to affect RF levels in the input stage.

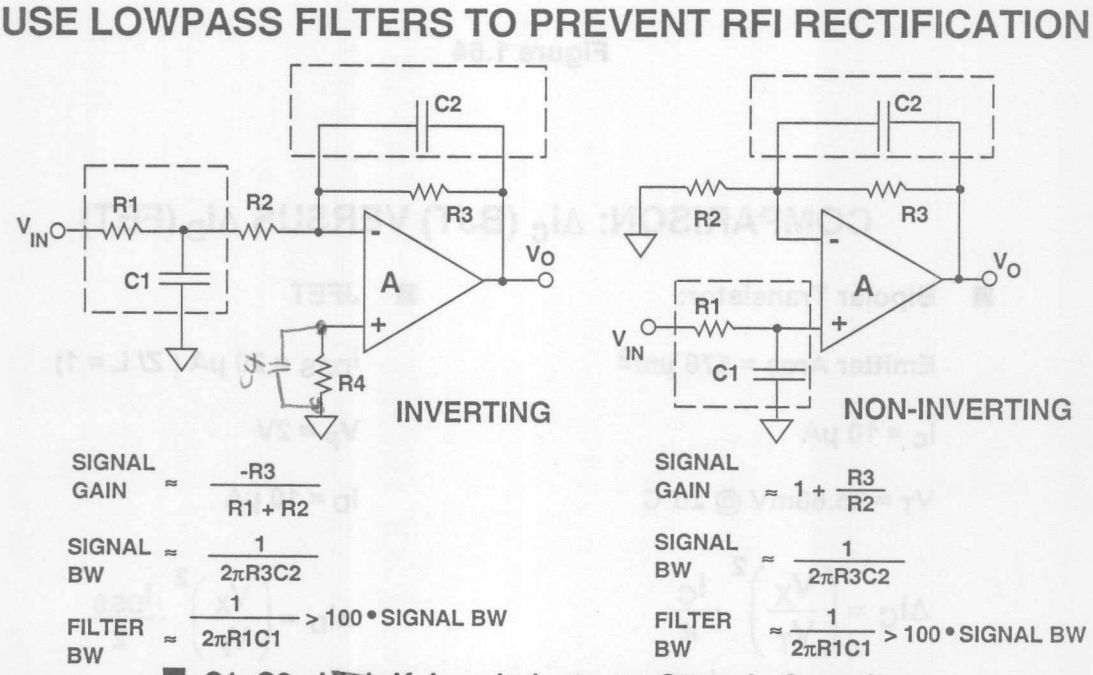


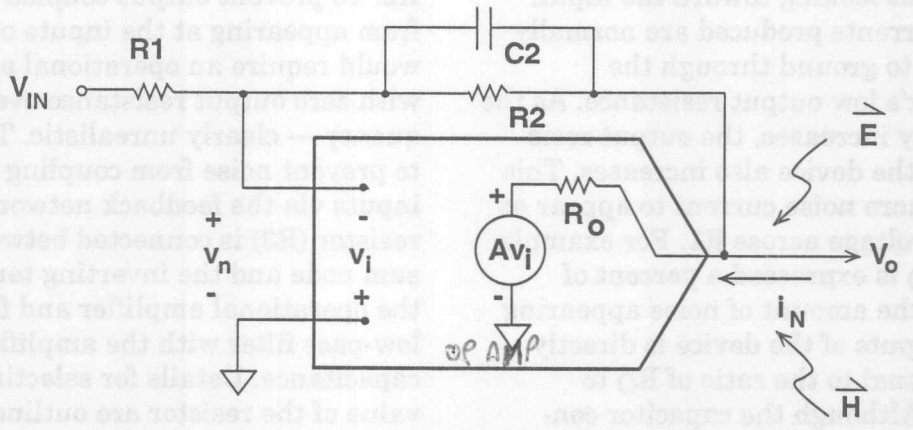
Figure 1.56

Equations illustrating the relationship between circuit element values and filter cutoff frequencies are given in Figure 1.56. Proper component selection is as important as the technique itself for successful noise filtering. Metal-film resistors should be chosen over composition or wire-wound ones for their low excess noise and low parasitic reactances. For best high-frequency noise filtering, low inductance NPO, COG, or film capacitors should be used.

Filtering operational amplifier inputs and limiting circuit bandwidths are both good techniques for eliminating noise. However, noise can also couple into an amplifier's input stages via its output (Figure 1.57). This is especially important in low-power circuits where operational amplifier output resistance and external circuit resistance levels are large.

The output resistance of operational amplifiers increases with frequency; thus it exhibits inductive behavior. If an amplifier has a low output impedance, external noise which finds its way to the output terminal is effectively grounded harmlessly. But if the output impedance rises with frequency then HF noise at the output is not attenuated so much and may couple to the amplifier input by passing backwards through the feedback network (Figure 1.58).

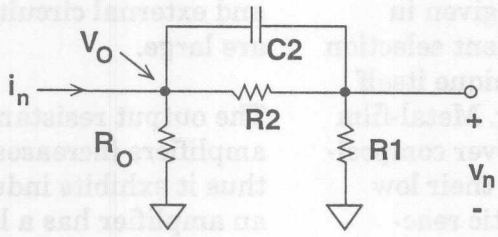
OP AMP OUTPUT IMPEDANCE ALSO AFFECTS RECTIFICATION SENSITIVITY



- Op Amp Output Impedance Increases With Frequency
- Larger R_o Produces More v_n at Op Amp Input

Figure 1.57

EQUIVALENT CIRCUIT OF OP AMP FEEDBACK NETWORK



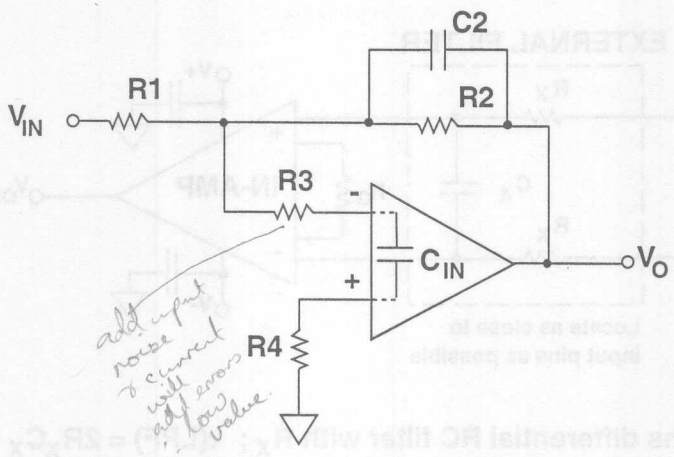
OP AMP R_O (% OF R1 + R2)	NOISE CURRENT IN R1 (% OF i_n)
0	0
0.1	0.09
1	0.9
10	9

■ C2 INCREASES NOISE BY SHUNTING R2 @ HF

Figure 1.58

Here the feedback network is viewed from the source of the interference at the output looking toward the input. Noise currents produced are normally shunted to ground through the amplifier's low output resistance. As the frequency increases, the output resistance of the device also increases. This causes more noise current to appear as a noise voltage across R1. For example, when R_O is expressed a percent of R1+R2, the amount of noise appearing at the inputs of the device is directly proportional to the ratio of R_O to R1+R2. Although the capacitor connected across the feedback resistor is used to limit signal bandwidth, it unfortunately provides a direct path for noise at high frequencies by shunting R2. To prevent output-coupled noise from appearing at the inputs of a device would require an operational amplifier with zero output resistance over frequency — clearly unrealistic. Therefore, to prevent noise from coupling into the inputs via the feedback network, a resistor (R3) is connected between the sum node and the inverting terminal of the operational amplifier and forms a low-pass filter with the amplifier's input capacitance. Details for selecting the value of the resistor are outlined in Figure 1.59.

CURING OUTPUT CIRCUIT INDUCED RECTIFICATION



- R3 Forms LPF with C_{IN} ($3pF \leq C_{IN} \leq 5pF$)
- Choose $1k\Omega \leq R3 \leq 10k\Omega$
- Set $R4 = R3 + R1 \| R2$
- Watch for e_n (R3)

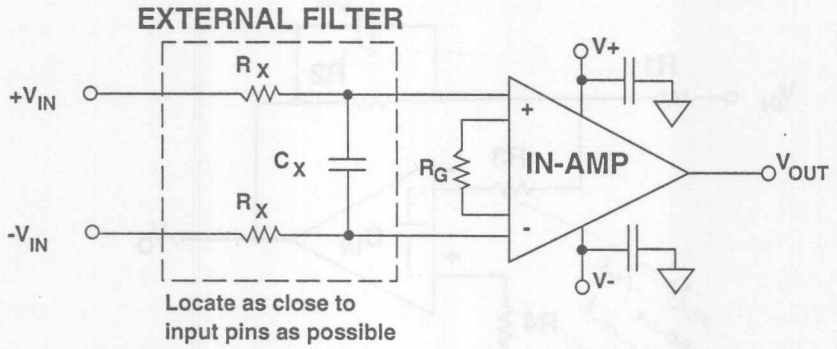
Figure 1.59

Reducing RFI Rectification in Instrumentation Amplifier Circuits

Filtering techniques used for operational amplifier circuits can also be applied to instrumentation amplifier circuits. As shown in Figure 1.60, low-pass filters are used in series with the differential inputs to prevent unwanted noise from reaching the inputs. Here, a capacitor, C_X, is connected across the inputs of the instrumentation amplifier and forms a differential low-pass filter with the two resistors R_X. An additional benefit of using a differentially-connected capacitor is that it reduces common-mode capacitance imbalance which helps to preserve high-frequency AC common-mode rejection. Since series resistors are required to form the low-pass filter, errors due to poor layout (CMR imbalance), component tolerance of R_X (input bias current-induced V_{OS}) and resistor thermal noise must be considered in the design process. In applications where the sensor is an RTD or a resistive strain gauge, R_X can be omitted, provided the sensor is close to the amplifier.

Some instrumentation amplifiers provide access to the base and emitter junctions of the input transistors (Figure 1.61). An external capacitor (C_X) can be connected across these terminals to reduce RFI rectification. This base-emitter bypass capacitor shunts high-frequency interference away from the base-emitter junction by forming a low-pass filter with an external resistance, R_X; however, a drawback to this technique is that the loop response of the amplifier input circuit is affected by the filter capacitor. As in the previous example, errors arising from the addition of a series resistance must be evaluated.

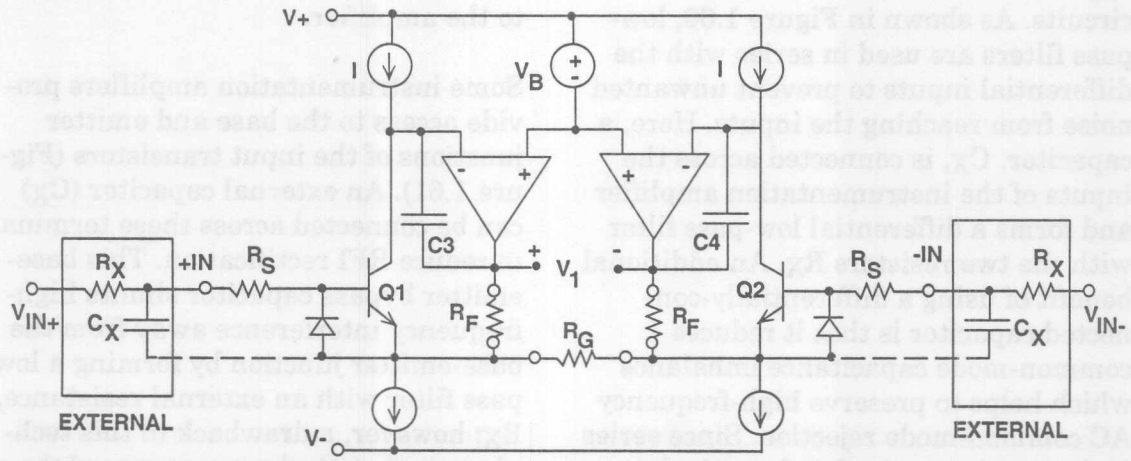
USE THE SAME TECHNIQUE FOR INSTRUMENTATION AMPS



- C_X forms differential RC filter with R_X; $\tau(LPF) = 2R_XC_X$
- C_X reduces common-mode capacitance imbalance $\rightarrow$ AC CMRR
- Evaluate R_X errors -- CMR, $I_b \Delta R_X$, $e_n(R_X)$
- R_X may be omitted if transducer is resistive and close to the amplifier

Figure 1.60

METHOD 2: BYPASS Q1 AND Q2 BASE-EMITTER JUNCTIONS WITH A CAPACITOR



- Must have access to the amplifier's base-emitter junctions
- C_X shunts interference away from base-emitter junctions
- C_X affects the amplifier's transient response
- Evaluate R_X errors

Figure 1.61

Since these capacitors can affect the loop stability of the input stage, they cannot be arbitrarily large. In fact, each instrumentation amplifier requires a specific value of capacitance depending on the gain setting. Exceeding the recommended capacitance value will damage the loop response. Figure 1.62 is a guide to selecting the recommended value of capacitance for each ADI instrumentation amplifier that provides direct access to the base and emitter terminals. Some, such as the AD625 and the AMP-01, require different values of capacitance for different gain settings. On the other hand, the AD626 does not require external R-C networks for noise filtering. At each input of the AD626, an internal 200kΩ resistor forms a 160kHz low-pass filter with an internal 5pF capacitor. The AD626 also provides access to an internal node for connecting a external capacitor for additional filtering.

DIFFERENT INSTRUMENTATION AMPLIFIERS REQUIRE DIFFERENT BASE-EMITTER BYPASSING

DEVICE	C_X	CONNECT C_X BETWEEN
AD524 AD624	<220pF	+IN and RG2 –IN and RG1
AD625	220pF (G<10) 680pF (G>10)	+IN and +GS –IN and –GS
AMP-01	220pF (G<10) 680pF (G>10)	+IN and pin 1 –IN and pin 2
AD620	<100pF (G>10)	+IN and pin 8 –IN and pin 1
AD626	RFI Filter Built-In	

Figure 1.62

Unfortunately not all instrumentation amplifiers are created equal. In Figure 1.63 are devices that do not provide direct access to the input transistors. Therefore, the base-emitter bypass technique cannot be used, and external networks for noise filtering must be considered. Before you use the base-emitter capacitance bypass technique do understand the topology of the amplifier.

NOT ALL INSTRUMENTATION AMPLIFIERS ARE EQUAL

- **Do not use base-emitter bypass on the following devices:**

  - **AMP-02**
  - **AD365**
  - **AMP-03**
  - **AD521**
  - **AD522**
  - **AMP-04**
  - **AMP-05**

Figure 1.63

Preventing RFI rectification in high-accuracy circuits requires an understanding of the electrical environment in which the circuit operates and using passive components (resistors, capacitors, ferrite beads) wisely. Passive components that exhibit low parasitic reactances should always be used.

Always consider the impact of external filtering networks (input or output) on the overall performance. Finally, whatever methods are used to reduce RFI rectification, preserve high AC common-mode rejection by using balanced layout to maintain input symmetry.

PREVENTING RFI RECTIFICATION IN HIGH ACCURACY CIRCUITS

- Know your environment
- Use your arsenal in filtering:
  - Metal film resistors
  - Ferrite beads
  - Low-inductance ceramic capacitors
- Consider the effects of external filtering
- Balance input layout for high AC CMR

Figure 1.64

INPUT OVERVOLTAGE PROTECTION

Op amps and instrumentation amplifiers must often have the interface to the outside world, which may entail handling voltages that exceed their absolute maximum ratings. Sensors are often placed in an environment where a fault may connect the sensor to high voltages: if the sensor is connected to an amplifier, the amplifier inputs may see voltages exceeding its power supplies. Whenever its input voltage goes outside its supply range, an op amp may be damaged, even when they are turned off. Almost all op amps' input absolute maximum ratings limit the maximum allowable input voltage to the positive and negative supplies or possibly 0.3V outside these supplies. A few exceptions to this rule do exist, which can be identified from individual data sheets, but the vast majority of amplifiers require input protection if over-voltage can possibly occur.

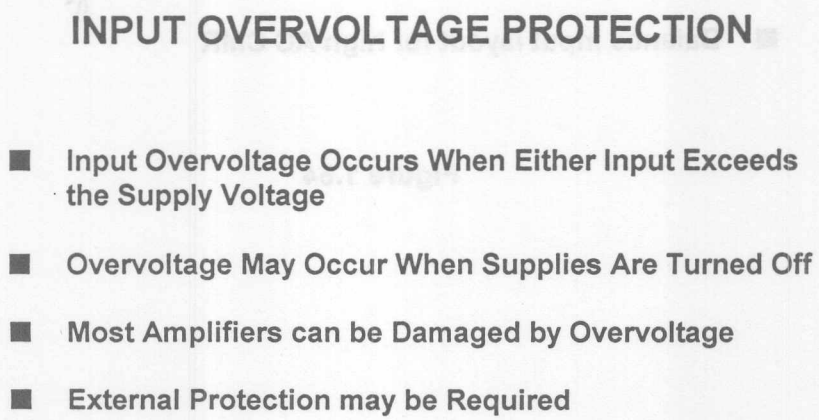


Figure 1.65

Any op amp input will break down to the positive rail or the negative rail if it encounters sufficient over-voltages. The breakdown voltage is entirely dependent on the structure of the input stage. It may be equivalent to a diode drop of 0.7V or to a process breakdown voltage of 50V or more. The danger of an overvoltage is that when conduction occurs large currents may flow, which can destroy the device. In many cases, overvoltage results in current well in over 100mA, which can destroy a part almost instantly.

To avoid damage, current should be limited to less than 5mA. This value is a conservative rule of thumb based on metal trace widths in a typical op amp input stage. Higher levels of current can cause metal migration, which will eventually lead to an open trace. Migration is a cumulative effect that may not result in a failure for a long period of time. Failure may occur due to multiple over-voltages, which is a difficult failure mode to identify. Thus, even though an amplifier may appear to withstand over-voltage currents well above 5mA for a short period of time, it is important to limit the current to guarantee long term reliability.

Two types of conduction occur in over-voltage conditions, forward biasing of PN junctions inherent in the structure of the input stage or, given enough voltage, reverse junction breakdown.

The danger of forward biasing a PN-junction is that excessive current will flow and damage the part. As long as the current is limited no damage should occur. However, when the conduction is due to the reverse breakdown of a PN junction, the problem can be more serious. In the case of a base-emitter junction break down, even small amounts of current can cause degradation in the beta of the transistor (Reference 15). After a breakdown occurs, input parameters such as offset and bias current may be well out of specification. Diode protection is needed to prevent base-emitter junction breakdown. Other junctions, such as base-collector junctions and JFET gate source junctions do not exhibit the same degradation in performance on break down, and for these the input current should be limited to 5mA.

OVERVOLTAGE CHARACTERISTICS

- Op Amps Will Conduct to the Positive and Negative Rail Given Enough Input Voltage
- The Voltage at Which Conduction Occurs Depends on the Input Stage Construction
- This Voltage may be as Low as a Diode Drop or as High as 30V or More
- Conduction Current Needs to be Limited (Rule of Thumb: 5mA)
- Avoid Reverse Bias Junction Breakdown in Base-Emitter Junctions
- No Two Amplifiers Are the Same

Figure 1.66

Various factors affect the over-voltage characteristics of an op amp. Figure 1.67 lists some of the structures commonly found in input stages. Such circuit elements as input protection diodes usually form a diode from a supply. When the input voltage goes more than 0.6V outside that supply, then a diode from the substrate through the protection diode conducts current and limits the input voltage. There are many different ways of building an input stage, and, with them, many different types of over-voltage characteristics. This list gives examples of various structures and their possible characteristics, but it certainly not exhaustive. Sometimes the characteristic of a particular op amp can be determined from a simplified schematic in the data sheet by looking for PN-junctions. Often, though, the data sheet schematic does not contain enough information to determine over-voltage characteristics. In these where no obvious breakdown path exists or the simplified schematic is not shown, the best strategy is to measure the performance.

FACTORS AFFECTING OVERVOLTAGE CHARACTERISTICS

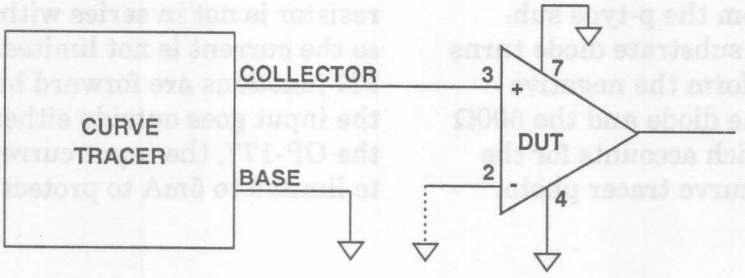
- INPUT PROTECTION DIODES: Usually Form a Diode from V–
- INPUT SERIES RESISTORS:
  - POLY: Form a Diode to V+
  - THIN FILM: Provides Current Limiting
- SUBSTRATE CONNECTION: Positive or Negative Supply
- INPUT TECHNOLOGY:
  - BIPOLAR: No Inherent Paths to Either Supply
  - JFET: Diode Formed from V– for P-Channel JFETs
- INPUT STAGE STRUCTURE: Is There a Conduction Path to Either Supply? Look for PN Junctions

Figure 1.67

A curve tracer can be configured to measure the over-voltage characteristics of any amplifier by connecting the part as shown in Figure 1.68. The curve tracer ramps a DC voltage on the input and measures the current flowing in the input stage. The supply voltages can be configured as desired; however for simplicity all measurements in this section were made with both supplies connected to ground. For most amplifiers this measurement yields the same results on both inputs. An exception to this is found with current feedback amplifiers, which have different characteristics at their inverting and noninverting inputs. If a curve tracer is not available, the measurements can be

done using a DC voltage source and a multi-meter. Connect the source to the input through a 10kΩ resistor, and measure the current as a function of the input voltage. Both methods yield the same results.

OVER-VOLTAGE CURVE TRACER TEST SETUP



- Test Both Inputs of Op Amp -- Results are Identical for Voltage Feedback Types, but Not Current Feedback
- Force a Voltage Using the Collector Output
- Display Collector Current Versus Voltage
- Results May Differ Depending on Whether the Other Input is Open or Grounded

Figure 1.68

Figures 1.69 through 1.78 show different examples of over-voltage characteristics of various op amps. A varied sample of devices were tested but this is certainly not an exhaustive selection of amplifiers. As mentioned above, two basic types of over-voltage characteristics are exhibited in amplifiers. Forward biased junctions are evident because, as the input voltage rises above the supplies, distinct break points are encountered when internal diodes turn on. In most cases, this characteristic occurs within one or two diode drops of either supply. On the other hand, reverse junction breakdown does not occur until the input goes 4V or more outside either supply. Breakdown voltages may be as large as 50V or even more. Such measurements are important because it is much easier to protect an amplifier against damage due to over-stress if its behavior when over-stressed is well understood.

Figure 1.69 shows the over-voltage characteristic of an OP-177 precision amplifier. As the curve tracer shows, an internal diode turns on and starts conducting when the input reaches 0.6V above the positive supply. In the negative direction, we see that a diode also turns on, but the input current is limited by a series resistance. The OP-177

input stage's schematic partially illustrates where the parasitic diodes develop. Figure 1.70 shows the cross section for the process to illustrate more clearly where the diodes originate. When the input goes 0.6V below the negative supply the cathode of the protection diode forms the cathode of a parasitic diode from the p-type substrate. When this substrate diode turns on, current flows form the negative supply through the diode and the 500Ω input resistor, which accounts for the slope seen in the curve tracer photo.

The actual resistor is fabricated with diffused p-type material in an n-well as shown in Figure 1.70. The n-well is biased to the positive supply potential. Thus, when the input voltage rises 0.6V above the positive supply, the diode formed by the p-type resistor and the n-well is turned on. In this case the resistor is not in series with the input, so the current is not limited. Because PN-junctions are forward biased when the input goes outside either supply of the OP-177, the input current need only to limited to 5mA to protect the device.

EFFECTS OF INPUT PROTECTION DIODES AND DIFFUSED RESISTORS FOR THE OP-177

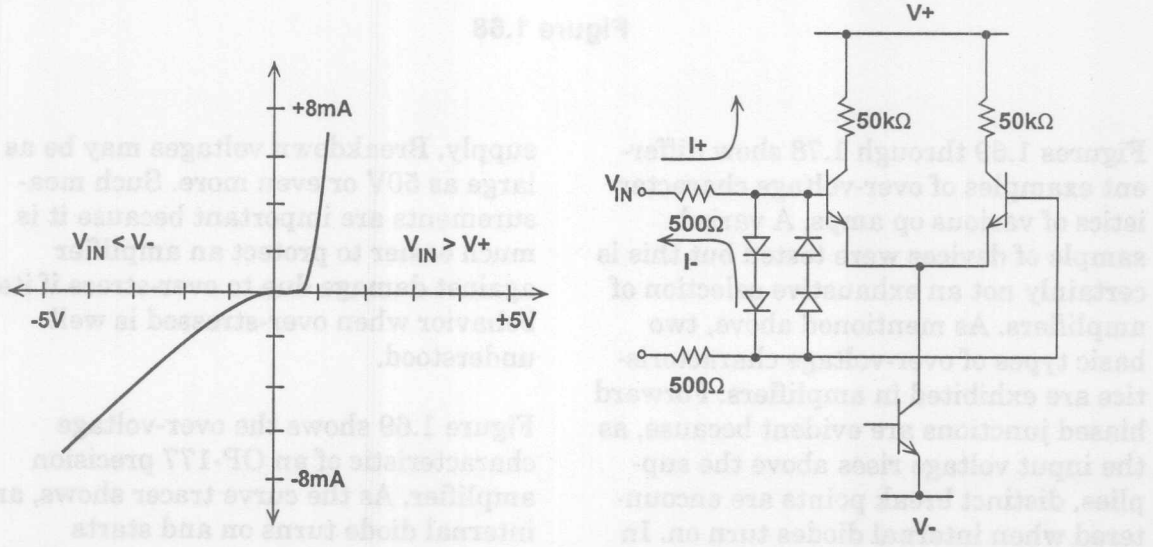


Figure 1.69

OP-177 CROSS-SECTION SHOWS CURRENT PATHS

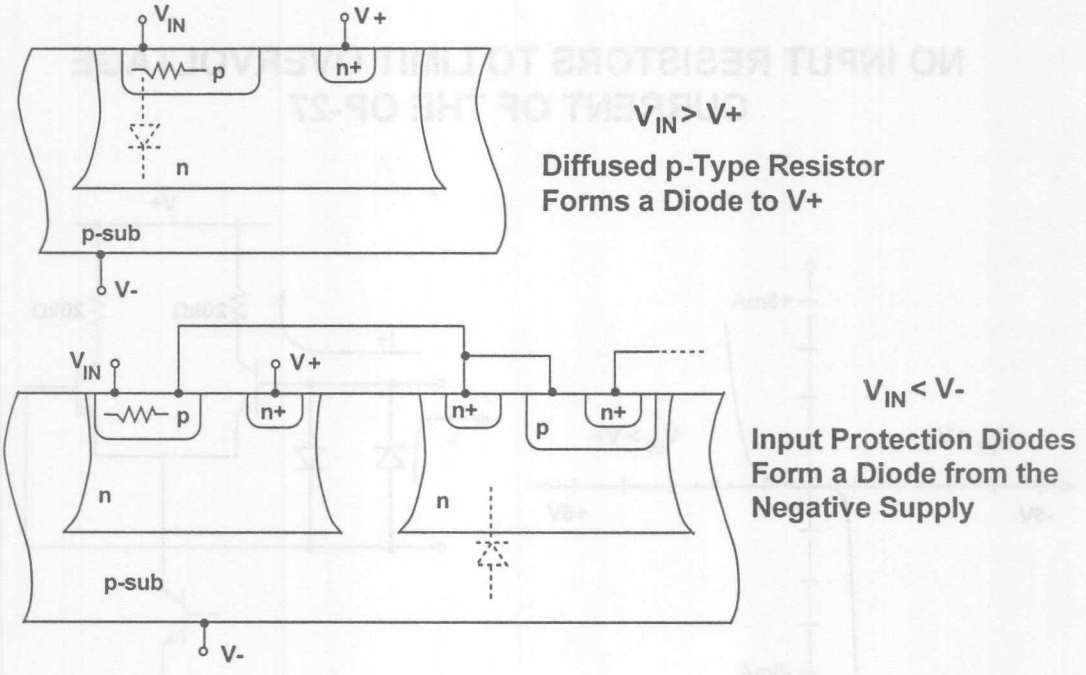


Figure 1.70

The OP-27 is an example of an input stage without input protection resistors (Figure 1.71). It still has input protection diodes, and like the OP-177, these form a diode from the substrate (Figure 1.72). As is evident in the curve tracer photo, the current is no longer limited in the negative direction because there are no input resistors. In the positive direction, the base collector junction of the NPN input transistor is forward biased at 0.6V above V+, and current starts to flow through the collector resistor. This collector resistor is also a p-type diffused resistor in an n-well. Thus, when the voltage across the resistor exceeds 0.6V a second diode turns on. The curve tracer actually shows the two diodes turning on. The first breakpoint occurs at 0.6V, which is followed by a sloped section due to the 20kΩ collector resistor, then a second breakpoint at 1.2V. Above this point, current flows with no limit. Since current is not limited in either direction, external protection is required to limit the input current to less than 5mA.

NO INPUT RESISTORS TO LIMIT OVERVOLTAGE CURRENT OF THE OP-27

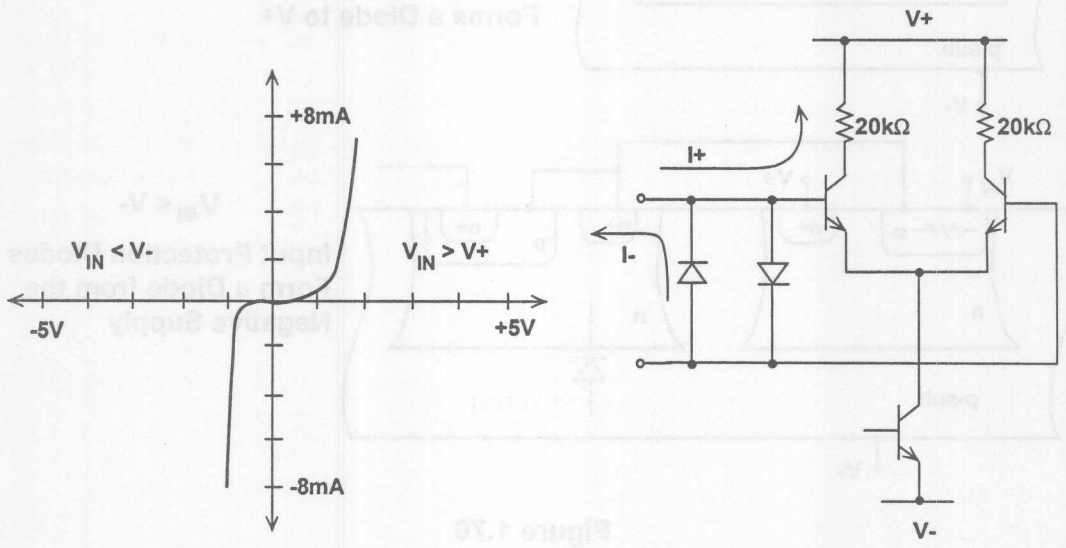
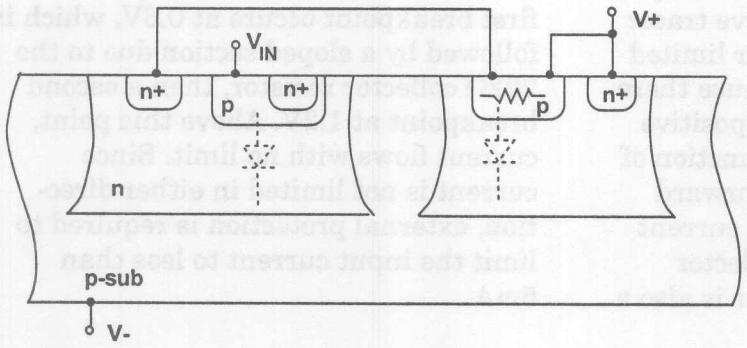


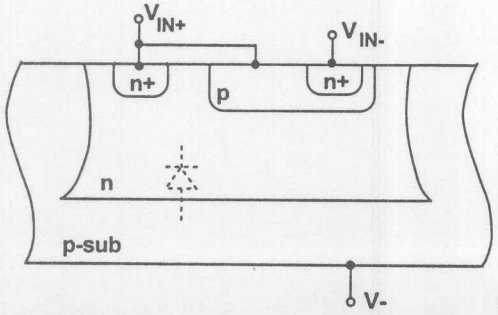
Figure 1.71

OP-27 CROSS SECTION



V_{IN} > V+

Forward Biases Base-Collector Junction First. Current is Limited By Collector Resistance. At 1.4V, Diffused Resistor Also Forward Biases.



V_{IN} < V-

Forward Biased Substrate Junction of Input Protection Diodes

Figure 1.72

Another common input stage device is a p-channel JFET differential pair. The part used as an example is the OP-42, but other JFET input devices such as the AD711, AD712, and OP-282 exhibit similar characteristics. As the curve tracer photo shows (Figure 1.73) the over-voltage characteristic is very different from those of the previous amplifiers. There is no over-voltage conduction path in the positive direction because there are no PN-junctions from the gate (Figure 1.74). When a positive over-voltage is applied to the inputs, the n-well and n-gate are pulled above V+.

Thus, the PN-junctions (formed by the gate to drain and n-well to substrate) are reverse biased and no conduction occurs. If the input voltage is increased the input junctions eventually break down. For the OP-42 this breakdown occurs at approximately 44V. This breakdown, unlike base-emitter breakdown, is not damaging to the JFETs as long as the input current is limited to less than 5mA. However, to ensure that the input is not damaged, external clamping, using a diode, is recommended if the input voltage approaches the breakdown region.

P-CHANNEL JFET INPUT OF THE OP-42

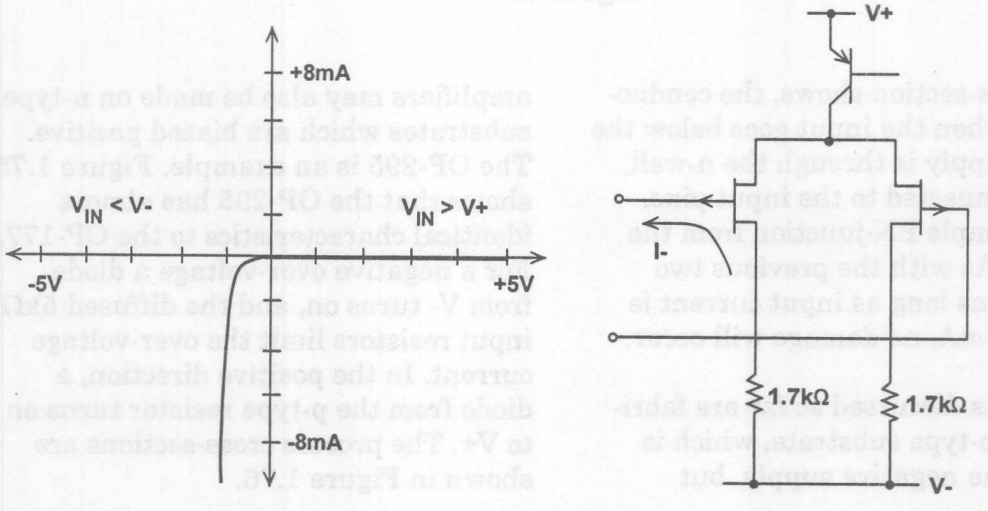


Figure 1.73

OP-42 CROSS SECTION

- $V_{IN} > V+$ — No Current Path, Breakdown Voltage > 30V
- $V_{IN} < V-$ — P-Channel JFET Forms a Diode From V-

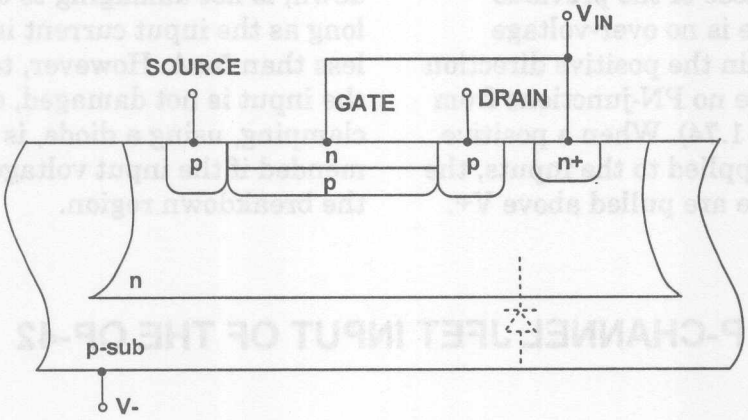


Figure 1.74

As the cross-section shows, the conduction path when the input goes below the negative supply is through the n-well, which is connected to the input pins. This is a simple PN-junction from the substrate. As with the previous two amplifiers, as long as input current is limited to 5mA, no damage will occur.

All the parts discussed so far are fabricated on a p-type substrate, which is biased to the negative supply, but amplifiers may also be made on n-type substrates which are biased positive. The OP-295 is an example. Figure 1.75 shows that the OP-295 has almost identical characteristics to the OP-177. For a negative over-voltage a diode from V- turns on, and the diffused 5kΩ input resistors limit the over-voltage current. In the positive direction, a diode from the p-type resistor turns on to V+. The process cross-sections are shown in Figure 1.76.

OP-295 ILLUSTRATES N-TYPE SUBSTRATE

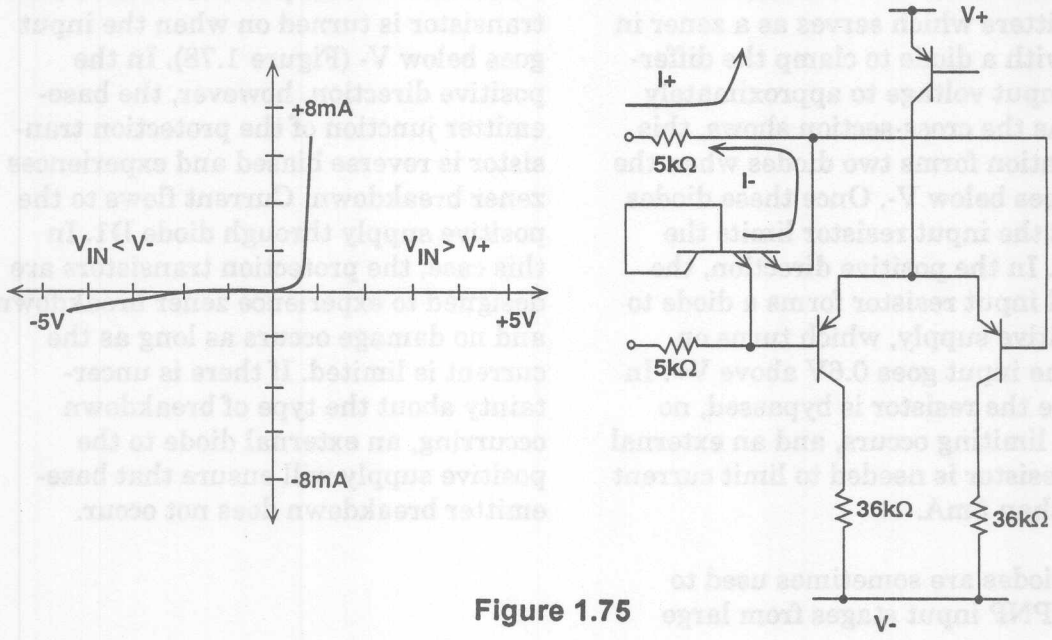
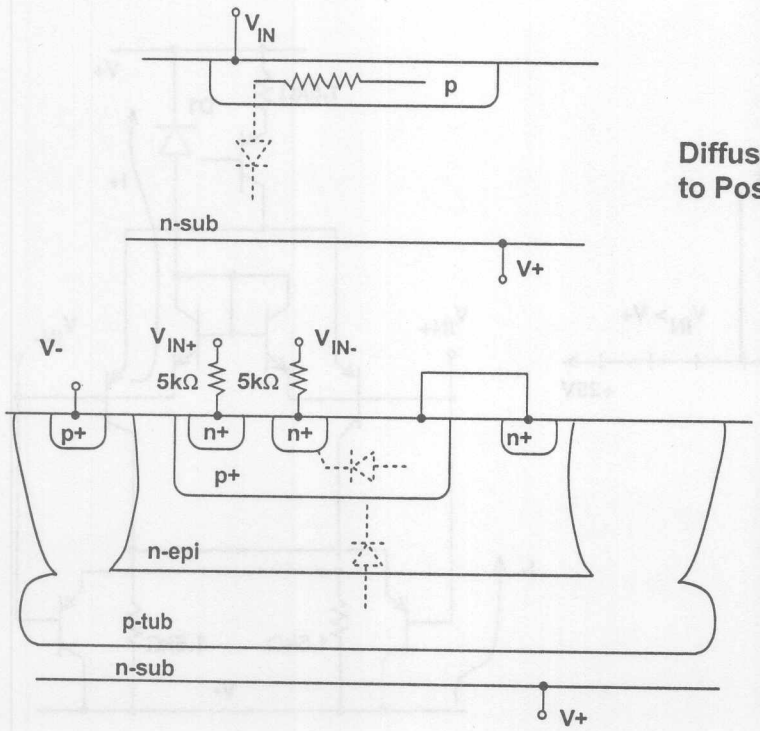


Figure 1.75

OP-295 CROSS SECTION



V_{IN} > V+

Diffused Resistor Forms Diode to Positive Supply

V_{IN} < V-

Protection Diode Provides Path from V-

Figure 1.76

The substrate is n-type and biased to the positive supply. NPN devices are built in p-wells biased to the negative supply. The input protection device on the OP-295 is an NPN transistor with two emitters which serves as a zener in series with a diode to clamp the differential input voltage to approximately ±10V. As the cross-section shows, this combination forms two diodes when the input goes below V-. Once these diodes conduct the input resistor limits the current. In the positive direction, the diffused input resistor forms a diode to the positive supply, which turns on when the input goes 0.6V above V+. In this case the resistor is bypassed, no current limiting occurs, and an external series resistor is needed to limit current to less than 5mA.

Zener diodes are sometimes used to protect PNP input stages from large differential voltages. The OP-213 input stage has two pairs of PNP input transistors (Figure 1.77). The breakdown in the negative direction is very simple. The collector-base junction of the PNP transistor is turned on when the input goes below V- (Figure 1.78). In the positive direction, however, the base-emitter junction of the protection transistor is reverse biased and experiences zener breakdown. Current flows to the positive supply through diode D1. In this case, the protection transistors are designed to experience zener breakdown and no damage occurs as long as the current is limited. If there is uncertainty about the type of breakdown occurring, an external diode to the positive supply will ensure that base-emitter breakdown does not occur.

OP-213 ILLUSTRATES ZENER DIODE BREAKDOWN

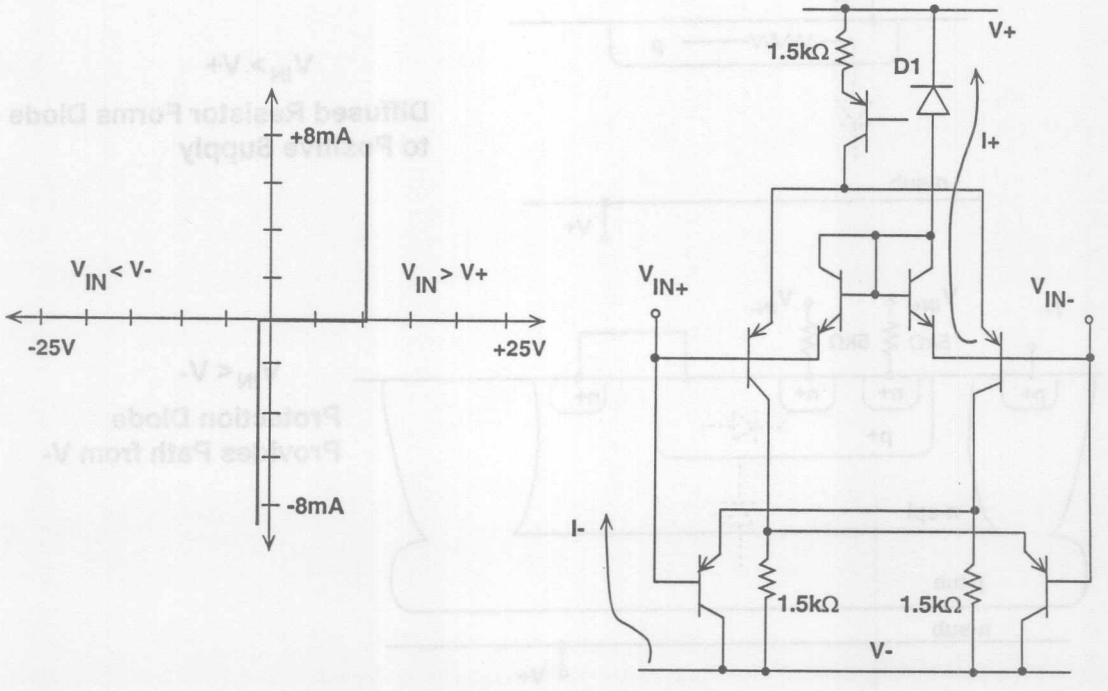


Figure 1.77

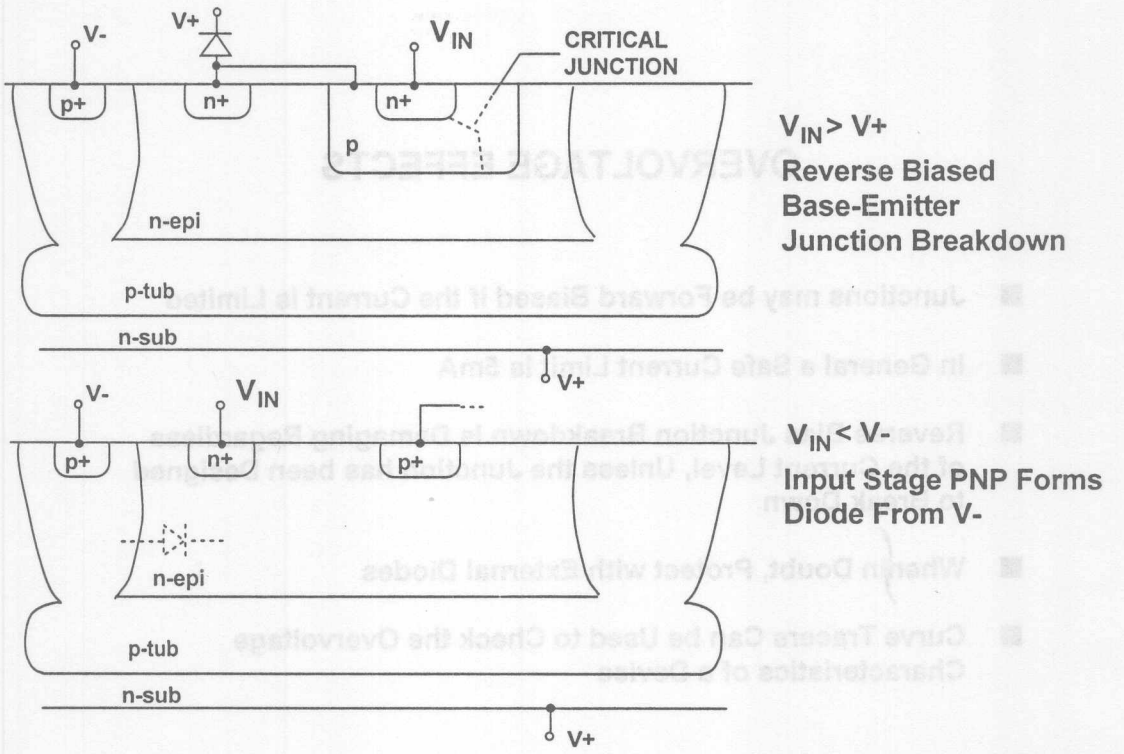


Figure 1.78

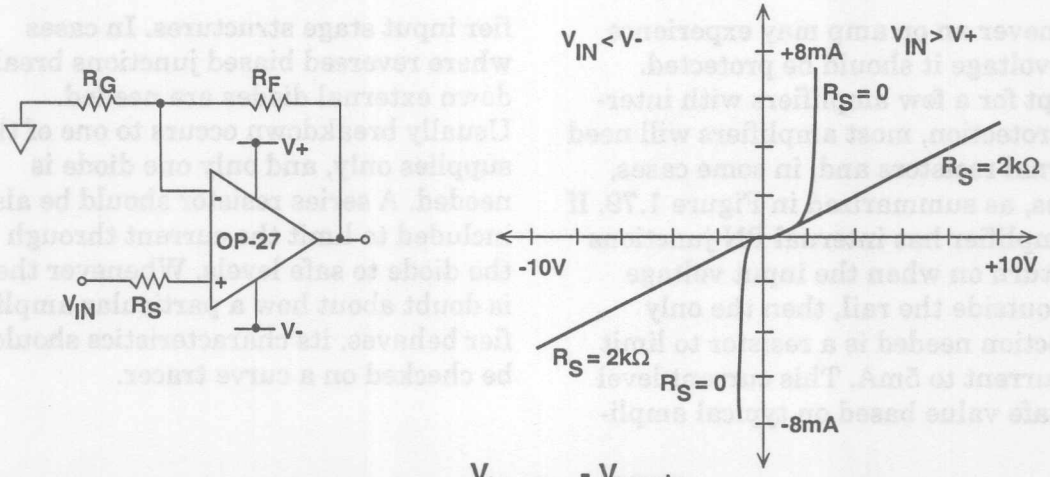
Whenever an op amp may experience over-voltage it should be protected. Except for a few amplifiers with internal protection, most amplifiers will need external resistors and, in some cases, diodes, as summarized in Figure 1.79. If an amplifier has internal PN-junctions that turn on when the input voltage goes outside the rail, then the only protection needed is a resistor to limit the current to 5mA. This current level is a safe value based on typical amplifier input stage structures. In cases where reversed biased junctions break down external diodes are needed. Usually breakdown occurs to one of the supplies only, and only one diode is needed. A series resistor should be also included to limit the current through the diode to safe levels. Whenever there is doubt about how a particular amplifier behaves, its characteristics should be checked on a curve tracer.

OVERVOLTAGE EFFECTS

- Junctions may be Forward Biased if the Current is Limited
- In General a Safe Current Limit is 5mA
- Reverse Bias Junction Breakdown is Damaging Regardless of the Current Level, Unless the Junction has been Designed to Break Down
- When in Doubt, Protect with External Diodes
- Curve Tracers Can be Used to Check the Overvoltage Characteristics of a Device

Figure 1.79

SERIES RESISTOR LIMITS OVERVOLTAGE CURRENT



- Pick R_S Such That: $R_S = \frac{V_{in\ max} - V_{supply}}{5mA}$
- For Example, When V_{supply} is Turned Off, and $V_{in\ max} = 10V$, $R_S = 2k\Omega$

Figure 1.80

Figure 1.80 shows the difference between a protected and an unprotected input stage. The curve tracer photo shows the OP-27 over-voltage characteristic without a series resistor. The current reaches 10mA with less than 1V on the input. With a 2kΩ resistor in series with the input, the current is limited to ±5mA for input voltages up to 10V outside the supply voltages. R_S is chosen so that at maximum over-voltage the current is limited to 5 mA. Most op-amp applications require over-voltage protection at only one input, but there are a few (differential amplifiers, for example) where both inputs can experience over-voltage and both must be protected. The need for both inputs to be protected is much commoner with instrumentation amplifiers.

It is evident that whenever resistance is added in series with an amplifier's input, its offset and noise performance is slightly degraded. In Figure 1.81, the additional noise and offset are calculated. The thermal noise of the resistor, the voltage noise due to the amplifier noise current flowing in the resistor and the input noise voltage of the amplifier are added together (using root sum of squares addition, since the noise voltages are uncorrelated) to determine the total input noise and may be compared with the input voltage noise in the absence of the protection resistor.

A protection resistor in series with an amplifier input has a voltage drop due to the amplifier bias current flowing in it. This drop appears in the system as an increase of offset voltage (and, if the bias current changes with temperature, offset drift). In amplifiers where bias currents are approximately equal a resistor in each input will tend to balance the effect and reduce the error.

If large resistors are necessary for adequate protection these noise and offset effects may become intolerable. In such a case it may be possible to use external Schottky diodes to clamp at higher current levels than the 5 mA limit on internal currents.

Figure 1.82 shows the benefit of adding an external diode to clamp the input over-voltage. The OP-213 with its 10V positive breakdown is used as an example. As the curve tracer shows, the clamp diode turns on when the input exceeds V+ by 0.6V, and the series resistor limits current in both directions. Two configurations are shown. The upper configuration offers lower leakage for small input voltages because the reverse bias on the diode is small but cannot be used with inputs >50mV as the diode turns on and the leakage goes up. In the lower configuration the cathode of the diode is connected to V+. The diode will not turn on until the input exceeds V+. This arrangement has higher leakage. A series resistor is still needed to limit the current.

SERIES RESISTOR EFFECTS

- Increases Noise:

$$E_{n\ Total} = \sqrt{e_{n\ op\ amp}^{\ 2} + e_{n\ Rs}^{\ 2} + (Rs \cdot i_{n\ op\ amp})^2}$$

- Voltage Offset Increases Due to Bias Currents:
  - $V_{os\ Total} = V_{os} + I_b R_s$
  - Balance Input Impedance to Minimize I_b Errors, $R_s = R_1 || R_2$
  - $V_{os\ Total} = V_{os} + I_{os} R_s$

Figure 1.81

DIODE CLAMP PREVENTS REVERSE BIAS BREAKDOWN

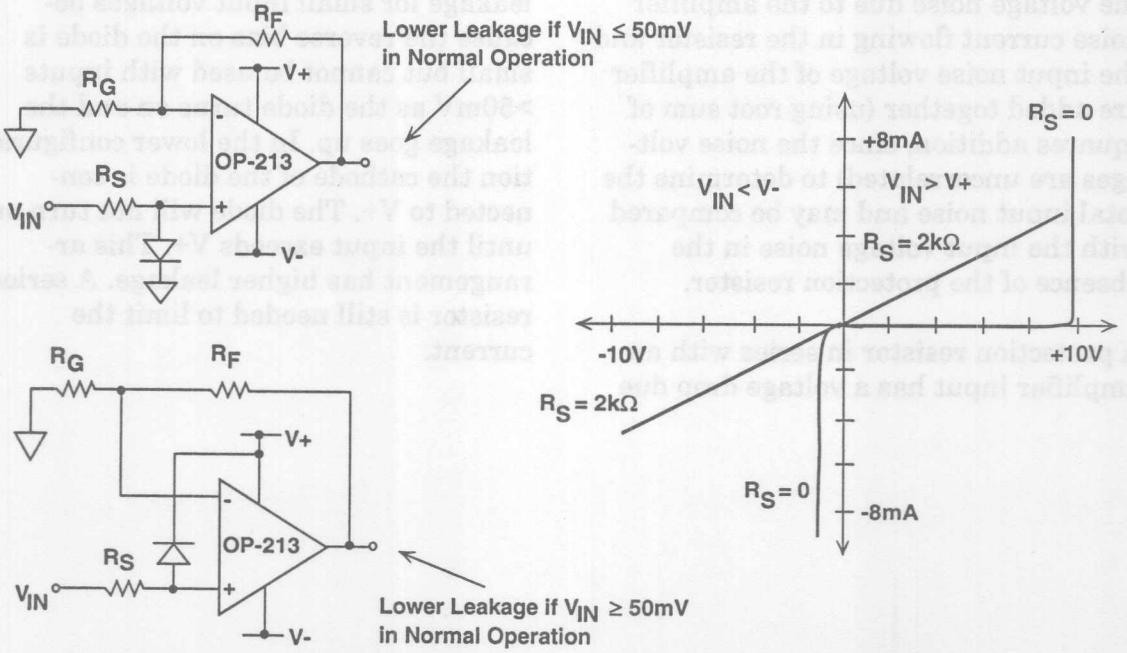


Figure 1.82

The choice of diode is important in applications where low bias current is important. Any component added to the input pin contributes some leakage. The choice of the diode depends on the bias current requirement for the application. The table in Figure 1.83 shows various protection diodes and their leakage currents. The common 1N914 or 1N4148 diode typically has 10nA of leakage current and is not a very good choice when using a JFET amplifier. A good choice for a protection diode is the base-collector junction of a 2N3906 transistor which is inexpensive and has leakage currents on the order of 10pA. For the most demanding applications, low leakage FETs may be required. Such parts as the 2N4117A and PAD1, from Siliconix, provide protection with leakage currents under 1pA. Temperature effects must also be considered, as the leakage current of diodes and JFET junctions doubles for every 10°C temperature rise.

The parts discussed do not have internal over-voltage protection. However, there is a small group of amplifiers that are designed to handle input voltages which exceed their supplies (Figure 1.84). Some of these parts have thin film resistors in series with their inputs. These resistors are isolated from the silicon and do not form a diode to a supply. They limit current as an external resistor does. The AMP-02 and the AD524 have protection JFETs in the input stage that turn on during overvoltage and allow the inputs to reach ±60V without damage.

DIODE CLAMP LEAKAGE AFFECTS BIAS CURRENT

- Diode Leakage May Be Significant Compared To I_b
- If Important: Pick A Low Leakage Diode
- Remember Leakage Doubles for every 10°C Temperature Rise

Diode	Leakage @ 25°C
1N914 1N4148	10nA 10nA
2N3906 (Base-Collector Junction)	10pA
2N4117A* PAD1* * Siliconix JFETS	1pA 1pA

Figure 1.83

SOME AMPLIFIERS HAVE BUILT-IN PROTECTION

- OP-90: Thin Film Input Resistors Allow the Input Voltage to Exceed the Supplies By 20V
- AMP-02: Protection FETs Allow 60V Inputs
- AD524, : Thin-Film Input Resistors Allow 60V Inputs
  AD626
- AMP-03, : 25kΩ Thin-Film Input Resistors
  SSM-2141
- SSM-2143: 12kΩ Thin-Film Input Resistors

Figure 1.84

Input over-voltage is a common problem. It can cause serious damage if suitable protection is not provided by the circuit designer. To provide such protection it is necessary to identify the values of over-voltage to be expected, and to understand the behavior of the amplifier used under over-voltage stress. Armed with this information the designer can provide suitable protection for his circuit.

AMPLIFIER OUTPUT PHASE REVERSAL

Some amplifiers exhibit output voltage phase reversal when their input exceeds their common mode range. Phase reversal is usually associated with JFET input amplifiers, but some bipolar devices (especially single supply amplifiers) may also be susceptible. Phase reversal does not harm the amplifier, but it may be disastrous in a servo loop! Once the amplifier inputs return within the correct operating range, output phase reversal ceases. Although a number of op amps suffer from phase reversal it is, surprisingly, rarely a problem in system design. It may also be necessary to consult the amplifier manufacturer, since phase reversal information rarely appears on data sheets.

Phase reversal in a BiFET op amp may be prevented by adding an appropriate input series resistance to limit the input current. Biplolar input devices may be protected by using a schottky diode to clamp the input to within a few hundred millivolts of the appropriate, usually negative, rail. For more information on phase reversal and how to prevent it, refer to Reference 1, Section XI, pages 1-10.

AMPLIFIER LATCH-UP

Destructive latch-up on power-up is rare in modern ICs. The typical trigger mechanism for latch-up is a signal which is present at an input of a device before power is applied. This may cause a parasitic SCR to fire, large currents flow between the supply pins and the device is damaged. This was common in older CMOS devices, but most IC op amps do not behave in this way.

If latch-up is a concern, the amplifier may be easily checked easily for susceptibility. Apply an input to the amplifier and, using current-limited supplies so that no damage is done if latch-up does occur, apply power to the device. If the device has more than one supply, it should be tested with every possible sequence of supply turn-on (i.e., V_{CC} then V_{SS} then V_{logic}; V_{SS} then V_{CC} then V_{logic}; etc., through ALL combinations). The test should be performed with all possible inputs as well. All op amps discussed in this section of the book have been checked in this way and are free from latch-up.

BEWARE OF AMPLIFIER OUTPUT PHASE REVERSAL

- **Sometimes Occurs in FET and Bipolar Input (Especially Single-Supply) Op Amps when Input Exceeds Common Mode Range**
- **Does Not Harm Amplifier, but may be Disasterous in Servo Systems!**
- **Not Usually Specified on Data Sheet, so Amplifier Must be Checked**
- **Easily Prevented:**

  BiFETs: **Add Appropriate Input Series Resistance**

  Bipolars: **Use Schottky Diode to Clamp Input Within the Supply Rails. Note: Some CB Process Devices Exhibit Phase Reversal with *POSITIVE*, and not Negative Inputs.**

Figure 1.85

OP AMP LATCH-UP RARELY OCCURS, BUT:

- If it does occur, it usually occurs when power is applied in the presence of an input signal (common occurrence in older CMOS devices)
- Large currents due to SCR action may destroy device
- Carefully observe all *Absolute Maximum* specifications
- If in doubt, consult manufacturer and test amplifier for latch-up
- "Catch" diodes (Schottky) from input to positive and negative supply rails may be added for additional protection against latch-up

Figure 1.86

TRANSMITTING PRECISION SIGNALS IN NOISY ENVIRONMENTS

Signal integrity is often compromised in the interconnections between portions of electronic systems (Reference 16) . In industrial applications, precision signals must often be transmitted long distances to other signal conditioning or A/D conversion circuitry without loss of accuracy. Balanced transmission and reception techniques can reject both HF and LF interference and maintain accuracy. There are many ways of implementing balanced signal transmission and reception, but not all of them are suitable for the transmission of high precision DC and LF signals. Most of the viable techniques use op-amps and instrumentation amplifiers.

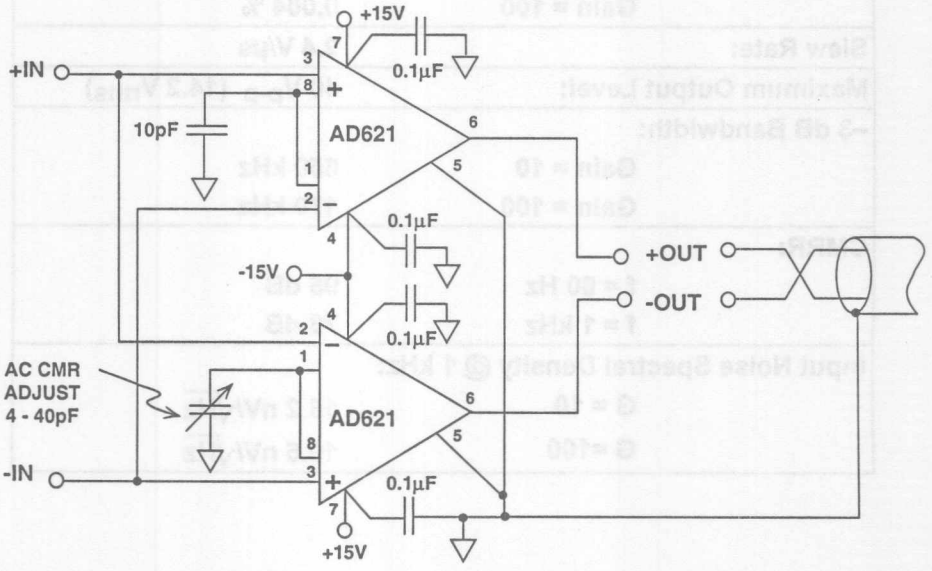
PARALLELING AMPLIFIERS FOR A PRECISION LINE DRIVER [REFERENCE 16]

One of the more important tasks of any signal conditioner is preserving signal-to-noise ratio. The circuit in Figure 1.87 illustrates a method of preserving signal-to-noise ratio in a system where two instrumentation amplifiers are connected together to form a precision differential line driver. The signal-to-noise ratio of the circuit is improved by $\sqrt{2}$ over a single amplifier because the output signals add differentially and are multiplied by 2, while the input noise only increases by $\sqrt{2}$.

In this circuit, the inputs of a pair of AD621s are connected in anti parallel while the outputs signal appears differentially between the outputs of the AD621s. Even though each instrumentation amplifier can be configured to

gains of 10 or 100, the circuit gain is twice this because of the differential output connection. The line driver exhibits an excellent transient response even when the output is 40 V_{p-p} (Figure 1.88). Its performance is summarized in Figure 1.89.

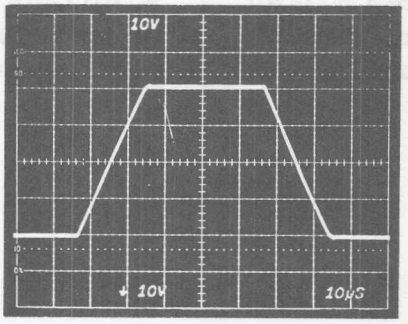
STACKING TWO INSTRUMENTATION AMPLIFIERS MAKES A PRECISION DIFFERENTIAL LINE DRIVER



G = 100

Figure 1.87

STACKED INSTRUMENTATION AMPLIFIER EXHIBITS EXCELLENT TRANSIENT RESPONSE



Horozontal Scale: 10us/div.
Vertical Scale: 10V/div.

G = 10

V_{in} = 2V peak-to-peak

Figure 1.88

PERFORMANCE OF PRECISION STACKED LINE DRIVER

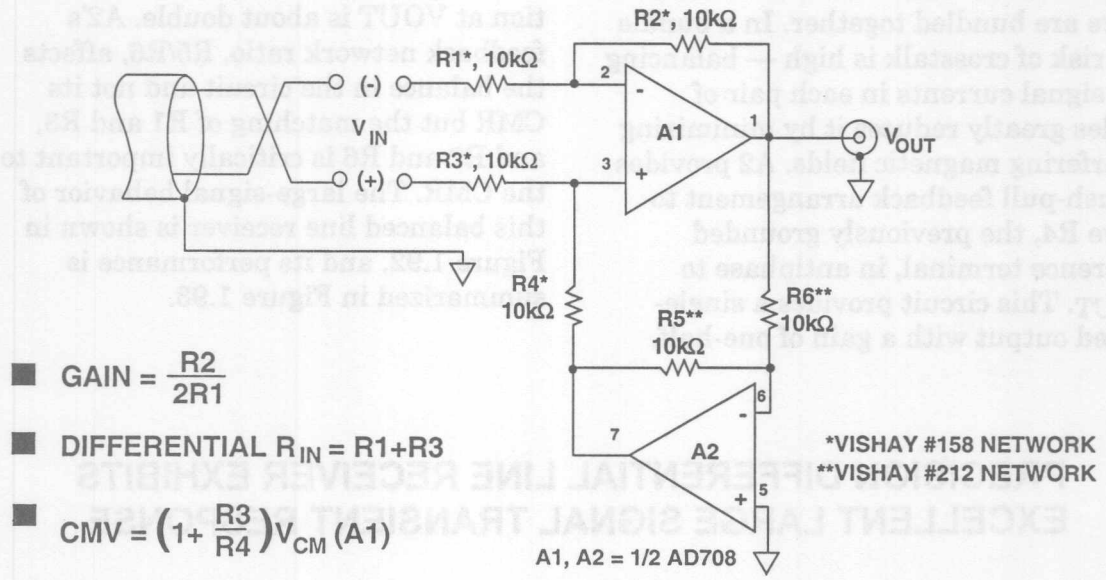
Nonlinearity:		
	Gain = 10	0.0002 %
	Gain = 100	0.004 %
Slew Rate:		2.4 V/μs
Maximum Output Level:		40 V_{p-p} (14.2 V_{rms})
–3 dB Bandwidth:		
	Gain = 10	650 kHz
	Gain = 100	170 kHz
CMRR:		
	f = 60 Hz	95 dB
	f = 1 kHz	73 dB
Input Noise Spectral Density @ 1 kHz:		
	G = 10	16.2 nV/$\sqrt{Hz}$
	G =100	10.5 nV/$\sqrt{Hz}$

Figure 1.89

A HIGH-PRECISION, BALANCED LINE RECEIVER [REFERENCE 17]

As important as the line driver is the differential line receiver. A line receiver's primary function is to reject common-mode noise. Figure 1.90 is an example of a high-precision, balanced line receiver built with a precision dual op amp, the AD708. The AD708's tight matching of V_{OS}, TCV_{OS}, I_B, and CMRR yield a design that achieves 95 dB CMR from dc to 1 kHz. The common-mode performance of the circuit is shown in Figure 1.91.

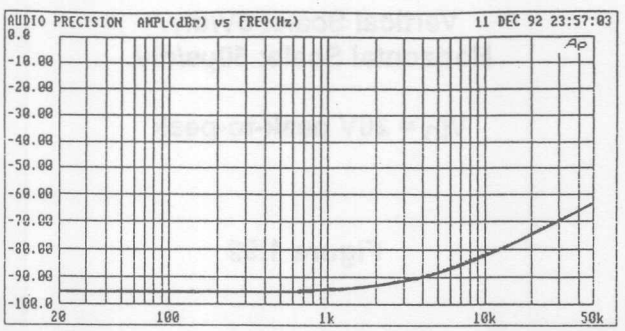
USING A HIGH PERFORMANCE DUAL OP AMP AS A PRECISION DIFFERENTIAL LINE RECEIVER



- GAIN = $\frac{R2}{2R1}$
- DIFFERENTIAL R_{IN} = R1+R3
- CMV = $\left(1+\frac{R3}{R4}\right)V_{CM}$ (A1)

Figure 1.90

USING A PRECISION DUAL OP AMP WITH MATCHED CHARACTERISTIC YIELDS HIGH CMRR

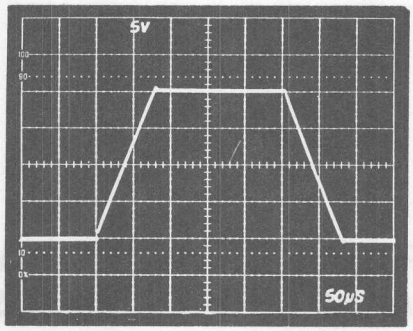


Vin = 2V peak-to-peak

Figure 1.91

The circuit uses a balanced topology that equalizes the signal currents in the two inputs, which is important in applications where a number of twisted pairs are bundled together. In a bundle the risk of crosstalk is high — balancing the signal currents in each pair of cables greatly reduces it by minimizing interfering magnetic fields. A2 provides a push-pull feedback arrangement to drive R4, the previously grounded reference terminal, in antiphase to V_{OUT}. This circuit provides a single-ended output with a gain of one-half, assuming that R2 = R1. The common-mode range of the circuit is equal to the common-mode range of conventional line receivers, but common-mode rejection at VOUT is about double. A2's feedback network ratio, R5/R6, affects the balance in the circuit and not its CMR but the matching of R1 and R3, and R2 and R6 is critically important to the CMR. The large-signal behavior of this balanced line receiver is shown in Figure 1.92, and its performance is summarized in Figure 1.93.

PRECISION DIFFERENTIAL LINE RECEIVER EXHIBITS EXCELLENT LARGE SIGNAL TRANSIENT RESPONSE



Vertical Scale: 5V/div.
Horizontal Scale: 50µs/div.

V_{IN} = 20V peak-to-peak

Figure 1.92

PERFORMANCE OF PRECISION LINE RECEIVER

Nonlinearity	0.00045
Slew Rate	0.3 V/μs
Common-Mode Input Range	± 28 V
–3 dB Bandwidth	660 kHz
CMRR	95 dB

Figure 1.93

ISOLATING TRANSDUCERS

There are many applications where it is desirable, or even essential, for a transducer to have no direct ("galvanic") electrical connection with the system to which it is supplying data, either in order to avoid the possibility of dangerous voltages or currents from one half of the system doing damage in the other, or to break an intractable ground loop. Such a system is said to be "isolated" and the arrangement which passes a signal without galvanic connections is known as an "isolation barrier".

The protection of an isolation barrier works in both directions, and may be needed in either, or even in both. The obvious application is where a sensor may accidentally encounter high voltages and the system it is driving must be protected, but it is equally possible that a sensor may need to be isolated from accidental high voltages arising downstream, in order to protect its environment:- examples include the need to prevent the ignition of explosive gases by sparks at sensors and the protection from electric shock of patients whose ECG, EEG or EMG is being monitored. The ECG case is interesting as protection may be required in *both* directions: the patient must be protected from accidental electric shock, but if the patient's heart should stop the ECG machine must be protected from the very high voltages (>7.5 kV) applied to the patient by the defibrillator which will be used to attempt to restart it.

WHERE IS ISOLATION USED?

- Transducer is at a High Potential Relative to other Circuitry (or may become so under fault conditions)
- Transducer may not Carry Dangerous Voltages, Irrespective of Faults in other Circuitry (e.g. Patient Monitoring and Intrinsically Safe Equipment for use with Explosive Gases)
- To Break Ground Loops

Figure 1.94

Just as interference, or *unwanted* information, may be coupled by electric or magnetic fields, or by electro-magnetic radiation, these phenomena may be used for the transmission of *wanted* information in the design of isolated systems. The commonest isolation amplifiers use transformers, which exploit magnetic fields, and another common type uses small high voltage capacitors, exploiting electric fields.

Opto-isolators, which consist of an LED and a photocell, provide isolation by using light, a form of electro-magnetic radiation. Different isolators have differing performance: some are sufficiently linear to pass high accuracy analog signals across an isolation barrier, with others the signal may need to be converted to digital form before transmission if accuracy is to be maintained.

TECHNIQUES FOR ISOLATION

- **Electric Field** — **Capacitive Signal Coupling**
- **Magnetic Field** — **Transformer Coupling**
- **Electromagnetic** — **Optical Coupling**
- **Sometimes a Technique will not have Adequate Linearity-- In Such Cases There are two Possibilities:**
  - **Voltage-Frequency Conversion / Transmission / Frequency-Voltage Conversion**
  - **Analog-Digital Conversion Before Transmission Across the Isolation Barrier**

Figure 1.95

Transformers are capable of analog accuracy of 12-16 bits and bandwidths up to several hundred kHz, but their maximum voltage rating rarely exceeds 10 kV and is often much lower. Capacitively coupled isolation amplifiers have lower accuracy, perhaps 12-bits maximum, lower bandwidth and lower voltage ratings - but they are cheap. Optical isolators are fast and cheap, and can be made with very high voltage ratings (although 4-7 kV is one of the commoner ratings), but they have poor linearity and are not usually suitable for direct coupling of precision analog signals (although there are some exceptions to this generalization they tend to be expensive).

Linearity and isolation voltage are not the only issues to be considered in the choice of isolation systems. Power is

essential. Both the input and the output circuitry must be powered and unless there is a battery on the isolated side of the isolation barrier (which is possible, but rarely convenient) some form of isolated power must be provided. Systems using transformer isolation can easily use a transformer (either the signal transformer or another one) to provide isolated power, but it is impracticable to transmit useful amounts of power by capacitive or optical means and systems using these forms of isolation must make other arrangements to obtain isolated power supplies - this is a powerful consideration in favor of choosing transformer isolated isolation amplifiers: they almost invariably include an isolated power supply. An example is the AD210 (Figure 1.96).

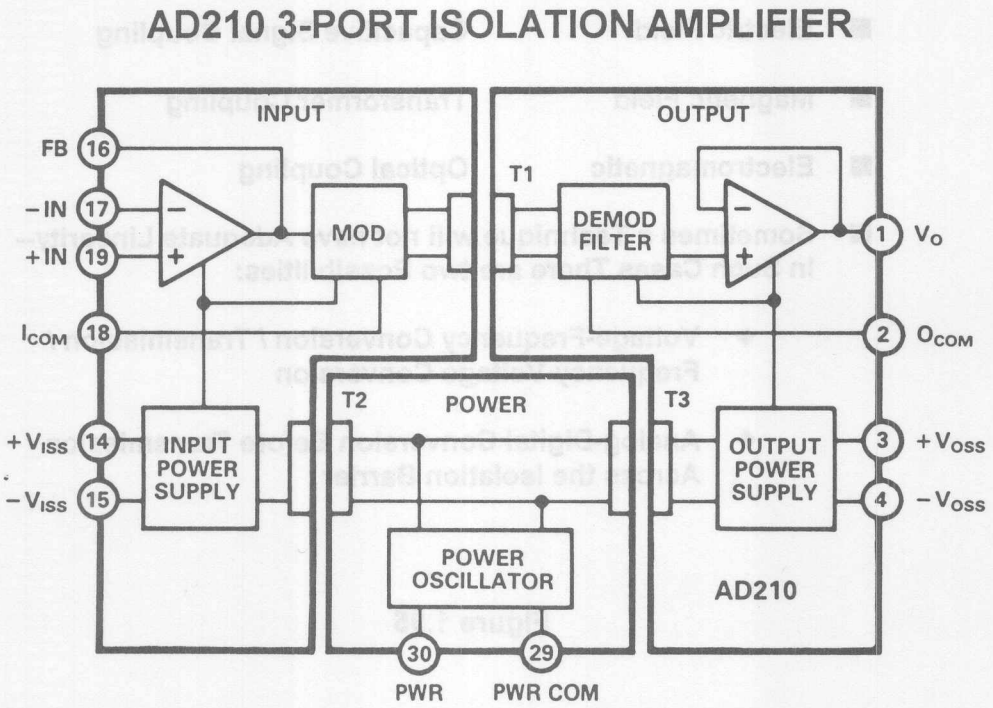


Figure 1.96

The AD210 is a 3-port isolation amplifier: the power circuitry is isolated from both the input and the output stages and may therefore be connected to either - or to neither. It uses transformer isolation to achieve 3500 V isolation with 12-bit accuracy. Key specifications for the AD210 are summarized in Figure 1.97.

AD210 ISOLATION AMPLIFIER KEY FEATURES

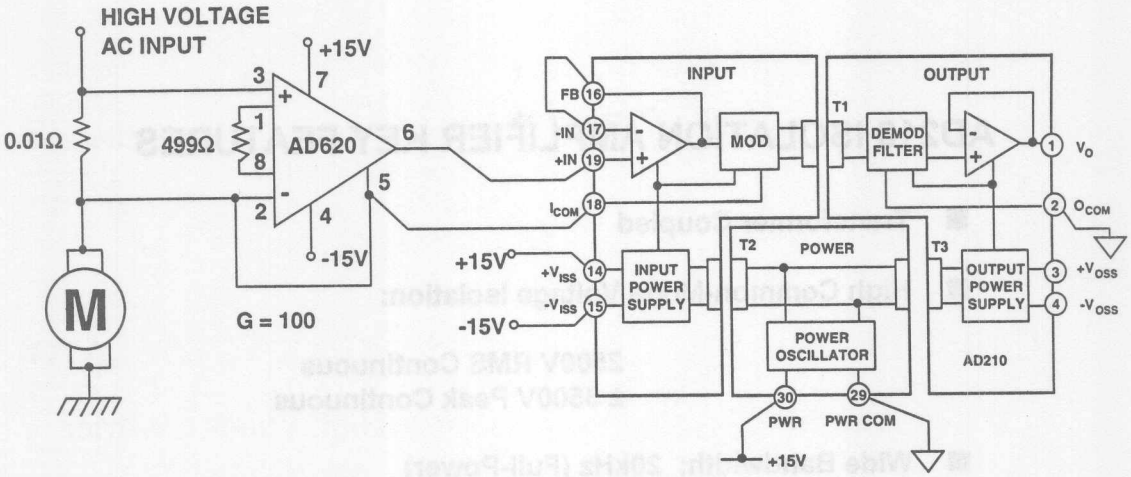
- Transformer Coupled
- High Common-Mode Voltage Isolation:

  2500V RMS Continuous
  ± 3500V Peak Continuous
- Wide Bandwidth: 20kHz (Full-Power)
- ± 0.012% Maximum Non-Linearity
- Input Amplifier: Gain 1 to 100
- Isolated Input and Output Power Supplies, ± 15V @ ± 5mA

Figure 1.97

A typical isolation amplifier application using the AD210 is shown in Figure 1.98. The AD210 is used with an AD620 instrumentation amplifier in a current-sensing system for motor control. The input of the AD210, being isolated, can be connected to a 110 or 230 V power line without any protection, and the isolated ±15 V powers the AD620, which senses the voltage drop in a small current sensing resistor. The 110 or 230 V rms common-mode voltage is ignored by the isolated system. The AD620 is used to improve system accuracy: the V_{OS} of the AD210 is 15 mV, while the AD620 has V_{OS} of 30 μV and correspondingly lower drift. If higher DC offset and drift are acceptable the AD620 may be omitted and the AD210 used directly at a closed loop gain of 100.

MOTOR CONTROL CURRENT SENSE



- High Accuracy/Low-Drift of AD620
- AD620 Powered By AD210
- Floating, Isolated, Senses Up To 2000V

Figure 1.98

ADI's range of transformer coupled isolation amplifiers is listed in Figure 1.99. There are a variety of devices with differing accuracies, bandwidths and breakdown voltages (as high as 3.5 kV), and, using transformer isolation, all of them have isolated power supplies, which simplifies system design.

ISOLATION AMPLIFIER FAMILY

Part	Peak Isolation Voltage	Gain Range V/V	Gain Nonlinearity % Maximum	Frequency Response, kHz
AD202	1000 - 2000	1 - 100	0.025 - 0.05	2
AD203	2000	1 - 100	0.025	10
AD204	1000 - 2000	1 - 100	0.025 - 0.05	5
AD208	1000 - 2000	1 - 1000	0.015 - 0.03	0.4 - 4
AD210	3500	1 - 100	0.012 - 0.025	20

Figure 1.99

Optical isolators using optical fibers may be made with isolation voltages of tens of MV. More general purpose devices consist of an LED and a photocell, electrically isolated but in a single DIL package, and having a breakdown voltage in the range 3.5 - 10 kV. The coupling between the two elements is not linear, so they cannot be used in simple analog isolation amplifiers, although they will carry digital signals and hence the results of A-D or V-F conversion very efficiently.

FOR HIGHER VOLTAGE BARRIERS USE OPTO-ISOLATORS

- Uses Light for Transmission Over a High Voltage Barrier
- An LED is the Transmitter, and a Photodiode or Phototransistor is the Receiver
- High Voltage Isolation is in the Range of 5000V to 7000V
- Usually Not Linear -- Best for Digital or Frequency Information

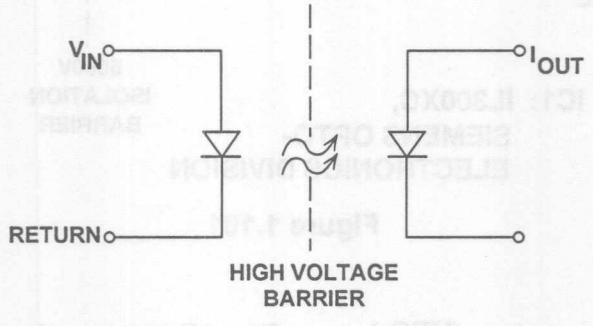


Figure 1.100

The Siemens IL300XC is an opto-coupler which contains two carefully matched photodetectors (they are actually matched at a sensitivity ratio of 0.7:1). By using one in a feedback system it is possible to linearize the response of the other when it is used as an isolation element. The linearity of such a system depends on accuracy of the matching of the photodetectors, and an optical design which ensures that both photodetectors receive the same amount of light from the LED.

Figure 1.101 shows an isolated temperature measuring scheme using such a device. The TMP-01 has a voltage output of 5 mV/K. Between -40° and +85°C its output is 1.16 - 1.8 V. This output voltage is applied to R1, and negative feedback in the OP-90 forces a current through the LED of the IL300XC such that a current flows in detector D1 to force pin 2 of the OP-90 to 2.5 V. Since D1 and D2 are matched at a ratio of 0.7:1 and operating in similar circuitry, 0.7 times this current

will flow in D2 and, as resistor R1 is 0.7 times the feedback resistor R2 (which may be trimmed for exact calibration), the output of the second OP-90 will be equal to the output of the TMP-01. The circuit is simple and uses a single +5 V supply. The TMP-01 may be replaced with other voltage sources <2.5 V.

HIGH VOLTAGE ISOLATION USING SINGLE-SUPPLY

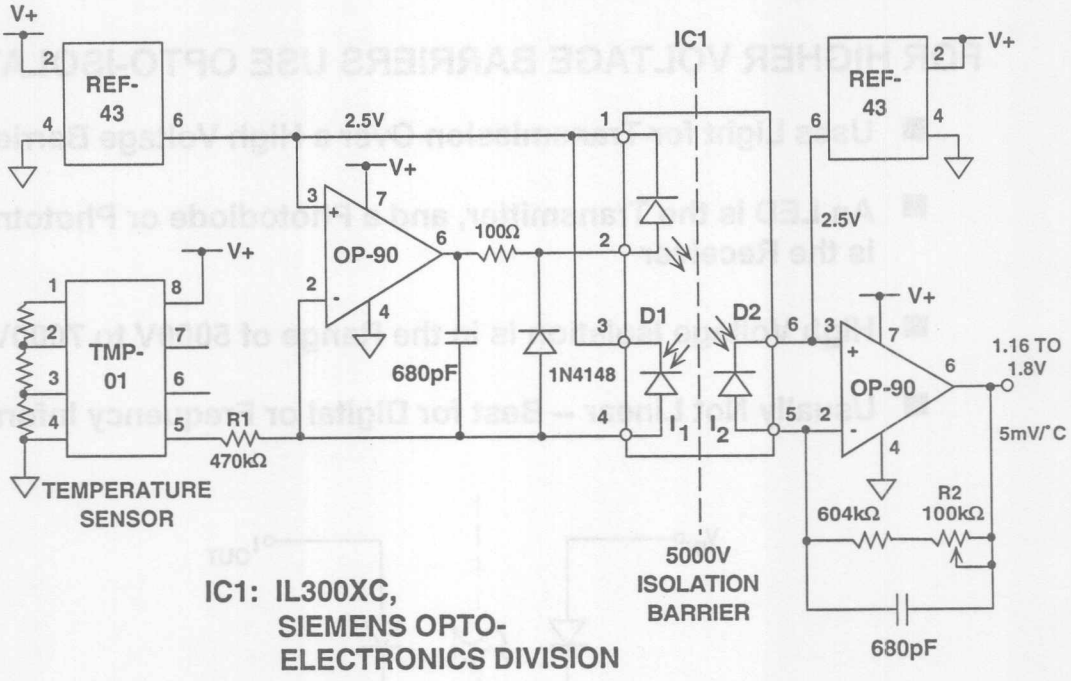


Figure 1.101

Voltage-Frequency Converters (VFCs) are valuable in systems requiring isolation. The analog signal is converted to a frequency in a VFC and may then be transmitted across an isolation barrier by very simple means with no risk of non-linearity and greatly reduced susceptibility to noise. At the receiver there are two options: the signal may be applied to a counter for a fixed period and the count read by a digital processor, the combination of VFC and counter acting as an ADC, or the frequency may be converted back to a voltage in a Frequency-Voltage Converter (FVC). FVCs are quite simple circuits and may generally be built with VFC ICs. (Reference 19)

The AD650 is a charge-balance VFC which is well suited for use in isolated VFC applications (Figure 1.103). The input to the AD650 charges a capacitor in an integrator. When the integrator output pass a threshold it fires a precision monostable (one-shot) which switches an accurate 1 mA current source into the integrator for a precisely-timed interval, removing a precise amount of charge from the integrator. It is obvious that the rate at which the monostable fires (which is the output frequency) is proportional to the current flows into the integrator, and hence to the voltage at the input terminal.

ISOLATION USING VOLTAGE-TO-FREQUENCY (V/F) CONVERTERS

- Converts A DC Voltage to a Frequency
- Frequency Information is Immune to Offsets and Noise
- V/F Output Can Be Transmitted Over Non-Linear Transmission Media
- Long Distance Transmission Over Twisted Pair or Fiber Optic Links
- A Frequency-to-Voltage (F/V) Converteris Used as the Receiver
- Accuracy is Determined by the V/F and F/V Conversion Process

Figure 1.102

THE AD650 CONNECTED AS A V/F CONVERTER

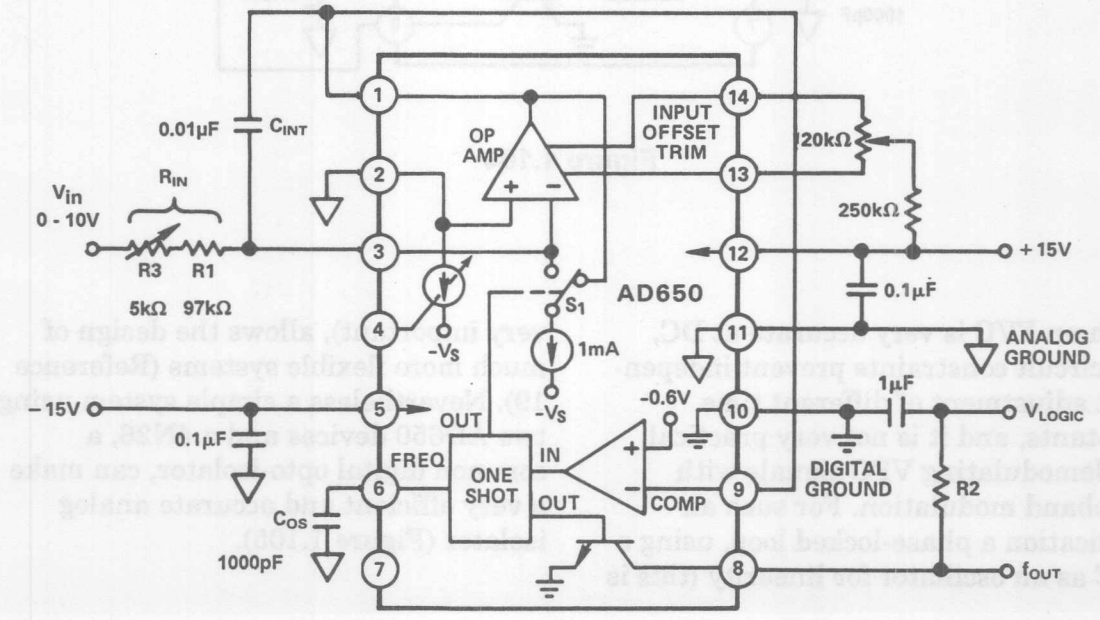


Figure 1.103

If the integrator of an AD650 is configured as a "leaky integrator" by connecting a resistor in parallel with the integration capacitor, and a pulse train is applied to the comparator to fire the precision monostable then the circuit will behave as an FVC: the more often the monostable fires the faster charge must leak out of the integration capacitor, and hence the larger the voltage on the integrator (see Figure 1.104).

THE AD650 CONNECTED AS AN F/V CONVERTER

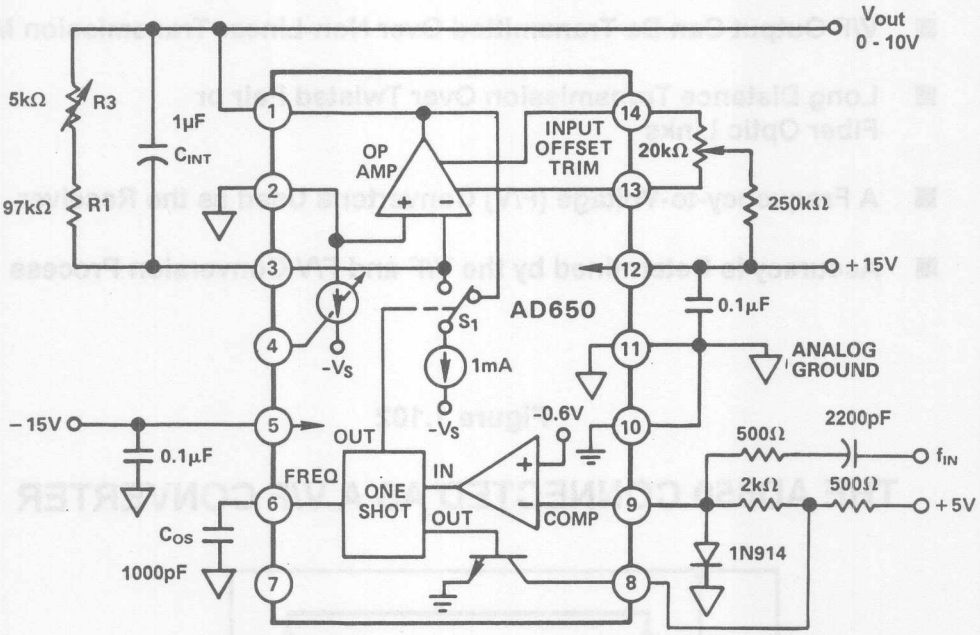


Figure 1.104

Such an FVC is very accurate at DC, but circuit constraints prevent independent adjustment of different time constants, and it is not very practical for demodulating VFC signals with wideband modulation. For such an application a phase-locked loop, using a VFC as an oscillator for linearity (this is very important), allows the design of much more flexible systems (Reference 19). Nevertheless a simple system using two AD650 devices and a 4N26, a common digital opto-isolator, can make a very efficient and accurate analog isolator (Figure 1.105).

AD650 IN A V/F, F/V OPTO-ISOLATED SYSTEM

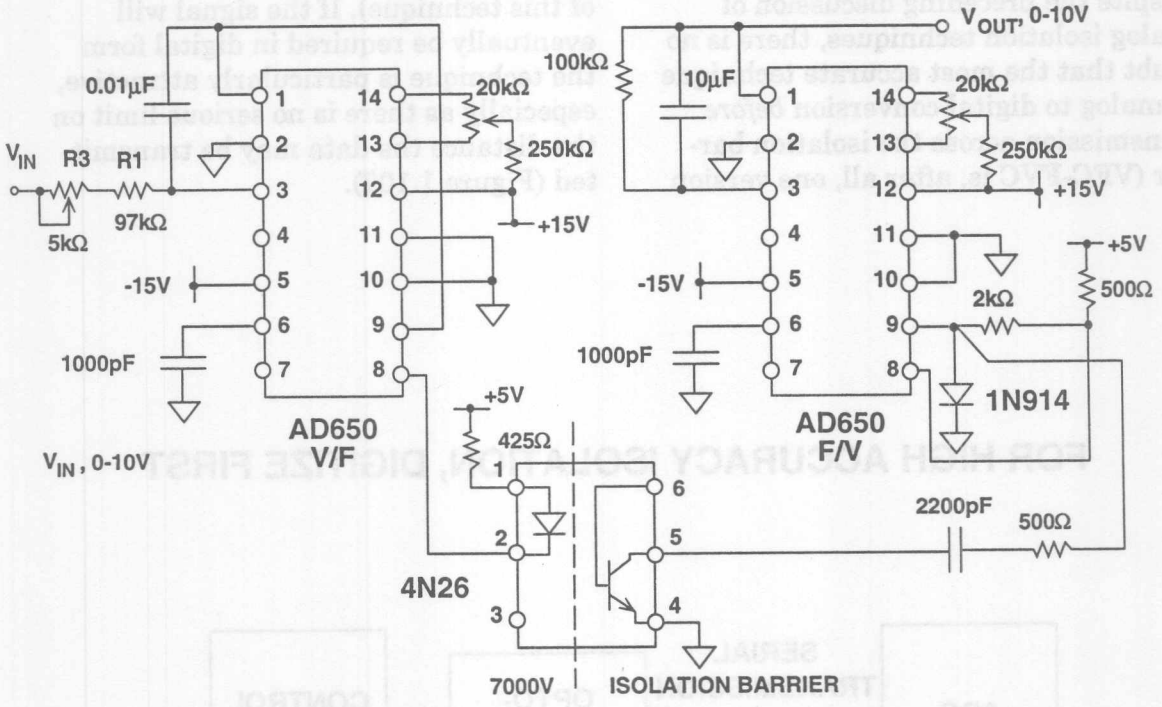


Figure 1.105

The accuracy of this circuit depends on the accuracy of the VFC and FVC conversions - the opto-isolator is not involved. Figure 1.106 shows the measured linearity of a prototype of the circuit, which is 0.006%, or better than 12-bits.

V/F, F/V LINEARITY

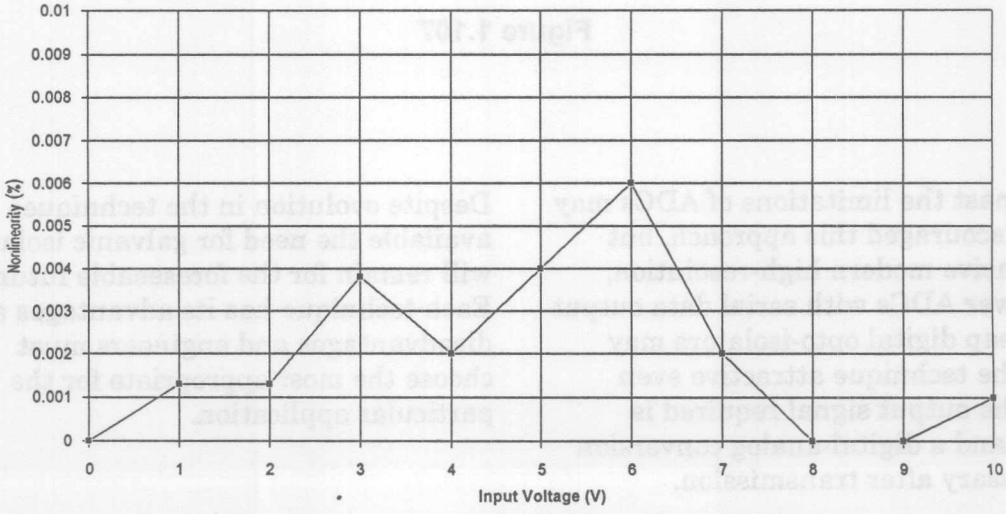
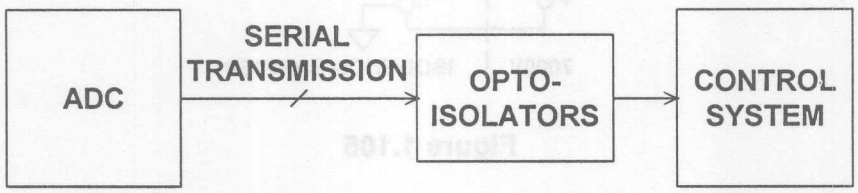


Figure 1.106

Despite the preceding discussion of analog isolation techniques, there is no doubt that the most accurate technique is analog to digital conversion *before* transmission across the isolation barrier (VFC-FVC is, after all, one version of this technique). If the signal will eventually be required in digital form the technique is particularly attractive, especially as there is no serious limit on the distance the data may be transmitted (Figure 1.107).

FOR HIGH ACCURACY ISOLATION, DIGITIZE FIRST



- Accuracy Limited Only By ADC
- Digital Transmission Relatively Immune To Noise

Figure 1.107

In the past the limitations of ADCs may have discouraged this approach, but inexpensive modern high-resolution, low-power ADCs with serial data output and cheap digital opto-isolators may make the technique attractive even when the output signal required is analog and a digital-analog conversion is necessary after transmission.

Despite evolution in the techniques available the need for galvanic isolation will remain for the foreseeable future. Each technique has its advantages and disadvantages and engineers must choose the most appropriate for the particular application.

ISOLATING TRANSDUCERS SUMMARY

TECHNOLOGY	ADVANTAGES	DISADVANTAGES
AD20x-Family Transformer Coupled	Fully Self-Contained 3-Port Isolation High Linearity Wide Bandwidth (20kHz)	Lower Breakdown Voltage
Opto-Isolators	High Voltage Immunity	Separate Power Needed External Amplifiers Required Poor Linearity
V/F and F/V Isolation	High Linearity Long Distance Transmission High Noise Immunity	Separate Power Needed DC Inputs Only
Digitize First	Highest Accuracy Best Linearity High Noise Immunity Long Distance Transmission	Separate Power Needed

Figure 1.108

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SECTION 2

MULTIPLEXING SIGNALS WITH ANALOG SWITCHES

- PARASITIC LATCHUP
- THE ANATOMY OF THE ANALOG SWITCH
- TRENCH-ISOLATED LC^{2}MOS ANALOG SWITCH FAMILY OFFERS MANY BENEFITS
- APPLYING THE ANALOG SWITCH

SECTION 2

MULTIPLEXING SIGNALS WITH ANALOG SWITCHES, *James Wong, Jerry Whitmore*

Analog signals can be switched, multiplexed, and easily connected using analog switches. With sufficient care there will be little or no degradation of signal quality. This section is devoted to CMOS technology in analog switch circuitry, their parasitic latchup mechanisms, and effective protection methods. It also discusses AC switch characteristics and how they affect the performance of a system, and some application circuits.

MULTIPLEXING CONCEPTS

- Advantages of CMOS Technology in Analog Switch Circuitry
- Parasitic Transistors/Latchup and Protection Methods
- Switch Equivalent Circuit dc and ac Analysis
- Applying the Analog Switch

Figure 2.1

The ideal analog switch has no ON-resistance, infinite OFF impedance and zero time delay, and can handle large signal and common-mode voltages. Real CMOS analog switches meet none of these criteria, but if we understand the limitations of analog switches, most of these limitations can be overcome.

CMOS switches have an excellent combination of attributes. In its most basic form, the MOSFET transistor is a voltage-controlled resistor. In the ON state, its resistance can be less than 100Ω, while in the OFF-state, the resistance increases to several hundreds of megohms, with nanoamp leakage currents.

CHARACTERISTICS OF THE IDEAL ANALOG SWITCH

- On Resistance: Zero
- Off Impedance: Infinite at All Frequencies
- Switching Time: Zero
- Switch Leakage: Zero
- Power Dissipation: Zero
- MTBF: Infinite

Figure 2.2

CMOS technology is compatible with logic circuitry and can be densely packed in an IC. Its fast switching characteristics are well controlled with minimum circuit parasitics.

MOSFET transistors are bilateral. That is, they can switch positive and negative voltages and conduct positive and negative currents with equal ease.

ADVANTAGES OF MIXED SIGNAL CMOS TECHNOLOGY

- A Great Logic Technology
  - High Density
  - Moderate to High Speed
  - Low Power Dissipation
- An Excellent Switch Technology
  - MOSFETs are Voltage Controlled Resistors
  - MOSFETs Lose No Current to the Control Input (Gate)
  - MOSFETs are Electrically Bilateral -- Can Switch Positive or Negative Voltages or Steer Positive or Negative Current with Equal Ease
  - No Offset Voltage in Series With ON MOSFET (Unlike Bipolar Transistor)

Figure 2.3

A MOSFET transistor has a voltage controlled resistance which varies nonlinearly with signal voltage as shown in Figure 2.4. Figure 2.5 shows a basic CMOS switch using complementary P-channel and N-channel MOS devices connected in parallel. This reduces the ON-resistance and also produces a resistance which varies less with signal voltage.

MOSFET SWITCH ON-RESISTANCE VERSUS SIGNAL VOLTAGE

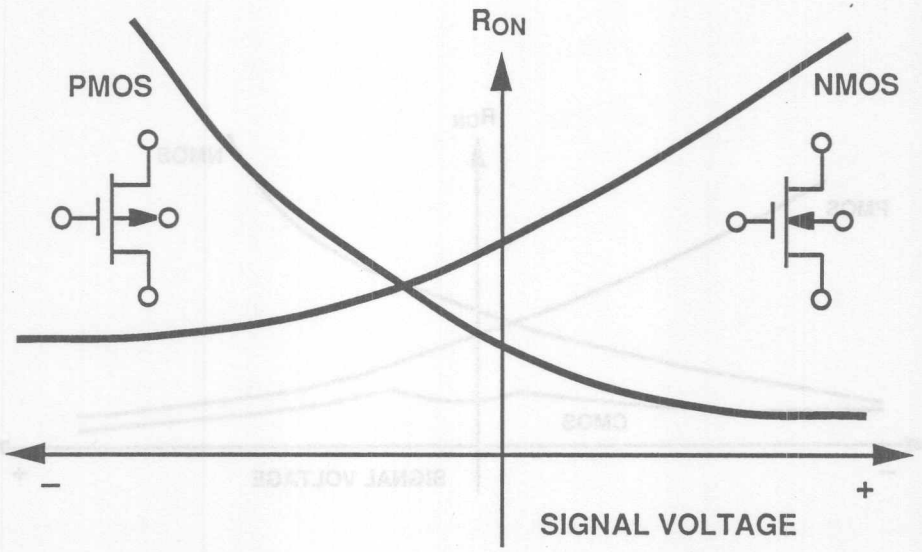


Figure 2.4

BASIC CMOS SWITCH USES COMPLEMENTARY PAIR TO MINIMIZE Ron VARIATION DUE TO INPUT SIGNAL SWING

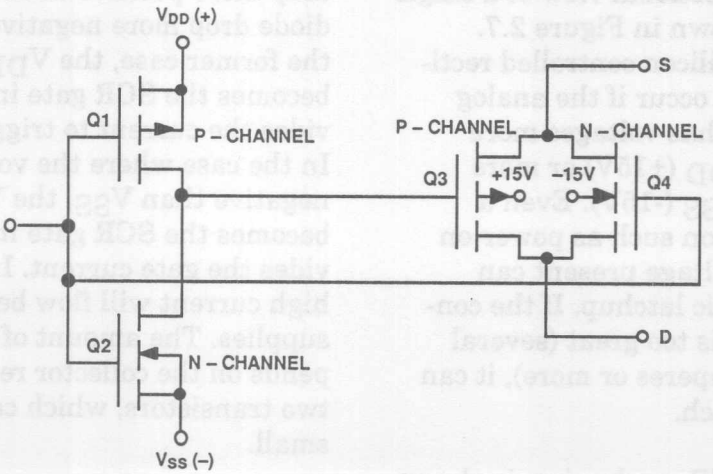


Figure 2.5

Figure 2.6 shows the ON-resistance changing with channel voltage for both N-type and P-type devices. This nonlinear resistance can causes errors in DC accuracy as well as AC distortion. The bilateral CMOS switch solves this problem. ON-resistance is minimized and its linearity is also improved. The bottom curve (Figure 2.6) shows the improved flatness of the ON-resistance characteristic of the switch.

CMOS SWITCH ON-RESISTANCE VERSUS SIGNAL VOLTAGE

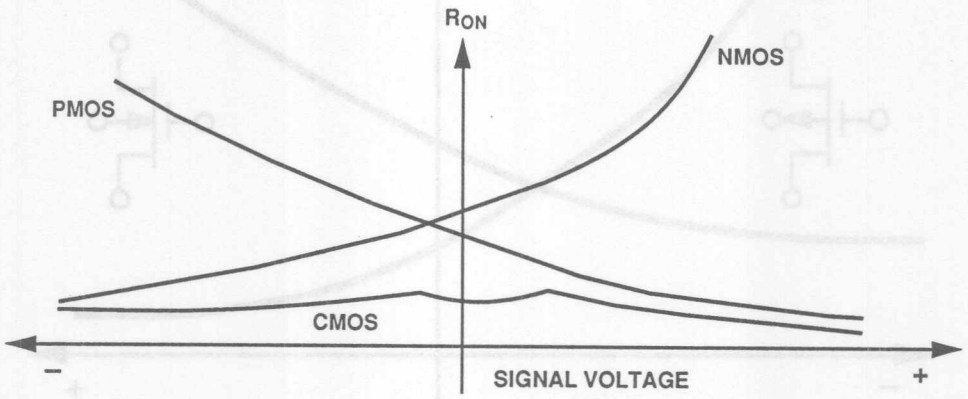


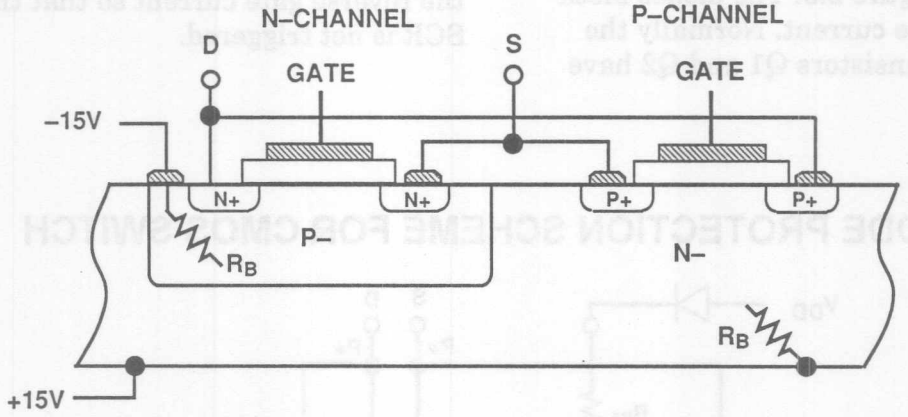
Figure 2.6

PARASITIC LATCHUP

Most CMOS analog switches are built using junction-isolated CMOS processes. A cross-sectional view of a single switch cell is shown in Figure 2.7. Parasitic SCR (silicon controlled rectifier) latchup can occur if the analog switch terminal has voltages more positive than V_{DD} (+15V) or more negative than V_{SS} (-15V). Even a transient situation such as power-on with an input voltage present can trigger a parasitic latchup. If the conduction current is too great (several hundred milliamperes or more), it can damage the switch.

The parasitic SCR mechanism is shown in Figure 2.8. SCR action takes place when either terminal of the switch (source or the drain) is either one diode drop more positive than V_{DD} or one diode drop more negative than V_{SS}. In the former case, the V_{DD} terminal becomes the SCR gate input and provides the current to trigger SCR action. In the case where the voltage is more negative than V_{SS}, the V_{SS} terminal becomes the SCR gate input and provides the gate current. In either case, high current will flow between the supplies. The amount of current depends on the collector resistances of the two transistors, which can be fairly small.

CROSS SECTION OF JUNCTION-ISOLATED CMOS SWITCH



- Problems Occur if Voltages More Positive Than V_{dd} or More Negative than V_{ss} are Applied to an Analog Switch Terminal

Figure 2.7

BIPOLAR TRANSISTOR EQUIVALENT CIRCUIT OF CMOS SWITCH SHOWS PARASITIC ACTION (A CLASSIC SCR LATCH)

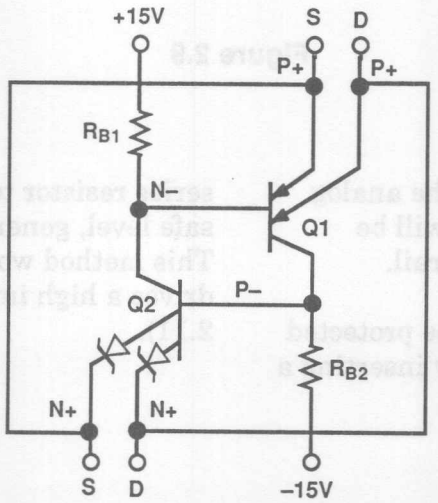
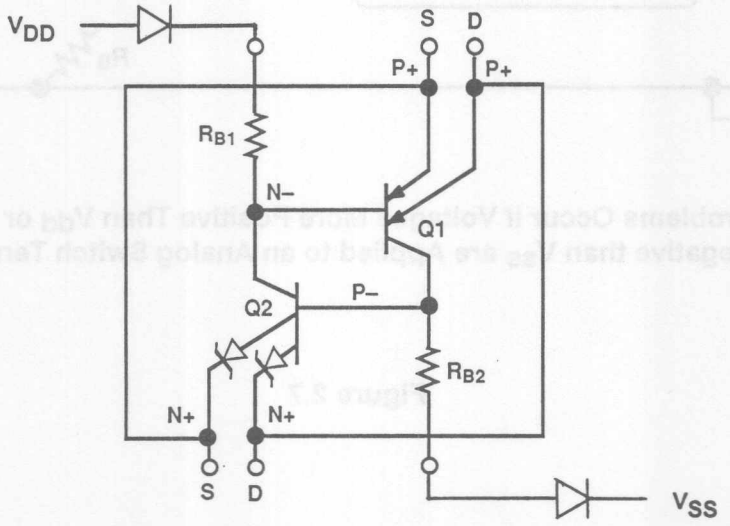


Figure 2.8

In order to prevent this type of SCR latchup, a series diode can be inserted into the V_{DD} and V_{SS} terminals as shown in Figure 2.9. The diodes block the SCR gate current. Normally the parasitic transistors Q1 and Q2 have low beta (usually less than 10) and require a comparatively large gate current to fire the SCR. The diodes limit the reverse gate current so that the SCR is not triggered.

DIODE PROTECTION SCHEME FOR CMOS SWITCH



■ Protection Diodes CR1 and CR2 Block Base Current Drive to Q1 and Q2 in Event of Overvoltage at S or D

Figure 2.9

If diode protection is used, the analog voltage range of the switch will be reduced by one V_{be} at each rail.

Analog switches must also be protected from possible overcurrent by inserting a series resistor to limit the current to a safe level, generally less than 25mA. This method works only if the switch drives a high impedance load (Figure 2.11).

PROTECTING CMOS SWITCH / MUX FROM LATCHUP USING DIODES

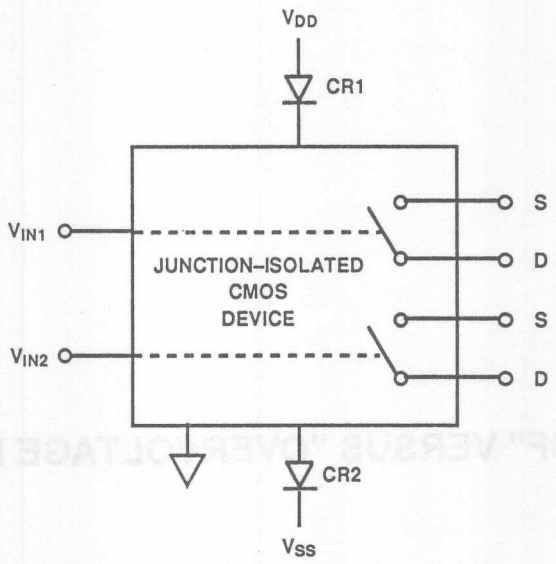
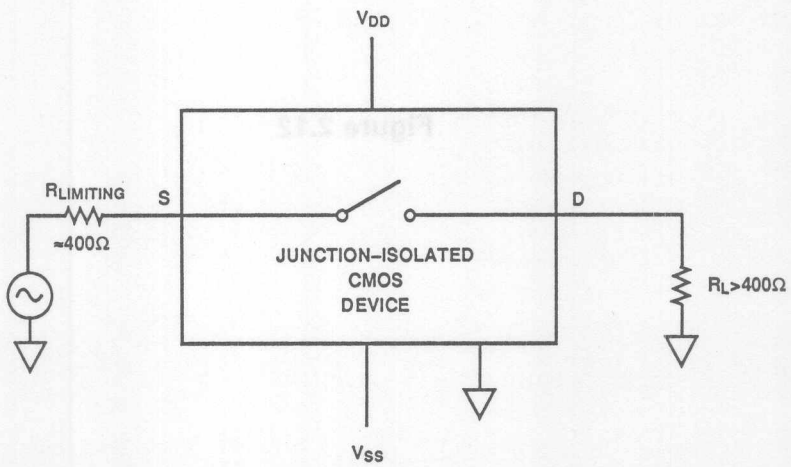


Figure 2.10

PROTECTING CMOS SWITCH / MUX FROM OVERCURRENT



- External Resistor Limits Current to Safe Value

Figure 2.11

Latchup protection and overcurrent protection schemes are mutually exclusive. If both fault conditions can exist in a system, then both protection protective diodes and resistors should be used.

"LATCHPROOF" VERSUS "OVERVOLTAGE PROTECTED"

- *Latchproof* only means the device won't go into an SCR mode.
- It does not guarantee *Overvoltage Protection*.

Figure 2.12

THE ANATOMY OF THE ANALOG SWITCH

It is important to understand the error sources in an analog switch. Many affect AC and DC performance, while others only affect AC. Figure 2.13 shows the equivalent circuit of two adjacent switches. It includes leakage currents and junction capacitances.

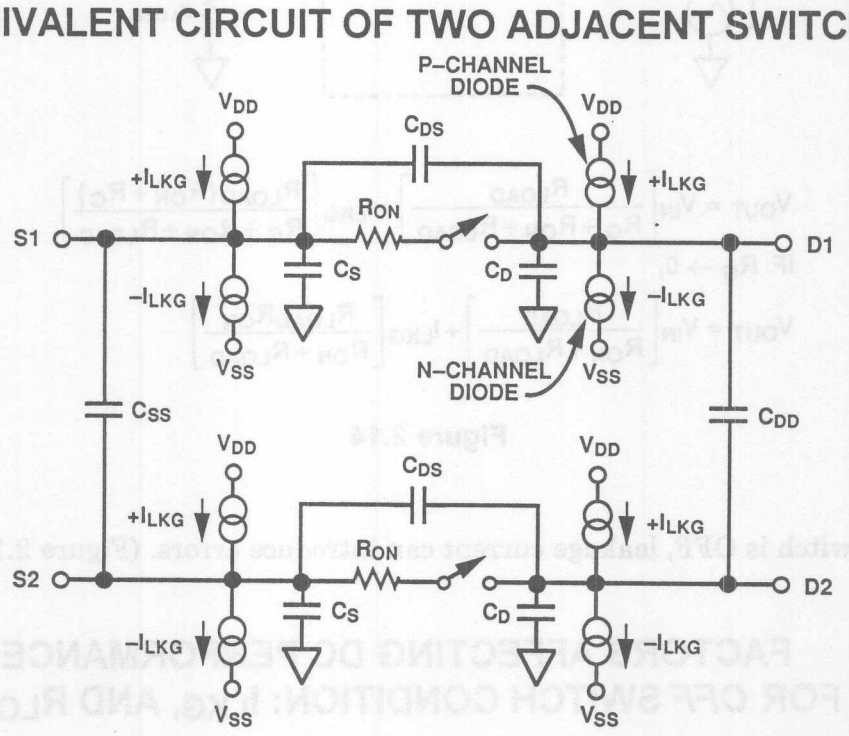
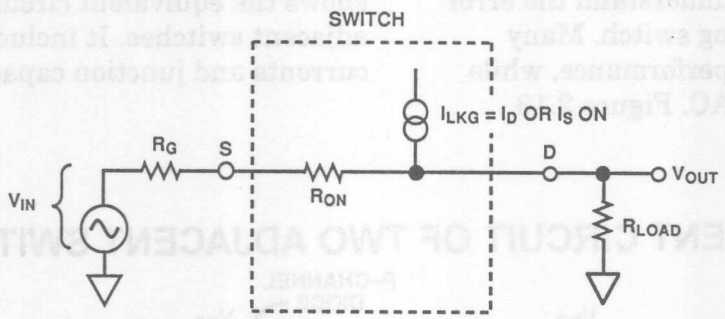


Figure 2.13

DC performance is affected mainly by the switch ON-resistance (R_{ON}) and leakage. Low resistance circuits are more subject to errors due to R_{ON} while high resistance circuits are affected by leakage currents. Figure 2.14 shows how these parameters affect DC performance.

FACTORS AFFECTING DC PERFORMANCE FOR *ON* SWITCH CONDITION: R_{ON}, R_{LOAD}, AND I_{LKG}



$$V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_G + R_{ON} + R_{LOAD}}\right] + I_{LKG}\left[\frac{R_{LOAD}(R_{ON} + R_G)}{R_G + R_{ON} + R_{LOAD}}\right]$$

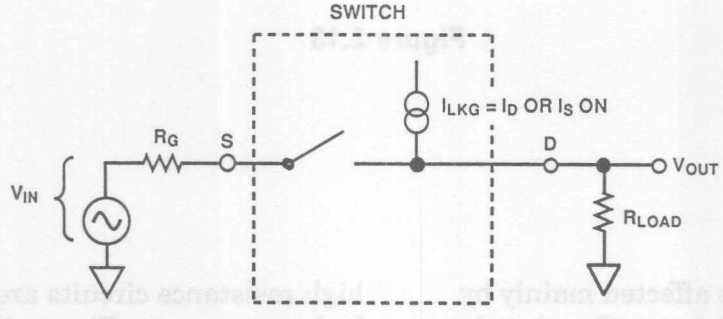
IF $R_G \rightarrow 0$,

$$V_{OUT} = V_{IN}\left[\frac{R_{LOAD}}{R_{ON} + R_{LOAD}}\right] + I_{LKG}\left[\frac{R_{LOAD}R_{ON}}{R_{ON} + R_{LOAD}}\right]$$

Figure 2.14

When the switch is OFF, leakage current can introduce errors. (Figure 2.15)

FACTORS AFFECTING DC PERFORMANCE FOR *OFF* SWITCH CONDITION: I_{LKG}, AND R_{LOAD}



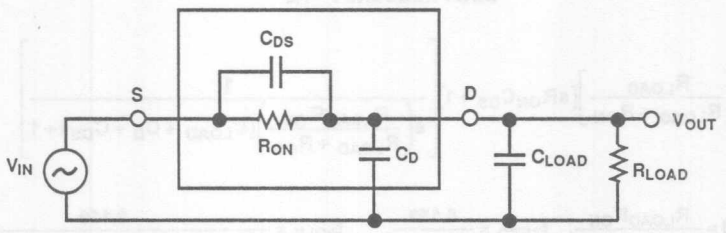
- Leakage Current Creates Error Voltage at V_{OUT} Equal to:

$$V_{OUT} = I_{LKG} \times R_{LOAD}$$

Figure 2.15

Figure 2.16 illustrates the parasitic components that affect the AC performance of CMOS switches. Additional external capacitances will further degrade performance. These capacitances affect feedthrough, crosstalk and system bandwidth.

DYNAMIC PERFORMANCE CONSIDERATIONS: TRANSFER ACCURACY VERSUS FREQUENCY



$$A(s)=\left[\frac{R_{LOAD}}{R_{LOAD}+R_{ON}}\right]\left[\frac{sR_{ON}C_{DS}+1}{s\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD}+R_{ON}}\right)(C_{LOAD}+C_D+C_{DS})+1}\right]$$

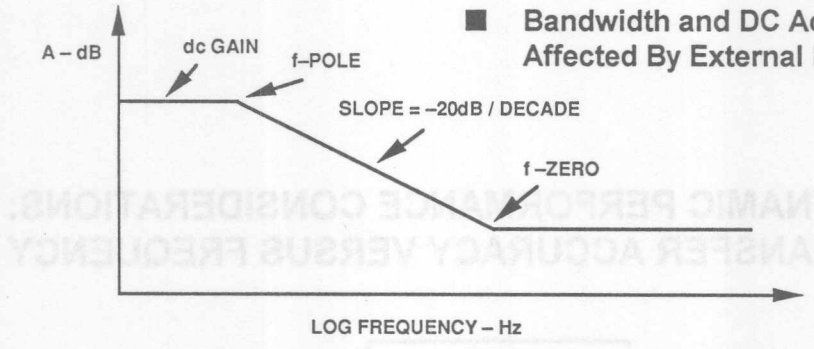
$$A(dB)=20\log\left[\frac{R_{LOAD}}{R_{LOAD}+R_{ON}}\right]+10\log\left[\omega^2(R_{ON}C_{DS})^2+1\right]-10\log\omega^2\left[\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD}+R_{ON}}\right)^2(C_{LOAD}+C_D+C_{DS})^2+1\right]$$

Figure 2.16

The signal transfer characteristic is dependent on the switch channel capacitance, C_{DS}. This capacitance creates a frequency zero in the numerator of the transfer function A(s). This zero usually occurs at high frequencies because the switch ON resistance is small. The bandwidth is also a function of the switch output capacitance in combination with C_{DS} and the load capacitance. This frequency pole appears in the denominator of the equation.

The composite frequency domain transfer function may be re-written as shown in Figure 2.17. In most cases, the pole breakpoint frequency occurs first because of the dominant effect of the output capacitance C_D. Thus, to maximize bandwidth a switch must have low input and output capacitance and low ON resistance.

DYNAMIC PERFORMANCE CONSIDERATIONS: TRANSFER ACCURACY VERSUS FREQUENCY



■ Bandwidth and DC Accuracy is Affected By External R and C

$$A(s) = \left[\frac{R_{LOAD}}{R_{LOAD} + R_{ON}}\right][sR_{ON}C_{DS} + 1]\left[\frac{1}{s\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}}\right)(C_{LOAD} + C_D + C_{DS}) + 1}\right]$$

$$\text{DC GAIN} = \frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}}, \quad f_{ZERO} = \frac{0.159}{R_{ON}C_{DS}}, \quad f_{POLE} = \frac{0.159}{\left(\frac{R_{LOAD}R_{ON}}{R_{LOAD} + R_{ON}}\right)(C_{LOAD} + C_D + C_{DS})}$$

Figure 2.17

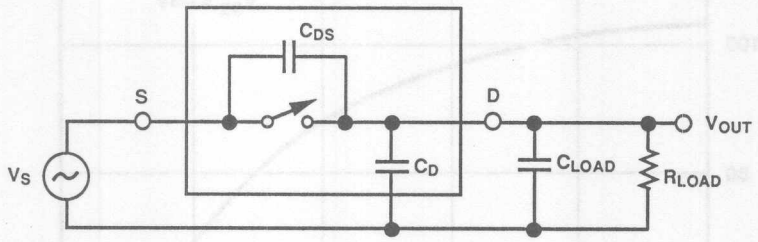
The series-pass capacitance, C_{DS}, not only creates a zero in the response in the ON-state, it degrades the feedthrough performance of the switch during its OFF state. When the switch is off, C_{DS} couples the input signal to the output load. (Figure 2.18)

Large values of C_{DS} will produce large values of feedthrough, proportional to the input frequency. Figure 2.19 illustrates the drop in OFF-isolation as a function of frequency. The simplest way to maximize the OFF-isolation is to choose a switch that has as small a C_{DS} as possible.

Figure 2.20 shows typical CMOS analog switch OFF-isolation as a function of frequency. From DC to several kilohertz, the switch has over 100dB isolation. As the frequency increases, an increasing amount of signal reaches the output. However, even at 1MHz, the switch still has nearly 70dB of isolation.

DYNAMIC PERFORMANCE CONSIDERATIONS: OFF ISOLATION

- OFF Isolation is Affected by External R and C Load



$$A(s) = \frac{s(R_{LOAD})(C_{DS})}{s(R_{LOAD})(C_{LOAD} + C_D + C_{DS}) + 1}$$

Figure 2.18

DYNAMIC PERFORMANCE CONSIDERATIONS: *OFF* ISOLATION VERSUS FREQUENCY

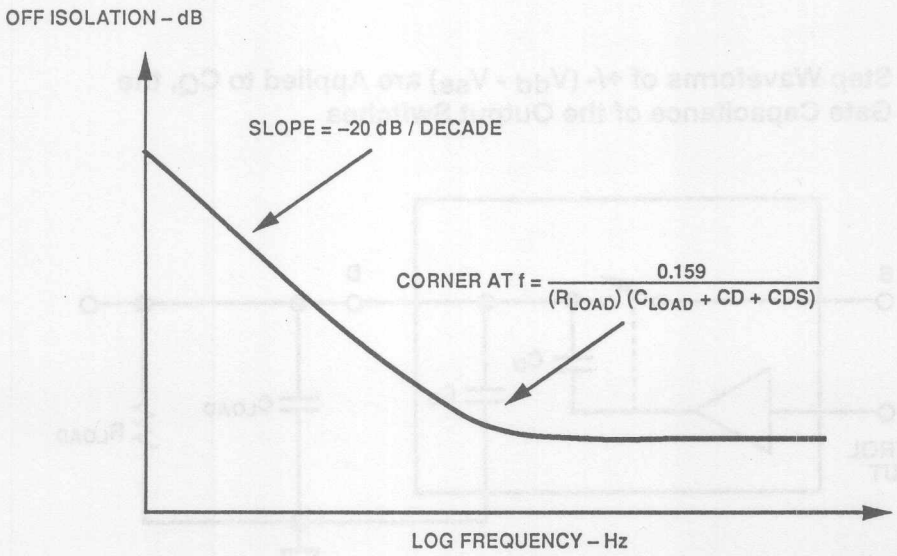


Figure 2.19

TYPICAL CMOS SWITCH *OFF* ISOLATION PERFORMANCE (ADG511/ADG512)

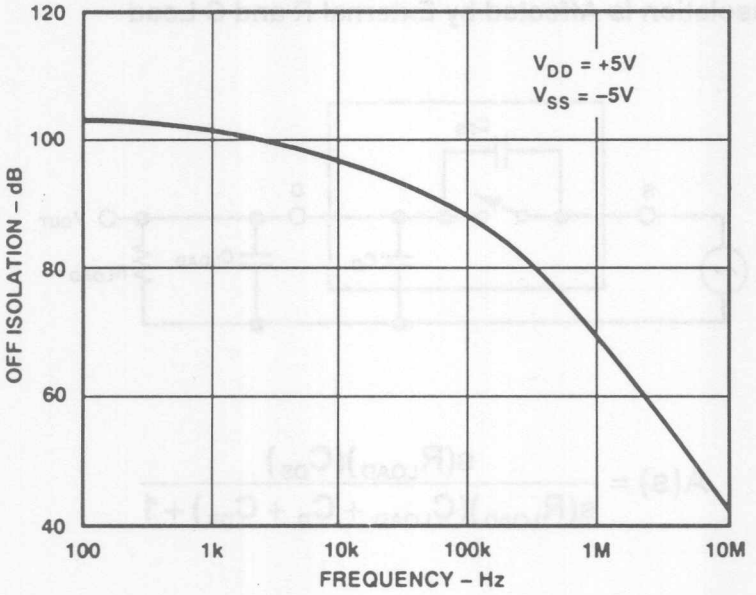


Figure 2.20

DYNAMIC PERFORMANCE CONSIDERATIONS: CHARGE INJECTION MODEL

- Step Waveforms of +/- (V_{dd} - V_{ss}) are Applied to C_Q, the Gate Capacitance of the Output Switches

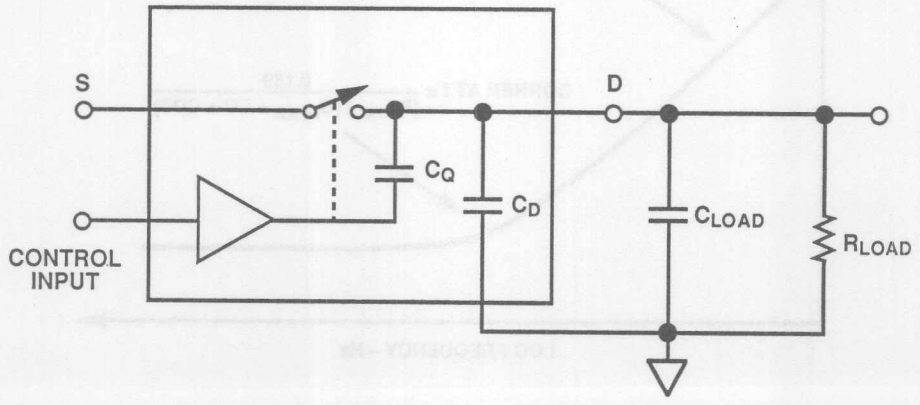


Figure 2.21

Another AC parameter that affects system performance is the charge injection that takes place during switching. Figure 2.21 shows the equivalent circuit of the charge injection mechanism.

When the switch control input is asserted, it causes the control circuit to apply a large voltage change (from V_{DD} to V_{SS}, or vice versa) at the gate of the MOSFET switch. This fast change in voltage injects a charge into the switch output through the gate-drain capacitance C_Q. The amount of charge coupled depends on the gate-drain capacitance.

The charge injection introduces a step change in output voltage when switching (refer to Figure 2.22). The change in voltage is a function of the amount of charge injected, which is in turn a function of the gate-drain capacitance.

Another problem caused by switch capacitance is the retained charge when channel switching which can cause transients in the switch output. Figure 2.23 illustrates the phenomenon.

EFFECTS OF CHARGE INJECTION

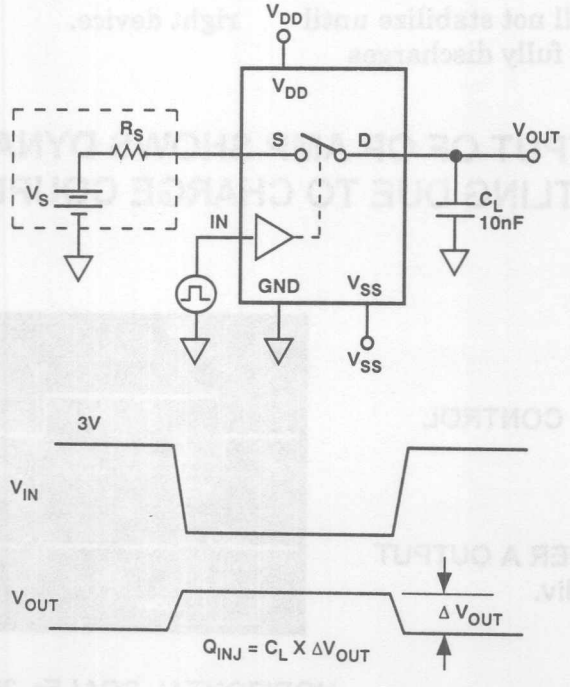


Figure 2.22

CHARGE COUPLING CAUSES DYNAMIC SETTLING NOISE WHEN MULTIPLEXING SIGNALS

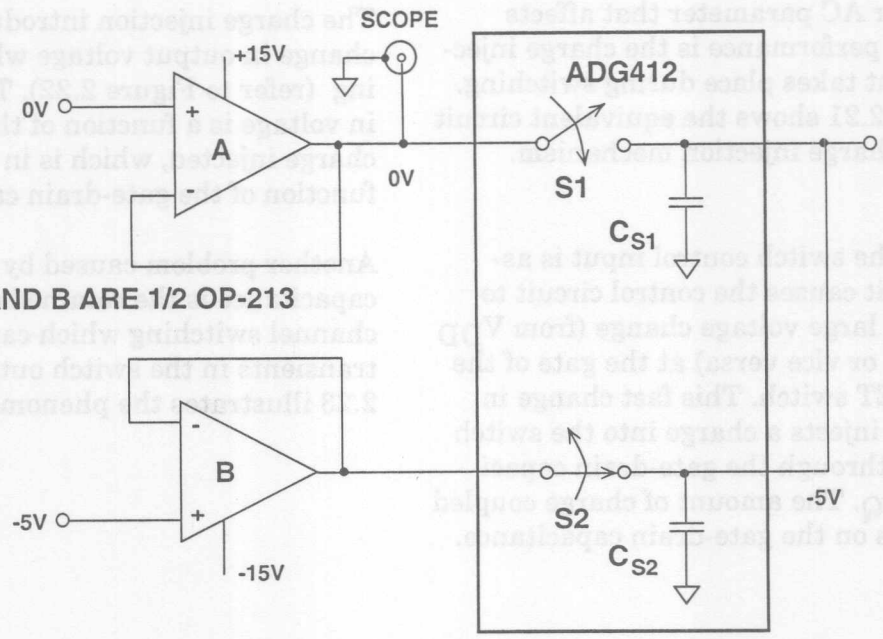


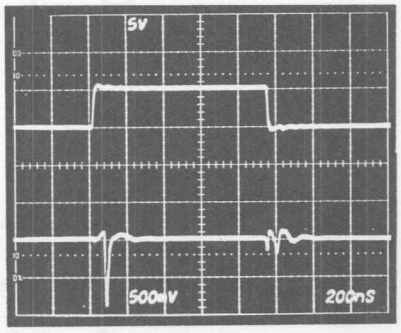
Figure 2.23

Assume that initially S2 is closed and S1 open. C_{S1} and C_{S2} are charged to -5V. As S2 opens, the -5V remains on C_{S1} and C_{S2}, as S1 closes. Thus the output of Amplifier A sees a -5V transient. The output will not stabilize until Amplifier A's output fully discharges C_{S1} and C_{S2} and settles to 0V. The scope photo in Figure 2.24 depicts this transient. The amplifier's transient load settling characteristics will be an important consideration when choosing the right device.

OUTPUT OF OP AMP SHOWS DYNAMIC SETTLING DUE TO CHARGE COUPLING

SWITCH CONTROL
5V/div.

AMPLIFIER A OUTPUT
500mV/div.



HORIZONTAL SCALE: 200ns/div.

Figure 2.24

Crosstalk is related to the capacitances between two switches. This is the C_{SS} shown in Figure 2.25.

CHANNEL-TO-CHANNEL CROSSTALK CONSIDERATION: EQUIVALENT CIRCUIT FOR ADJACENT SWITCHES

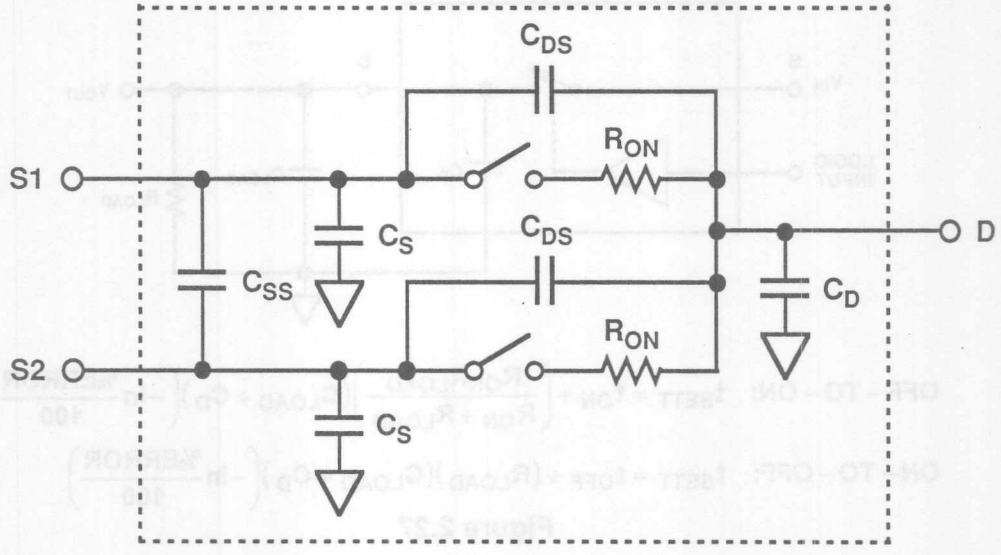


Figure 2.25

Figure 2.26 shows typical crosstalk performance of a CMOS analog switch.

CROSSTALK PERFORMANCE OF ADG511 SWITCH

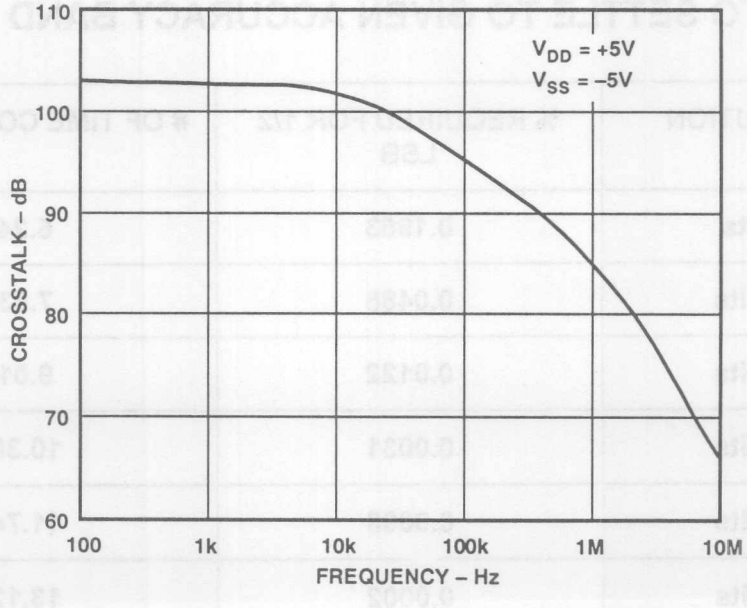
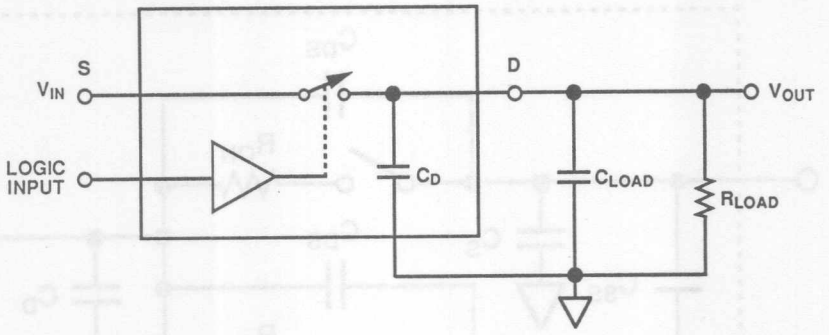


Figure 2.26

Finally, the switch itself has a settling time that must be considered. Figure 2.27 shows the dynamic transfer function.

DYNAMIC PERFORMANCE CONSIDERATIONS: SETTLING TIME

■ **Settling Time is the Time Required for the Switch Output Voltage to Settle to Within a Given Accuracy Band of the Final Value.**



$$\text{OFF-TO-ON:}\quad t_{SETT} = t_{ON} + \left(\frac{R_{ON}R_{LOAD}}{R_{ON}+R_{LOAD}}\right)(C_{LOAD}+C_D)\left(-\ln\frac{\%ERROR}{100}\right)$$

$$\text{ON-TO-OFF:}\quad t_{SETT} = t_{OFF} + (R_{LOAD})(C_{LOAD}+C_D)\left(-\ln\frac{\%ERROR}{100}\right)$$

Figure 2.27

The settling time can be calculated because the response is a function of the switch and circuit resistances and capacitances. One can assume that this is a single-pole system and calculate the number of time constants required to settle to the desired system accuracy (Figure 2.28).

NUMBER OF TIME CONSTANTS REQUIRED TO SETTLE TO GIVEN ACCURACY BAND

RESOLUTION	% REQUIRED FOR 1/2 LSB	# OF TIME CONSTANTS
8 Bits	0.1953	6.24
10 Bits	0.0488	7.63
12 Bits	0.0122	9.01
14 Bits	0.0031	10.38
16 Bits	0.0008	11.74
18 Bits	0.0002	13.12

Figure 2.28

TRENCH-ISOLATED LC²MOS ANALOG SWITCH FAMILY OFFERS MANY BENEFITS

Analog Devices uses trench-isolation technology to produce its LC²MOS analog switches. The process reduces the latchup susceptibility of the device, the junction capacitances, increases switching time and leakage current, and extends the analog voltage range to the supply rails.

ADG411/ADG511 FAMILY OF TRENCH-ISOLATED LC²MOS ANALOG SWITCHES

- Latch-Up Proof
- Analog Signal Range to Supply Rails
- Fast Switching Times
- Break Before Make Switching
- Low ON-Resistance
- Low Leakage

Figure 2.29

Figure 2.30 shows the cross-sectional view of the complementary CMOS structure. The buried oxide layer and the side walls completely isolate the substrate from each transistor junction. Therefore, no reverse-biased PN junction is formed. Consequently the bandwidth-reducing capacitances and the possibility of SCR latchup are greatly reduced.

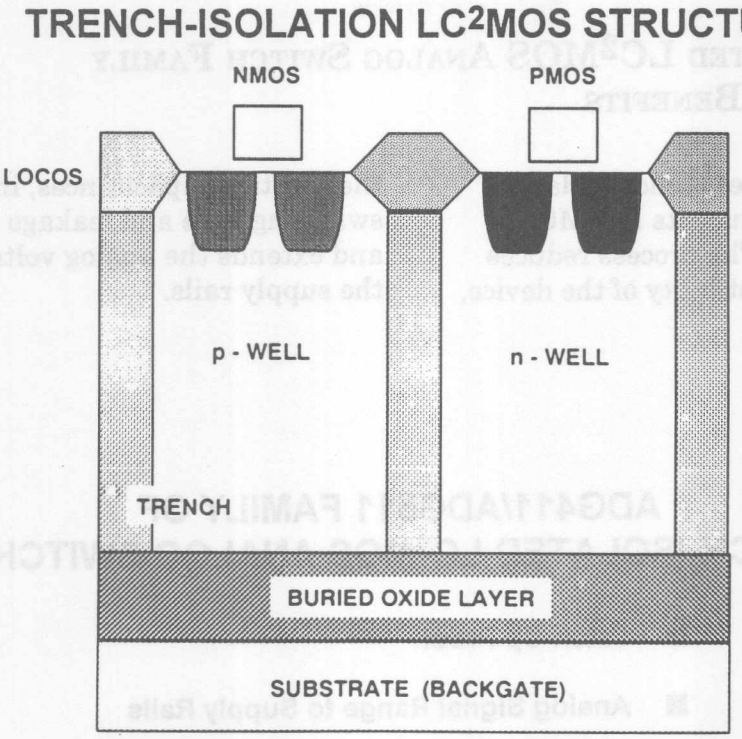


Figure 2.30

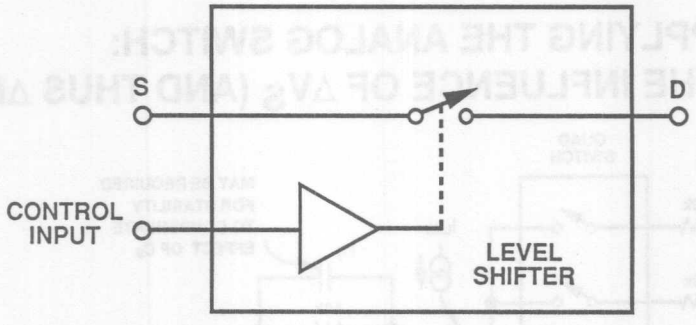
APPLYING THE ANALOG SWITCH

Switching time is an important consideration in applying analog switches, but switching time should not be confused with settling time. ON and OFF times are simply a measure of the propagation delay from the control input to the toggling of the switch and are largely caused by time delays in the drive and level-shift circuits.

When a CMOS multiplexer switches inputs to an inverting summing amplifier, it should be noted that the ON-resistance, as well as its nonlinear change as a function of input voltage, will cause errors (refer to Figure 2.32). If the resistors are large the switch leakage current may introduce error. Small resistors minimize leakage current error but increase the error due to the finite value of R_{ON}.

APPLYING THE ANALOG SWITCH: DYNAMIC PERFORMANCE CONSIDERATIONS

- t_{on} and t_{off} should not be confused with settling time.



- t_{on} and t_{off} are simply a measure of the propagation delay from control input to operation of the analog switch. It is caused by time delays in the drive / level-shifter logic circuitry.

Figure 2.31

APPLYING THE ANALOG SWITCH: UNITY GAIN INVERTER WITH SWITCHED INPUT

- Problem: Effect of ΔR_{ON} versus ΔV_S on Circuit Linearity.
- R_{ON} variation due to ΔV_{IN} degrades linearity of V_{OUT} relative to V_{IN}

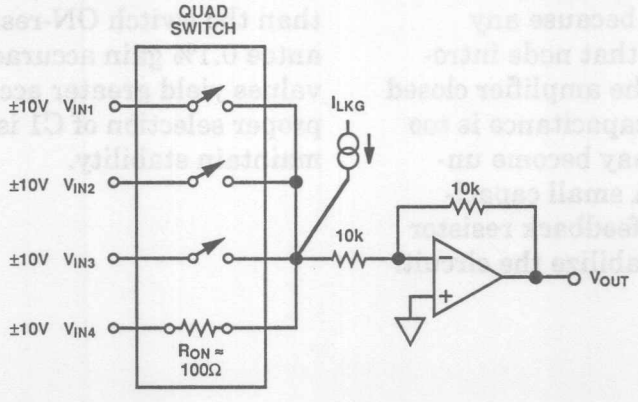
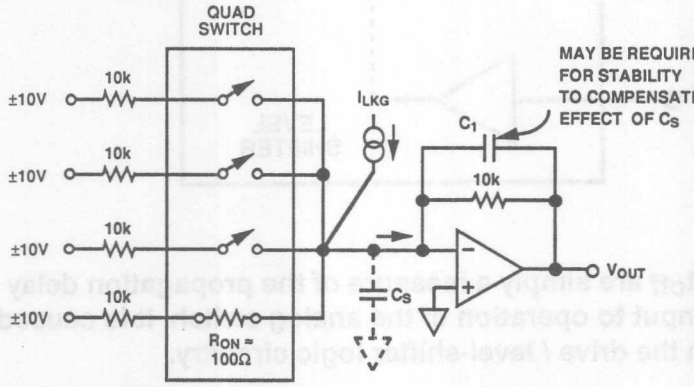


Figure 2.32

To minimize the effect of R_{ON} change due to the change in input voltage, it is advisable to put the multiplexing switches at the op amp summing junction as shown in Figure 2.33. This ensures the switches are only modulated with about ±100mV rather than the full ±10V - but a resistor is required for each input leg.

APPLYING THE ANALOG SWITCH: MINIMIZING THE INFLUENCE OF ΔV_S (AND THUS ΔR_{ON})



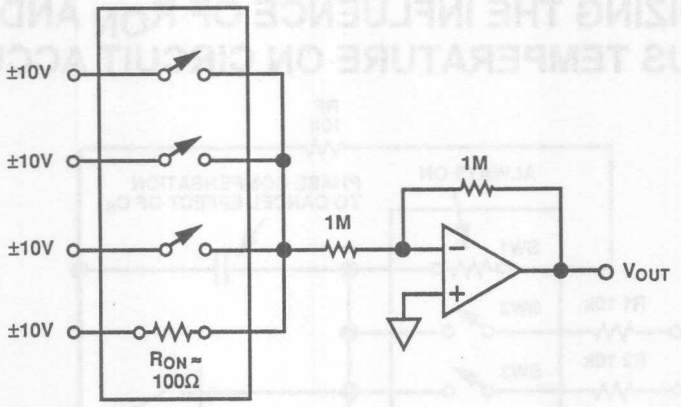
- Connecting the Switch at the Summing Point
- The switch only sees ± 100mV, not ± 10V. R_{ON} variation is minimized, and V_{OUT} accuracy is improved.

Figure 2.33

It is important to know how much parasitic capacitance has been added to the summing junction as a result of adding a multiplexer because any capacitance added to that node introduces phase shift to the amplifier closed loop response. If the capacitance is too large, the amplifier may become unstable and oscillate. A small capacitance, C1, across the feedback resistor may be required to stabilize the circuit.

The finite value of R_{ON} is a significant error source. The gain-set resistors should be at least 1,000 times larger than the switch ON-resistance to guarantee 0.1% gain accuracy. Higher values yield greater accuracy, but the proper selection of C1 is critical to maintain stability.

APPLYING THE ANALOG SWITCH: MINIMIZING THE INFLUENCE OF ΔV_S (AND THUS ΔR_{ON})

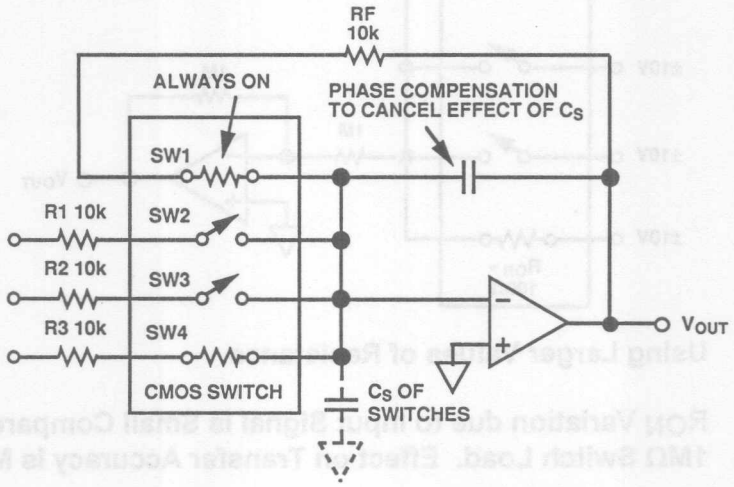


- Using Larger Values of Resistance
- R_{ON} Variation due to Input Signal is Small Compared to the 1MΩ Switch Load. Effect on Transfer Accuracy is Minimized.
- Bias Current and Leakage are now very important

Figure 2.34

A better method of compensating for R_{ON} is to place one of the switches in series with the feedback resistor of the inverting amplifier as shown in Figure 2.35. It is a safe assumption that the multiple switches, fabricated on a single chip, are well-matched in absolute characteristics and tracking over temperature. Therefore the amplifier closed loop gain stable at unity gain, since the total feedforward and feedback resistors are matched.

APPLYING THE ANALOG SWITCH: MINIMIZING THE INFLUENCE OF R_{ON} AND ΔR_{ON} VERSUS TEMPERATURE ON CIRCUIT ACCURACY



■ **Switch in Series With Feedback Resistor Compensates for Gain Error.**

Figure 2.35

The best multiplexer drives the non-inverting input of the amplifier. The high input impedance of the non-inverting input eliminates the errors due to R_{ON}. (Figure 2.36)

When multiplexing signals into an ADC, particularly the successive-approximation (SAR) type, it is advisable to place a buffer between the switch output and the input of the converter. The transient currents at the ADC input produced by the conversion process (DAC switching) are absorbed by a drive amplifier of sufficiently low output impedance and high bandwidth. Driving the ADC directly with the switches will produce significant conversion errors due to the finite R_{ON} resistance.

APPLYING THE ANALOG SWITCH: MINIMIZING THE INFLUENCE OF ΔV_S (AND THUS ΔR_{ON}) NON-INVERTING SOLUTION

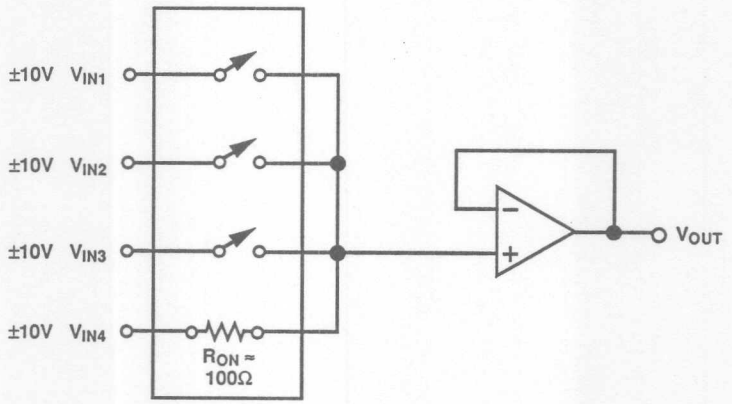


Figure 2.36

APPLYING THE ANALOG SWITCH: BUFFER THE MUX OUTPUT INTO AN ADC TO MINIMIZE GAIN ERROR AND PROVIDE ISOLATION

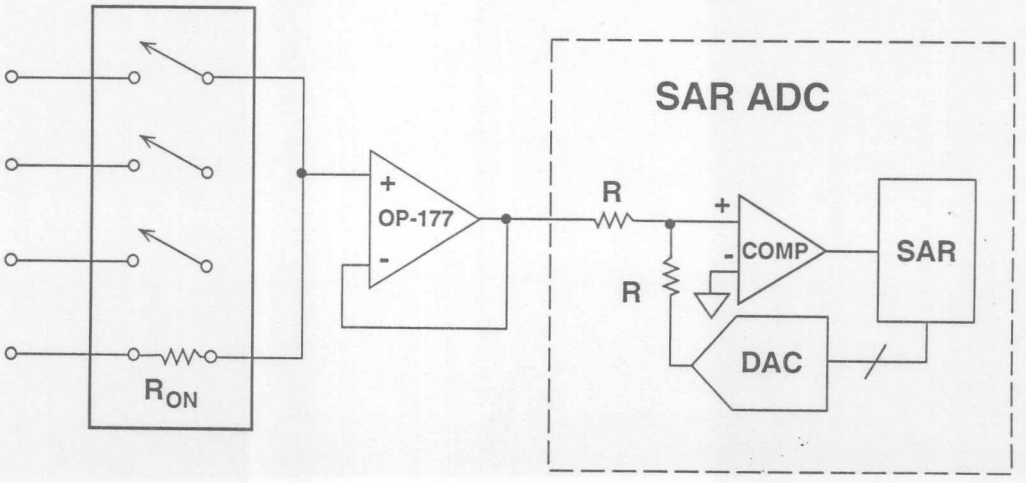
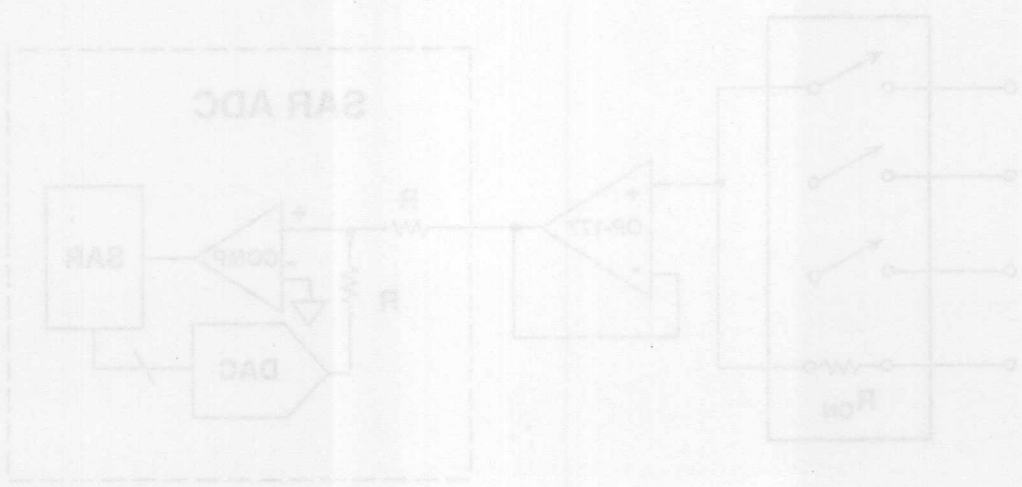


Figure 2.37



SECTION 3

PROGRAMMABLE GAIN AMPLIFIERS

SECTION 3

PROGRAMMABLE GAIN AMPLIFIERS

Joe Buxton

Most systems with wide dynamic range need some method of adjusting the input signal level to the analog to digital converter. The ADC compares the input signal to a fixed voltage reference (+5V or +10V are typical values). To achieve the rated precision of the converter, the input should be fairly near its full scale voltage. However transducers have a wide range of output voltages. High gain is needed for a small sensor voltage, but with a large transducer output a high gain will cause the amplifier or ADC to saturate. So some type of controllable gain device is needed. Such a device has a gain that is controlled by a DC voltage or, more commonly, a digital input. This device is known as a *programmable gain amplifier* or PGA. Programmable gain amplifiers have a variety of applications, and Figure 3.2 lists some of them .

PROGRAMMABLE GAIN AMPLIFIERS (PGAs)

- When Are They Needed?
- How is the Gain Switched
- What Are the Important Design Considerations?
- Tradeoffs Between Integrated and Home-Made Solutions

Figure 3.1

PGA APPLICATIONS

- Instrumentation
- Photodiode Circuits
- Ultrasound Preamplifiers
- Sonar
- Wide Dynamic Range Sensors
- Automatic Gain Control (AGC) Loops

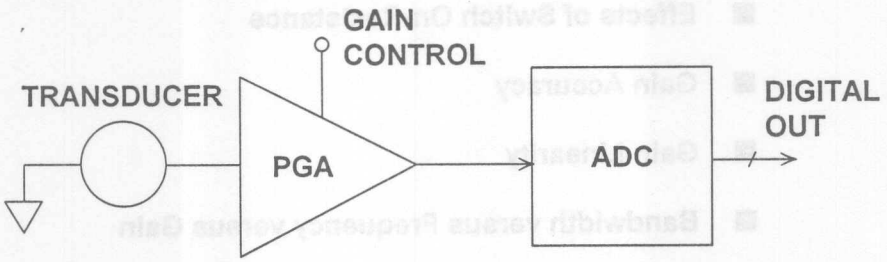
Figure 3.2

A PGA is usually located between a sensor and its ADC. Additional signal conditioning may take place before or after the PGA, depending on the application. For example, a photodiode needs a current to voltage converter between it and the PGA. In other systems, it is better to place the gain first, and condition a larger signal. This reduces errors introduced by the signal conditioning circuitry.

To understand the benefits of variable gain, assume an ideal PGA with two settings, gains of one and two. The dynamic range of the system is increased by 6dB. Increasing the gain to four results in a 12dB increase in dynamic range.

If the LSB of an ADC is equivalent to 10mV of input voltage, the ADC cannot resolve smaller signals but when the gain of the PGA is increased to two, input signals of 5mV may be resolved. Thus, the processor can combine gain information with the digital output of the ADC to increase its resolution by one bit. Essentially this is the same as adding additional resolution to the ADC.

PROGRAMMABLE GAIN AMPLIFIERS (PGAs)



- Used to Increase Dynamic Range of Circuit
- A PGA With a Gain From 1 To 2 Theoretically Increases the Dynamic Range by 6dB, A Gain of 1 To 4 Gives 12dB Increase, etc.

Figure 3.3

In practice PGAs are not ideal, and their error sources must be studied. The most fundamental problem with PGA design is accurate gain programming. Electromechanical relays have minimal R_{ON} but are otherwise unsuitable for gain switching, being slow, large and expensive, while silicon switches, as discussed in the section on switches and multiplexers, have quite large R_{ON}, which is both voltage- and temperature-variable, and stray capacities which may affect the AC parameters of a PGA using them.

PGA DESIGN ISSUES

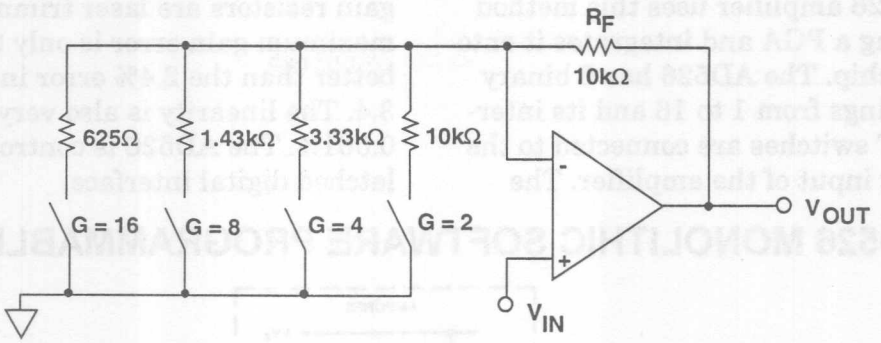
- How to Switch the Gain
- Effects of Switch On-Resistance
- Gain Accuracy
- Gain Linearity
- Bandwidth versus Frequency versus Gain
- Offset
- Temperature Effects on Gain and Offset
- Settling Time After Switching

Figure 3.4

To understand how R_{ON} can affect the performance of a PGA, let us consider a poor PGA design (Figure 3.5). An op amp is configured in the standard non-inverting gain circuit with 4 different gain setting resistors, each grounded by a switch. Most silicon switches have ON resistance in the range of 100Ω-500Ω. Even if the ON resistance were as low as 25Ω, the error for a gain of 16 would be 2.4%, much worse than 8-bits. Furthermore R_{ON} drifts over temperature, and varies from switch to switch. If the value of the feedback and gain setting resistors were increased, noise and offset would become a problem. The only way to achieve accuracy with this circuit is to replace silicon switches with relays which have virtually no ON resistance.

It is better to use a circuit where R_{ON} is unimportant. In Figure 3.6, the switch is placed in series with the inverting input of an op amp. The input impedance of an op amp is very large, the R_{ON} of the switch is irrelevant. The gain is now determined by the resistors. The R_{ON} may add a small offset error if the op amp bias current is large.

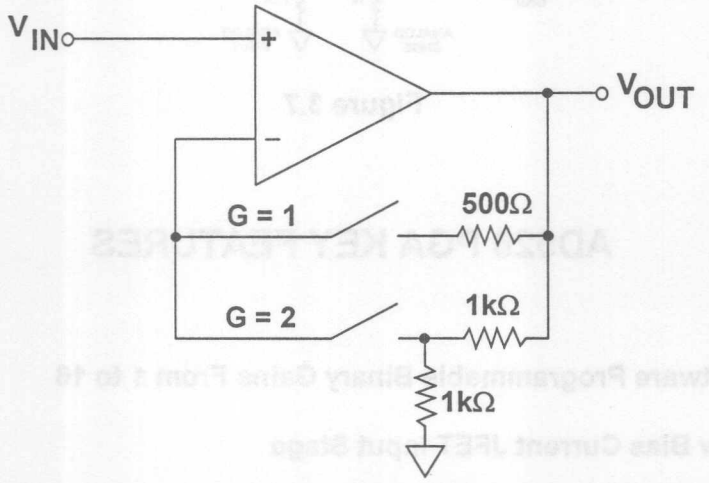
HOW NOT TO BUILD A PGA



- Gain Accuracy Limited by Switch's On Resistance, R_{on} and R_{on} Modulation
- R_{on} Typically 100 - 500Ω for a CMOS Or JFET Switch
- Even With R_{on} = 25Ω, There is a 2.4% Gain Error for A_V = 16
- R_{on} Drift Over Temperature Limits Accuracy
- Only Solution is to Use Very Low R_{on} Switches (Relays)

Figure 3.5

ALTERNATE CONFIGURATION MAKES R_{on} NEGLIGIBLE



- R_{on} is Not in Series With Gain Setting Resistors
- R_{on} is Very Small Compared to Input Impedance
- Only a Slight Offset Error Occurs Due to the Bias Current Flowing Through the Switch

Figure 3.6

The AD526 amplifier uses this method of building a PGA and integrates it onto a single chip. The AD526 has 5 binary gain settings from 1 to 16 and its internal JFET switches are connected to the inverting input of the amplifier. The gain resistors are laser trimmed. The maximum gain error is only 0.02%, far better than the 2.4% error in Figure 3.4. The linearity is also very good at 0.001%. The AD526 is controlled by a latched digital interface.

AD526 MONOLITHIC SOFTWARE PROGRAMMABLE PGA

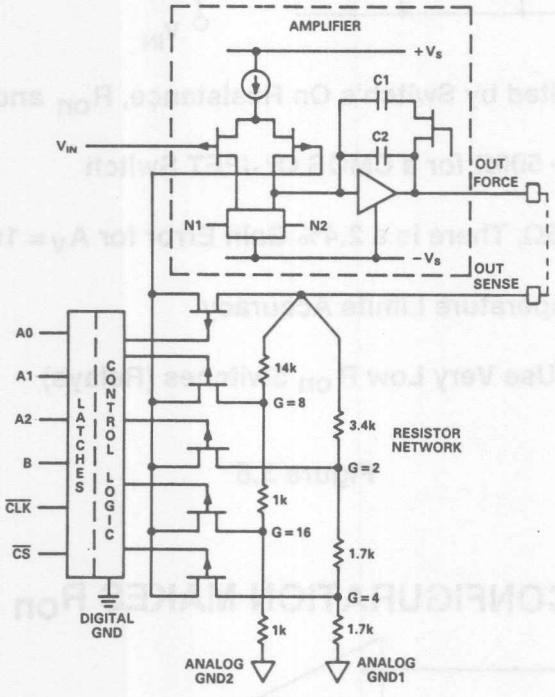


Figure 3.7

AD526 PGA KEY FEATURES

- Software Programmable Binary Gains From 1 to 16
- Low Bias Current JFET Input Stage
- Worst Case Gain Error is 0.02% (12 Bit Performance)
- Gain Nonlinearity is 0.001% Maximum
- Latched TTL Compatible Control Inputs

Figure 3.8

This same design can be used to build the discrete PGA shown in Figure 3.9. It uses a single op amp, a quad switch, and precision resistors. The low noise AD797 replaces the JFET input op amp of the AD526, but almost any voltage feedback op amp could be used in this circuit. The ADG412 was picked for its low ON resistance of 35Ω.

The resistors were chosen to give gains of 1, 10, 100 and 1000, but if other gains are required the resistor values may easily be altered. Ideally, a trimmed resistor network should be used both for initial gain accuracy and for low drift over temperature. The 20pF ensures stability and holds the output voltage when the gain is switched. The control signal to the switches turns one switch off a few nanoseconds before the second switch turns on. During this break the op amp is open-loop. If the capacitor was not used the output would start slewing. Instead, the capacitor holds the output voltage during the switching. Since the time that both switches are open is very short, only 20pF is needed. For slower switches a larger capacitor may be necessary.

A VERY LOW NOISE PGA USING THE AD797 AND THE ADG412

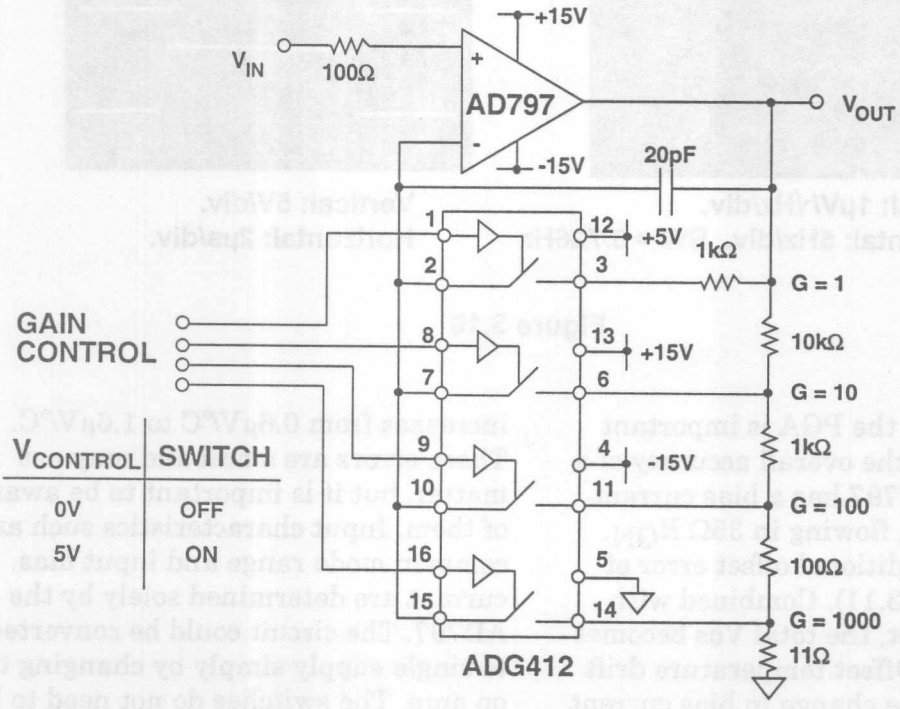


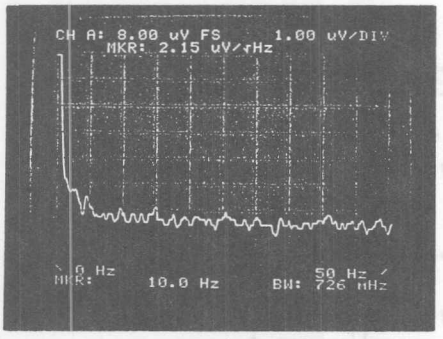
Figure 3.9

Figure 3.10 shows the noise and switching performance of the circuit. The spectral noise density is only 1.65nV/√Hz at 1kHz, only slightly higher than the noise performance of the AD797 alone. The increase is due to the noise of the ADG412 and the current noise of the AD797 flowing through the ON resistance. The noise was measured at a gain of 1000. The second photo shows the output as a function of the gain setting. The top two traces show the switch control changing the gain from 1 to 10 and back to 1. The AD797 has a constant 1 V input during this time, and as the bottom trace shows, the output changes from 1V to 10V. The circuit is well behaved with no unexpected glitches, and minimal overshoot and ringing.

AD797, ADG412 PGA NOISE AND SWITCHING TIME

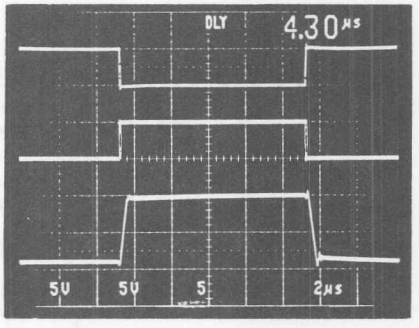
Spectral Noise Density

2.15nV/√Hz @ 10Hz
1.65nV/√Hz @ 1kHz
G = 1000



Vertical: 1μV/√Hz/div.
Horizontal: 5Hz/div., BW = 0.726Hz

Switching Time for 1V Input
From G = 1 to G = 10 to G = 1
Top Trace: G = 1 Switch Control
Middle Trace: G = 10 Switch Control
Bottom Trace: Output



Vertical: 5V/div.
Horizontal: 2μs/div.

Figure 3.10

The accuracy of the PGA is important in determining the overall accuracy of a system. The AD797 has a bias current of 0.9μA, which, flowing in 35Ω R_{ON}, results in an additional offset error of 31.5μV (Figure 3.11). Combined with the AD797 offset, the total Vos becomes 71.5μV (max). Offset temperature drift is affected by the change in bias current and ON resistance. Calculations show that the total temperature coefficient increases from 0.6μV/°C to 1.6μV/°C. These errors are small and may not matter, but it is important to be aware of them. Input characteristics such as common mode range and input bias current are determined solely by the AD797. The circuit could be converted to single supply simply by changing the op amp. The switches do not need to be changed.

AD797 PGA ACCURACY

- R_{on} Adds Additional Input Offset And Drift:

  $\Delta V_{OS} = I_b R_{on} = (0.9\mu A)(35\Omega) = 31.5\mu V$ (max)

  Total $V_{OS} = 40\mu V + 31.5\mu V = 71.5\mu V$ (max)
  (Note: 40μV is Due To The AD797B)

- Temperature Drift Due To R_{on} :

  At +85°C, $\Delta V_{OS} = (2\mu A)(45\Omega) = 90\mu V$ (max)

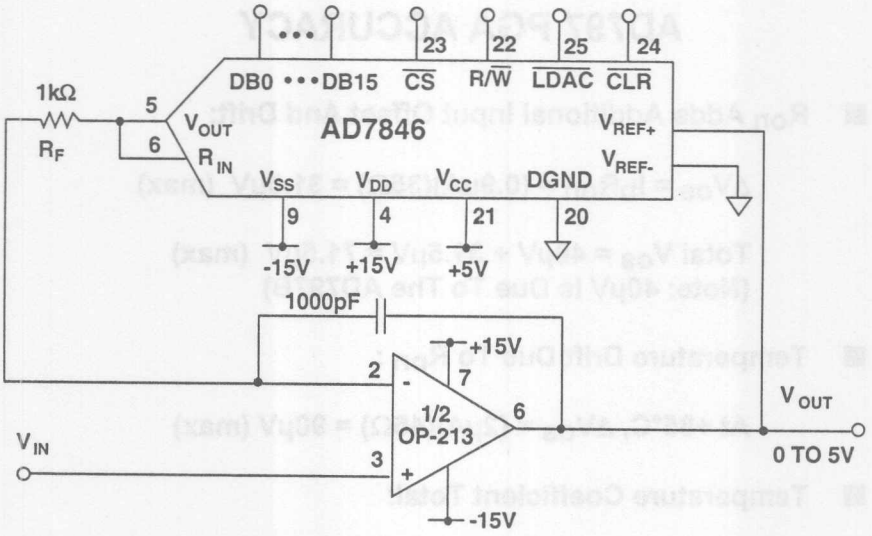
- Temperature Coefficient Total:

  $\Delta V_{OS} / \Delta T = 0.6\mu V/°C + 1.0\mu V/°C = 1.6\mu V/°C$ (max)
  (Note: 0.6μV/°C Is Due To The AD797B)

Figure 3.11

Another PGA configuration uses a DAC in the feedback loop of an op amp to adjust the gain under digital control (Figure 3.12). The digital code of the DAC controls its attenuation. Attenuating the feedback signal increases the closed-loop gain. A non-inverting PGA of this type requires a multiplying DAC with a voltage output (a multiplying DAC is a DAC with a wide reference voltage range *which includes zero*). For most applications of the PGA the reference input must be capable of handling bipolar signals. The AD7846 is a 16-bit converter that meets these requirements. In this application it is used in standard 2-quadrant multiplying mode. The OP-213 is a low drift, low noise amplifier, but the choice of amplifier is flexible and depends on the application. The input voltage range depends on the output swing of the AD7846, which is 3V less than the positive supply and 4V above the negative supply. A 1000pF capacitor is used in the feedback loop for stability.

ACCURATE BINARY GAIN PGA



- Multiplying DAC in Feedback Loop Adjusts Gain
- $G = \dfrac{2^{16}}{\text{Decimal Value of Digital Code}}$

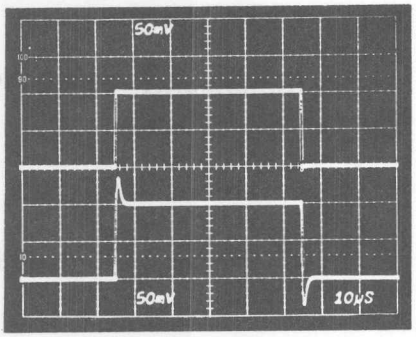
Figure 3.12

The gain of the circuit is set by adjusting the digital inputs of the DAC according to the equation given in Figure 3.12. $D_{0\text{-}15}$ represents the decimal value of the digital code. For example, if all the bits were set high the gain would be 65,536/65,535 = 1.000015. If the 8 least significant bits are set high and the rest low the gain would be 65,536/255 = 257.

Figure 3.13 shows the small signal response at a gain of 1 with a 100mV square wave input. The bandwidth is a fairly high 4MHz. However, this does reduce with gain, and for a gain of 256 the bandwidth is only 600Hz. If the gain bandwidth product were constant, the bandwidth in a gain of 256 should be 15.6kHz; but the internal capacitance of the DAC reduces the bandwidth to 600Hz.

BINARY GAIN PGA PERFORMANCE

SMALL SIGNAL RESPONSE



Top Trace: Input, 50mV/div.
Bottom Trace: Output, 50mV/div.
Horizontal Scale: 10µs/div.

Bandwidth (G=+1) = 4MHz
Bandwidth (G=+256) = 600Hz

Nonlinearity (G=+1) = 0.001%

Offset = 100µV

Noise = 50nV/√Hz

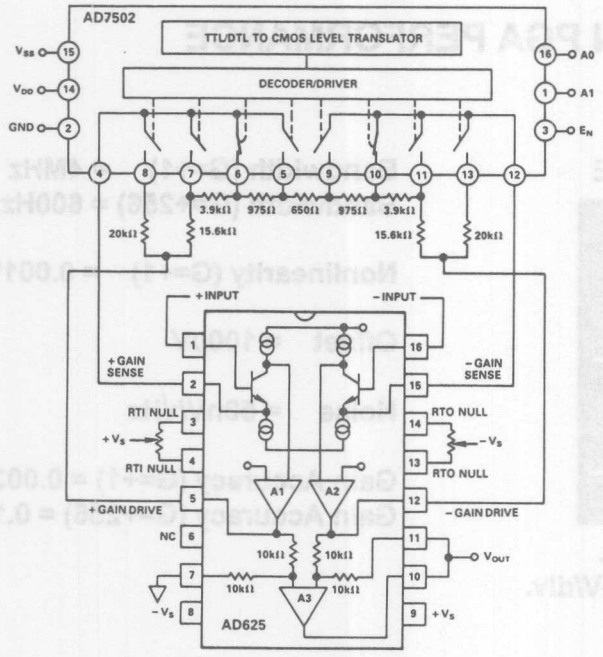
Gain Accuracy (G=+1) = 0.003%
Gain Accuracy (G=+256) = 0.1%

Figure 3.13

The gain accuracy of the circuit is determined by the resolution of the DAC and the gain setting. At a gain of 1 all bits are on, and the accuracy is determined by the DNL specification of the DAC, which is ±1 LSB maximum. Thus, the gain accuracy is equivalent to 1LSB in a 16-bit system, or 0.003%. However, as the gain is increased, fewer of the bits are on. For a gain of 256 only bit 8 is turned on. The gain accuracy is still dependent on the ±1 LSB of DNL, but now that is compared to only the lowest 8 bits. Thus, the gain accuracy is reduced to 1 LSB in a 8-bit system, or 0.4%. If the gain is increased above 256, the gain accuracy is reduced further. The designer must determine an acceptable level of accuracy. In this particular circuit the gain was limited to 256.

There are often applications where a PGA with differential inputs is needed instead of the single ended types discussed so far. The AD625 combines an instrumentation amplifier topology with gain switching capabilities to accomplish 12 bit gain accuracy (Figure 3.14). An external switch is needed to switch between different gain settings. In the example shown, resistors were chosen for gains of 1, 4, 16, and 64. Other features of the AD625 are 0.001% nonlinearity, wide bandwidth, and very low input noise.

A SOFTWARE PROGRAMMABLE GAIN AMPLIFIER



- G = 1, 4, 16, 64
- Differential Input Stage
- 12 Bit Gain Accuracy
- Nonlinearity = ± 0.001% (G = 1 to 256)
- Low Noise: 4nV/√Hz
- 25MHz Gain-Bandwidth Product

Figure 3.14

Consider the circuit in Figure 3.15. The gain is set to 64 with R_G=634Ω and the two resistors R_F=20kΩ. Since transistors Q1 & Q3, and Q2 & Q4 have 50μA current sources in both their emitters and their collectors, negative feedback around A1 and A2 respectively will ensure that no net current flows through either gain sense pin into either emitter. Since no current flows in the gain sense pins no current flows in the gain setting switches and their R_{on} does not affect either gain or offset. In real life there will be minor mismatches but the errors are well under the 12-bit level.

If no current is to flow in the gain sense pins the voltages at the ends of R_G must equal the voltages on the pins, and the voltages are determined by the voltages on the outputs of A1 and A2 and the voltage drops due to current flowing in the two R_F resistors. The differential gain between the amplifier inputs and the outputs of A1 and A2 is therefore set by the ratio (R_F+R_F):R_G. The unity gain subtractor amplifier formed by A3 and four matched resistors removes the common-mode and drives the output.

SIMPLIFIED CIRCUIT FOR AD625

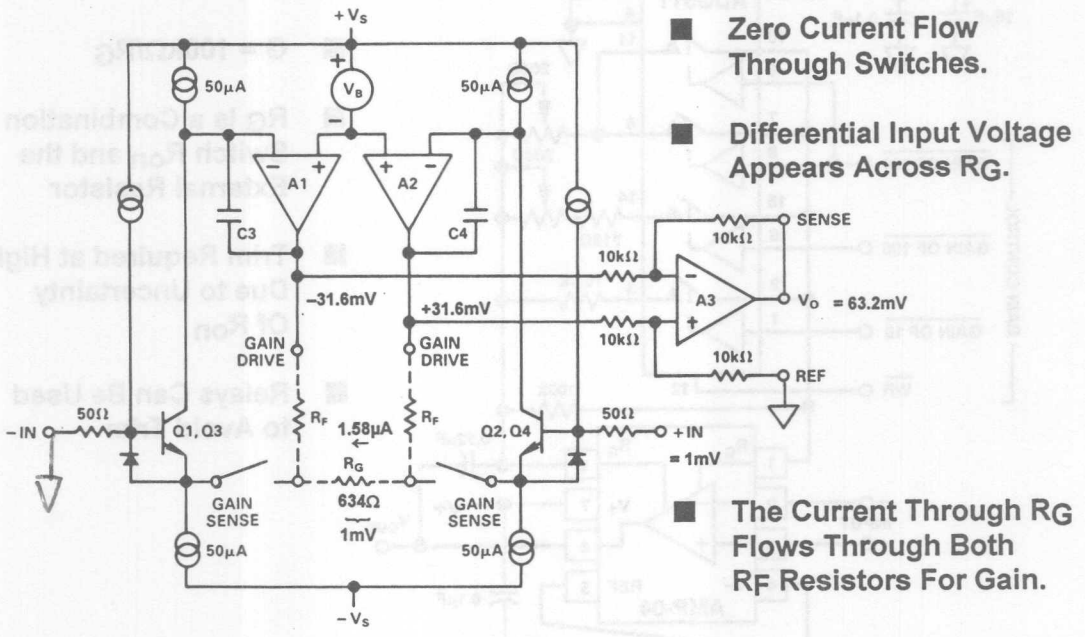
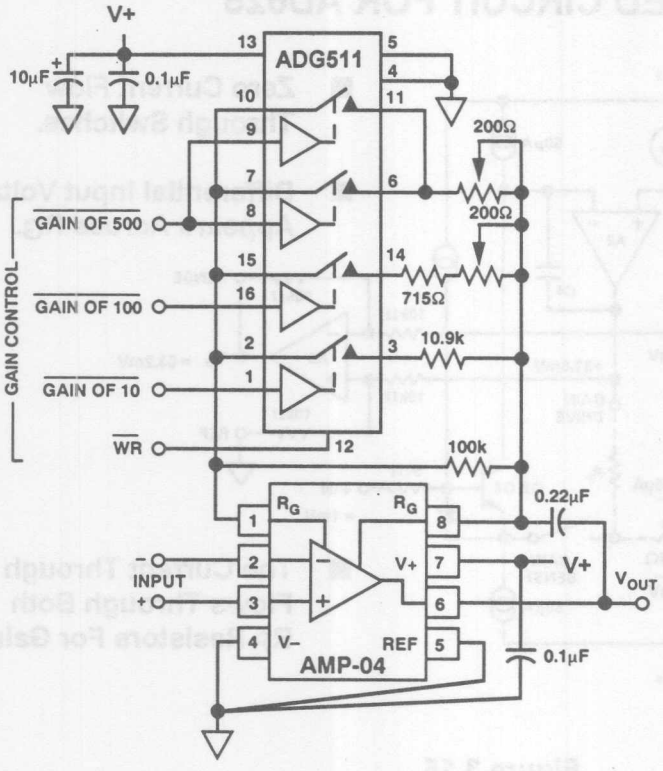


Figure 3.15

Noninverting PGA circuits using an op amp are easily adaptable to single supply, but the instrumentation amplifier topology does not lend itself to single supply applications. However, the AMP-04 can be used with an external switch to produce the single supply instrumentation PGA shown in Figure 3.16. This circuit has selectable gains of 1, 10, 100, and 500, which are controlled by an ADG511. The ADG511 was chosen as a single supply switch with a low R_{ON} of 45Ω. The gain of this circuit is dependent on the R_{ON} of the switches. Trimming is required at the higher gains to achieve accuracy. At a gain of 500, two switches are used in parallel, but their resistance causes a 10% gain error in the absence of adjustment.

As will be discussed in Chapter 6 certain ADCs have PGAs built in. Circuit design is much easier because an external PGA and its control logic are not needed. Furthermore, all the errors of the PGA are included in the specifications of the ADC, making error calculations simple. The PGA gain is controlled over the same serial interface as the ADC, and the gain setting is factored into the conversion, saving additional calculations to determine input voltage. This combination of ADC and PGA is very powerful and enables the realization of highly accurate system with a minimum of circuit design.

SINGLE SUPPLY (+5V TO +10V) INSTRUMENTATION PGA



- G = 100kΩ/RG
- RG Is a Combination of Switch Ron and the External Resistor
- Trim Required at High G Due to Uncertainty Of Ron
- Relays Can Be Used to Avoid Trim

Figure 3.16

THE AD7710 ADC HAS A BUILT-IN PGA WITH GAIN CONTROLLED BY A SERIAL INTERFACE

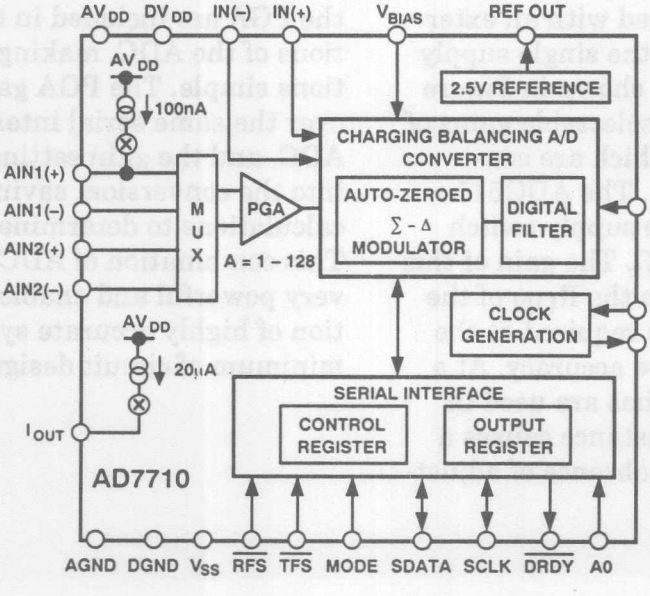


Figure 3.17

SECTION 4

HIGH ACCURACY SAMPLE AND HOLD CIRCUITRY

SECTION 4

HIGH ACCURACY SAMPLE AND HOLD CIRCUITRY

James Wong

The "sample and hold" amplifier or SHA is a critical part of many data acquisition systems. It captures an analog signal and holds it during some operation (most commonly analog-digital conversion). The circuitry involved is demanding, and unexpected properties of commonplace components such as capacitors and printed circuit boards may degrade SHA performance.

In the past the commonest application of a SHA was to maintain the input to an ADC at a constant value during conversion (with many, but not all, types of ADC the input may not change by more than 1 LSB during conversion lest the process be corrupted - this either sets very low input frequency limits on such ADCs, or requires that they be used with a SHA to hold the input during each conversion). Today, high density IC processes allow the manufacture of ADCs containing an integral SHA. Wherever possible such ADCs with integral SHA (often known as *sampling* ADCs) should be used in preference to separate ADCs and SHAs. The advantage of such a sampling ADC, apart from the obvious ones of smaller size, lower cost and fewer external components, is that the overall performance is specified and the designer need not spend time ensuring that there are no specification, interface or timing issues involved in combining a discrete ADC and a discrete SHA.

While both AC and DC specifications are important in determining the accuracy of a SHA, the AC specifications are generally the most difficult to achieve. The dynamic behavior, and typical dynamic imperfections, of a SHA are shown in Figure 4.2.

SAMPLE-AND-HOLDS ARE DEMANDING CIRCUITS

- Where Possible use ADCs with Built-In SHAs (Sampling ADCs)
- Understand SHA Parameters
- Select the Hold Capacitor Carefully
- Take Great Care with Board Layout

Figure 4.1

KEY SHA DYNAMIC PERFORMANCE CHARACTERISTICS

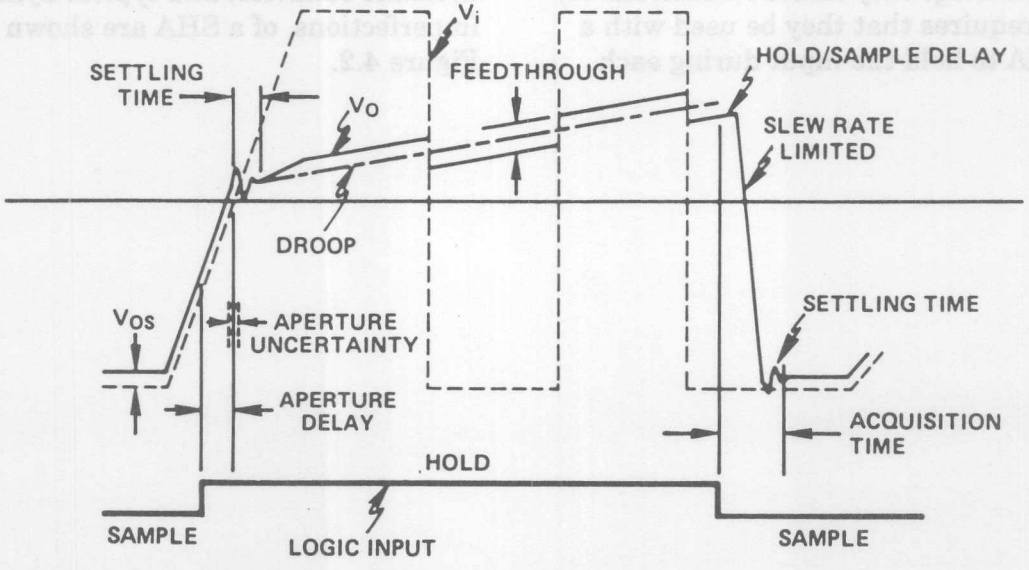


Figure 4.2

The input signal is illustrated as a dotted line and the SHA output as a solid line. When the sample/hold control is in sample mode the output follows the input with only a small voltage offset. (There do exist SHAs where the output during "sample" does not follow the input accurately and the output is only accurate during the "hold" period · these are uncommon and will not be considered here. Strictly speaking a sample and hold with good tracking performance should be referred to as a "track and hold" circuit, but in practice the terms are used interchangeably.)

Ideally, when the "hold" signal is asserted the SHA output is locked at its value at the instant of assertion. In practice there is a delay, known as the aperture time, before the hold command takes effect, and there is an uncertainty, which varies from sample to sample, in the exact value of the aperture time - this is known as the aperture jitter. In a sampled data system it may be demonstrated that phase noise, or jitter, on the sampling clock is a major cause of loss of system resolution (Reference I). In early sampled data systems the major cause of sampling clock jitter was the aperture jitter of the SHA in the system - today SHA performance has improved and other sources of jitter (noisy clocks, digital interference, etc.) are at least equally important.

Switching to hold disturbs the system. There will be a short interval, known as the settling time, while it settles down to its proper value again. Settling time is defined as the delay between the hold edge and the SHA returning within *and remaining within* some error band. Different SHAs have widely different settling times, but for a given SHA the settling time will be longer if a tight error band is chosen.

Ideally the output of a SHA immediately before and immediately after the hold transition should be identical. In practice the transients generated by the sample-hold transition inject a small amount of charge into the capacitor which stores the signal and produce an offset between the sample and hold states. This offset is called the *pedestal.* In some SHAs the pedestal amplitude varies with signal and is a source of non-linearity.

Almost all SHAs use a capacitor to store the voltage which is being "remembered". If a leakage current flows in or out of this capacitor it will slowly charge or discharge, and its voltage will change. This effect is known as "droop" in the SHA output. Droop can be caused by leakage across a dirty PCB if an external capacitor is used, or by a leaky capacitor, but is most usually due to leakage current in semiconductor switches and the bias current of amplifiers connected to the capacitor. Droop is expressed in V/μS. An acceptable value of droop is where the output of a SHA does not change by more than ½ LSB during the conversion time of the ADC it is driving. Where droop is due to leakage current in reverse biased junctions (switches or FET amplifier gates) it will double for every 10°C increase in chip temperature - which means that it will increase a thousand fold between 25°C and +125°C. Droop and pedestal can be reduced by increasing the value of the hold capacitor, but this will also increase acquisition time and reduce bandwidth in sample mode.

Stray capacity in a SHA may allow a small amount of the AC input to be coupled to the output during hold. This effect is known as *feedthrough.*

SHAs which are built into sampling ADCs do not require very good droop

specifications, since the ADC conversion takes place quite quickly and once the conversion is complete the SHA need not store accurately any longer. Such SHAs generally use a small hold capacitor built on the chip itself. Where long hold times and low droop are required a separate discrete hold capacitor will be required.

Hold capacitors for SHAs must have low leakage, but there is another characteristic which is equally important: low *dielectric absorption*. If a capacitor is charged, then discharged, and then left open circuit it will recover some of its charge. The phenomenon is known as *dielectric absorption*, and it can seriously degrade the performance of a SHA, since it causes the remains of a previous sample to contaminate a new one, and may introduce random errors of tens or even hundreds of mV.

DIELECTRIC ABSORPTION - CHARGE RETENTION

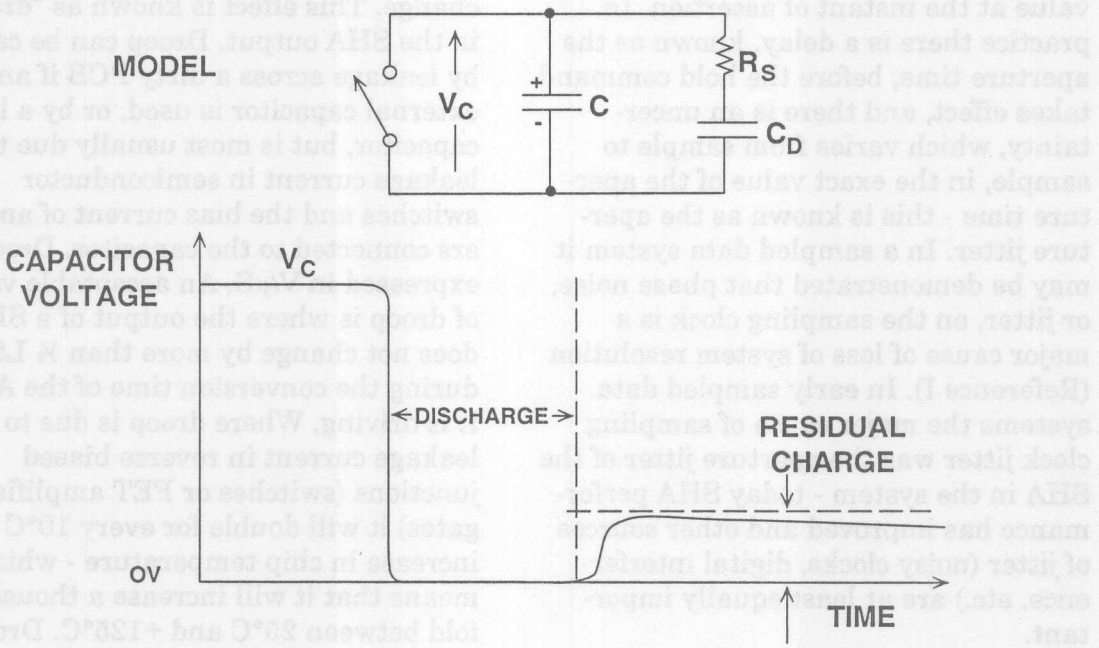


Figure 4.3

Different capacitor materials have differing amounts of dielectric absorption:- electrolytic capacitors are dreadful (their leakage is also high) and some high-K ceramic types are bad, while mica, polystyrene and polypropylene are generally good. Unfortunately dielectric absorption varies from batch to batch and even occasional batches of polystyrene and polypropylene capacitors may be affected. It is therefore wise to pay 30-50% extra when buying capacitors for SHA applications and buy devices which are guaranteed by their manufacturers to have low dielectric absorption, rather than types which might generally be expected to have it.

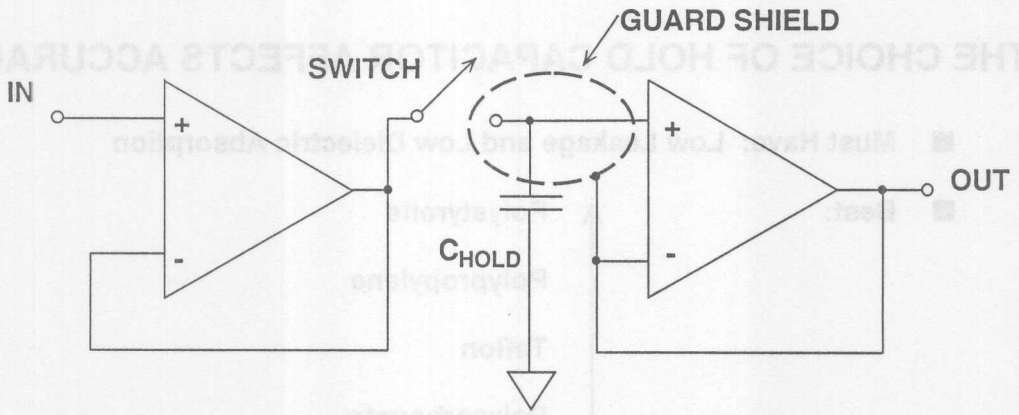
THE CHOICE OF HOLD CAPACITOR AFFECTS ACCURACY

- Must Have: Low Leakage and Low Dielectric Absorption
- Best:
  - Polystyrene
  - Polypropylene
  - Teflon
  - Polycarbonate
- Worst:
  - Mylar
  - Glass
  - Electrolytic

Figure 4.4

Even quite small leakage currents can cause troublesome droop when SHAs use small hold capacitors. Leakage currents in PCBs may be minimized by the intelligent use of guard rings. A guard ring is a ring of conductor which surrounds a sensitive node and is at the same potential. Since there is no voltage between them there can be no leakage current flow. In a non-inverting application, such as is shown in Figure 4.5, the guard ring must be driven to the correct potential, whereas the guard ring on a virtual ground can be at actual ground potential. The surface resistance of PCB material is much lower than its bulk resistance, so guard rings must always be placed on both sides of a PCB - and on multi-layer boards guard rings should be present in all layers.

DRIVE THE GUARD SHIELD WITH THE SAME VOLTAGE AS THE HOLD CAPACITOR TO REDUCE BOARD LEAKAGE



Note: Be Sure a Guard Shield is in Each Layer of the PCB

Figure 4.5

We have mentioned that modern ADCs frequently contain integral SHAs. Figure 4.7 shows how a venerable old ADC, the AD574 (the most widely sold 12-bit ADC ever manufactured), has been redesigned as a sampling ADC, the AD1674. The AD1674 is identical to the AD574 in most respects, including pinout and power requirements, although it outperforms it on a number of specifications, but contains a high performance SHA to extend its utility. The AD1674 may be used in any AD574 socket but will also handle much faster input signal changes.

USING A GUARD SHIELD ON A VIRTUAL GROUND SHA DESIGN

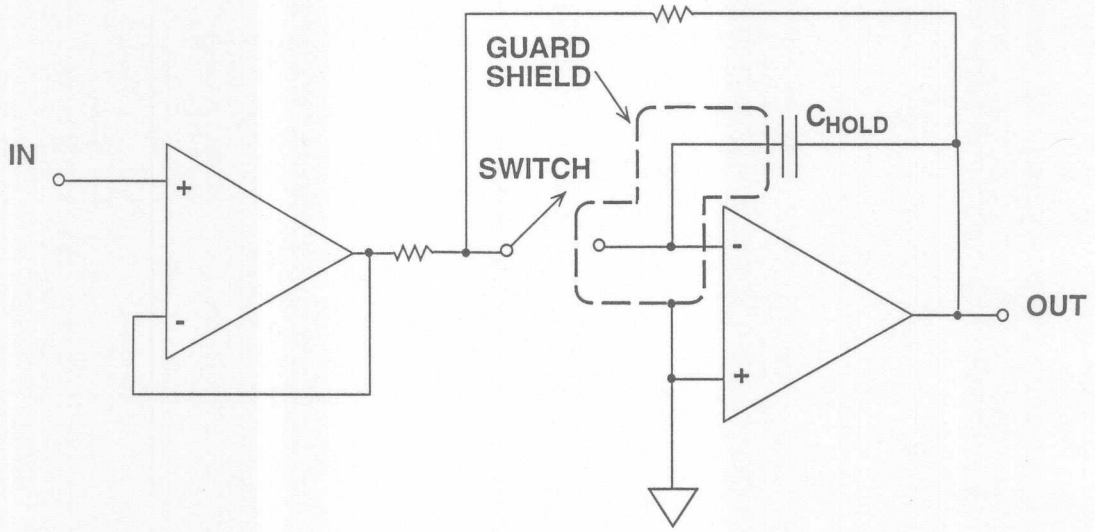


Figure 4.6

MANY LATEST GENERATION ADCs HAVE ON-CHIP SHAs

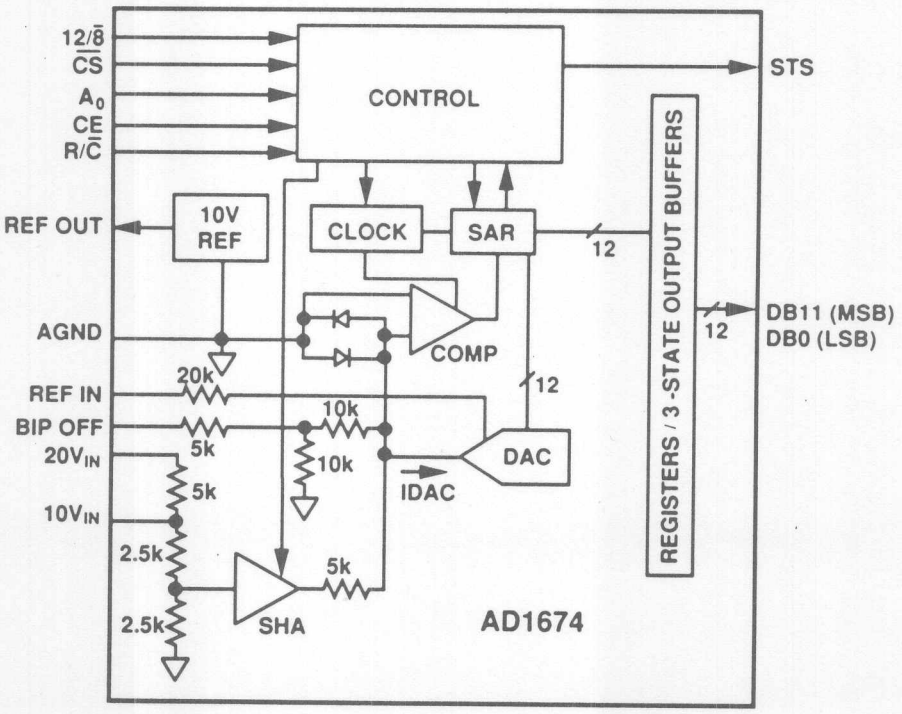


Figure 4.7

REFERENCES

[1] **Mixed Signal Seminar,** Analog Devices, Chapter 1

SECTION 5

VOLTAGE REFERENCES FOR HIGH ACCURACY SYSTEMS

- A LOW-NOISE DISCRETE BANDGAP DESIGN
- AN ULTRA LOW-NOISE REFERENCE CIRCUIT
- AVOID HEAVY LOADS ON REFERENCE OUTPUTS

SECTION 5

VOLTAGE REFERENCES FOR HIGH ACCURACY SYSTEMS

James Wong

Voltage references have a major impact on the performance and accuracy of analog systems. A ±5mV tolerance on a 5V reference corresponds to ±0.1% absolute accuracy–only 10-bits. For a 12-bit system choosing a reference that has a ±1mV tolerance may be far more cost effective than performing manual calibration, while both high initial accuracy and calibration will be necessary in a system making absolute 16-bit measurements. (Many systems make *relative* measurements rather than absolute ones and in such cases the absolute accuracy of the reference is not important, although noise and short-term stability may be.)

Temperature drift or drift due to aging may be an even greater problem than absolute accuracy. The initial error can always be trimmed, but compensating for drift is difficult. Where possible references should be chosen to have a temperature coefficient and aging characteristics that preserve adequate accuracy over the operating temperature range and expected lifetime of the system.

Long-term stability is rarely specified on data sheets. Where a figure is given it is usually drift expressed in ppm/1000 hours. There are 8766 hours in a year and many engineers multiply the 1000 hour figure by 8.77 to find the annual drift - this is incorrect. Long term drift in precision analog circuits is a "random walk" phenomenon and increases with the *square root* of the elapsed time (this supposes that drift is due to random micro-effects in the chip and not some over-riding cause such as contamination). The 1 year figure will therefore be about $\sqrt{8.766} \approx 3$ times the 1000 hour figure and the ten year value will be roughly 9 times the 1000 hour value. In practice things are a little better even than this, as devices tend to stabilize with age.

Only three things in life are certain: death and taxes - and noise. Noise in voltage references is often overlooked, but it can be very important in system design. It is generally specified on data sheets, but system designers frequently ignore the specification and assume that voltage references do not contribute to system noise.

There are two dynamic issues that must be considered with voltage references: their behavior at start-up and their behavior with transient loads. Voltage references do not power up instantly (this is true of references inside ADCs and DACs as well as discrete designs). Many early designs took tens, or even hundreds, of milliseconds to deliver any output at all and as long again before reaching full accuracy - modern designs tend to start up more quickly (but read the data sheet) but still need time to reach thermal equilibrium. It is rarely possible to turn on an ADC and reference, whether internal or external, make

a reading, and turn off again within a few microseconds, however attractive such a procedure might be in terms of energy saving. (There are also issues, which we shall not consider here, of anomalous ADC logic states on start-up. Irrespective of reference accuracy the first, and sometimes even the second, result from an ADC after powering up may be in error because of misbehavior arising from the state of its logic immediately after power is applied.)

Many reference have low power, and therefore low bandwidth, buffer amplifiers. This makes for poor behavior under fast transient loads, which may degrade the performance of fast ADCs, especially successive approximation and flash ADCs (Reference 2). Suitable decoupling can ease the problem (but some references oscillate with capacitive loads), or an additional external broadband buffer amplifier may be used to drive the node where the transients occur.

CHOOSING VOLTAGE REFERENCES FOR HIGH RESOLUTION SYSTEMS

- Tight Tolerance Improves Accuracy, Reduces Costs
- Temperature Drift Affects Accuracy
- Long-Term Stability Assures Repeatability
- Noise Limits System Resolution
- Dynamic Loading Causes Errors

Figure 5.1

There are two common types of voltage references: bandgap and buried zener. Both make good stable references, and each has particular strengths and weaknesses which are listed in Figure 5.2.

ATTRIBUTES OF REFERENCE ARCHITECTURES

BANDGAP	BURIED ZENER
■ Low Reference Voltage	■ Low Noise
■ Low Quiescent Power	■ Good Long-Term Stability

Figure 5.2

Bandgap references make use of the bandgap voltage of silicon: 1.230 V. Properly designed bandgap references compensate PTAT and CTAT ("Proportional to Absolute Temperature" and "Complimentary to Absolute Temperature") voltages to obtain a stable output near this value (Reference 3). Other voltages may be obtained by using this as the input to a precision amplifier with suitable gain.

Buried zener diodes are zener diodes fabricated beneath the surface of a chip. The surface of a chip is prone to contamination and lattice dislocations and zener diodes at the surface are more noisy and less stable than "buried" ones. Buried zener diodes may be made with a range of voltages, they all have good low noise performance (better than bandgap references) but ones which, in combination with their temperature compensating diodes, have a breakdown voltage just below 7V have the best temperature performance. Figure 5.3 shows a range of voltage references, both bandgap and buried zener, with high initial accuracy and low drift.

VOLTAGE REFERENCE CHARACTERISTICS

PART NUMBER	OUTPUT VOLTAGE	INITIAL ACCURACY	MAXIMUM TC	SUPPLY CURRENT
AD780	+2.50V	±1mV	3 ppm/°C	1mA
REF-195	+5.00V	±1mV	4 ppm/°C	40µA
AD588	+10V, +5V, ±5V, -5V, -10V	±1mV	1.5 ppm/°C	10mA
REF-43	+2.50V	±1.5mV	10 ppm/°C	450µA
AD584	+10V	±2.5mV	5 ppm/°C	1mA
AD581	+10v	±5mV	5 ppm/°C	1mA
AD680	+2.5V	±5mV	20 ppm/°C	250µA

Figure 5.3

If the output of a voltage reference must be trimmed, it is important that a single trim potentiometer be used in order to preserve the low drift of the reference. As shown in Figure 5.4, the output voltage is amplified from the reference. The gain of the amplifier is set by resistors, and gain stability depends on the matching of their temperature coefficients (TCs). If the resistors are thin film types on the reference chip the matching will be excellent, but if external resistors are used to trim gain the TCs will not match and the TC of the adjusted reference voltage will be degraded. The circuit shown in Figure 5.4 is the best way to trim the output of a voltage reference, since the TC of the external resistors has least effect on the reference TC. Of course a better, but more complex, technique would be to use a second trimmable amplifier after the output of the untrimmed voltage reference - if the TC of this amplifier can be kept low enough then the TC of the system will not be degraded.

Reference voltage drift makes maintaining 14-bit accuracy over temperature especially difficult. Figure 5.5 illustrates the accuracy that can be expected as a function of drift. Even the best available reference, at 1 ppm/°C, is only 14-bit accurate over the temperature range of +25°C to +85°C. Special techniques are required for better accuracy.

IF YOU MUST TRIM:

- Use single trim potentiometer
- Do not insert fixed resistors in the trim leg -- this causes poor tempco match

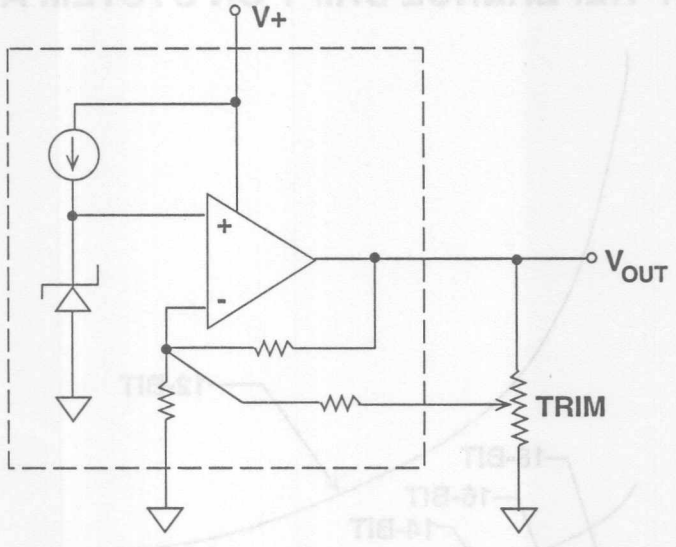


Figure 5.4

EFFECTS OF DRIFT ON SYSTEM ACCURACY

DRIFT	TOTAL CHANGE IN OUTPUT, 10V FS (25°C TO 85°C)	EQUIVALENT ACCURACY
10 ppm/°C	6mV	10 bit
5 ppm/°C	3mV	11 bit
4 ppm/°C	2.4mV	12 bit
1 ppm/°C **	0.6mV	14 bit
0.25 ppm/°C	0.15mV	16 bit

** Best Reference Available Commercially

Figure 5.5

Figure 5.6 shows the allowable reference voltage drift in ppm/°C as a function of total system temperature span. Curves are shown for 12, 14, 16, and 18-bit accuracy. The reference voltage specification becomes more demanding as resolution and temperature range increase.

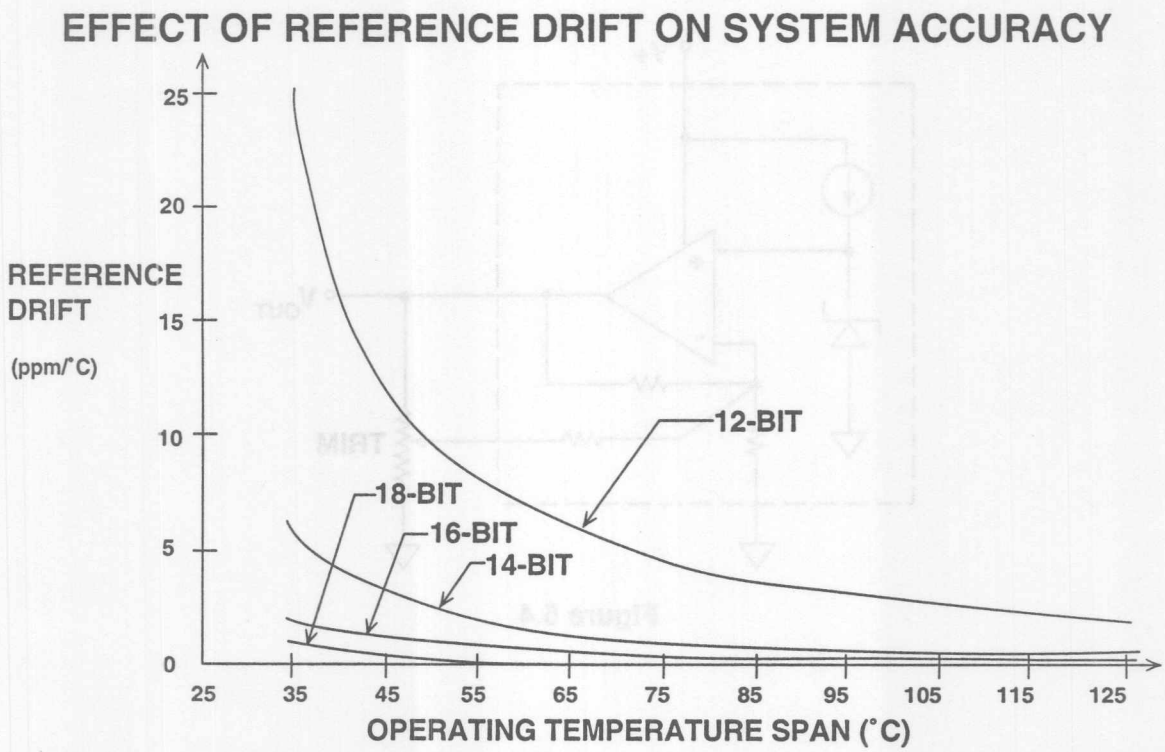


Figure 5.6

Maintaining absolute 16-bit accuracy requires reference voltage TCs of less than 1ppm/°C. The best commercially available references are only about 1ppm/°C, so continuous self-calibration must be used to maintain the required accuracy.

FOR APPLICATIONS GREATER THAN 16-BITS, IT IS DIFFICULT TO RELY ON REFERENCE DRIFT BELOW 1 ppm/°C

- Use System Calibration Technique
- Temperature Drift Compensation
- Buffer Heavy Loads to Minimize Drift Due to Self-Heating
- Reference Noise May Limit Repeatability

Figure 5.7

Heavy loads at the reference output induce self-heating of the die. Self-calibration cycles cannot always be synchronized to the self-heating time constants and consequently, thermal drift will modulate the output despite self-calibration. But buffer amplifiers will not necessarily overcome the problem, since they too will have errors due to self-heating. Careful design, self-calibration, plus heat sinking and study of thermal time constants will be necessary to meet the requirements of 16-bit systems.

Reference noise is often overlooked as a source of error. Reference voltage noise is usually specified as a peak-to-peak value in the bandwidth of 0.1Hz to 10Hz. However, many references have no provisions for limiting bandwidth, so the actual rms noise will be much larger unless steps are taken to limit the bandwidth externally. Figure 5.8 illustrates how wideband noise (100kHz bandwidth) can limit resolution.

The benefit of limiting noise bandwidth is illustrated in Figure 5.9. A terminal is provided on the AD587 for noise filtering. The capacitor C_N forms a low pass filter with the internal resistor R_B that limits the noise bandwidth at the output of the zener diode. A 1µF capacitor gives a 3dB bandwidth of 40Hz. The photo shows noise measured in a 1MHz bandwidth with and without the filter capacitor. Even lower noise can be achieved by increasing the filter capacitor at the expense of longer turn-on time. But the external filter capacitor, C_N, does not eliminate the wideband noise in the output buffer of the AD587, and this sets a limit to the possible improvement. Noise may be reduced further by placing another filter at the output terminal of the AD587.

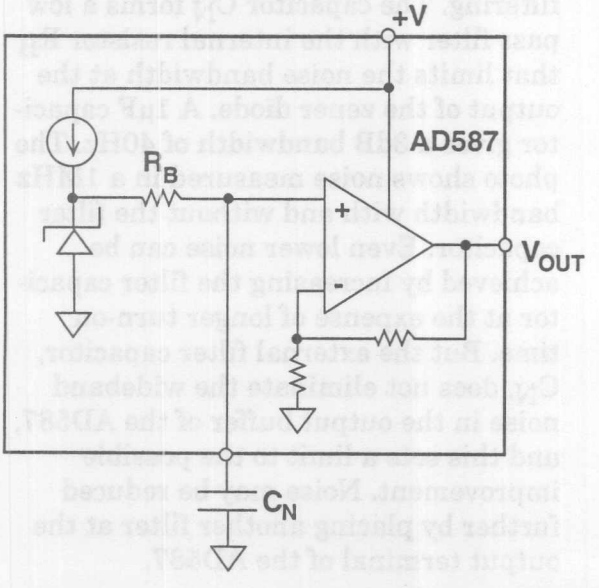
EFFECTS OF REFERENCE NOISE ON SYSTEM ACCURACY, RULE OF THUMB: KEEP NOISE < 1/4 LSB

NOISE SPECTRAL DENSITY	NOISE VOLTAGE (BW = 100kHz)	EQUIVALENT ACCURACY
322 nV/√Hz	610 µV p-p	12 bits
80 nV/√Hz	153 µV p-p	14 bits
20 nV/√Hz	38 µV p-p	16 bits
5 nV/√Hz	10 µV p-p	18 bits
1.3 nV/√Hz*	2.4 µV p-p	20 bits

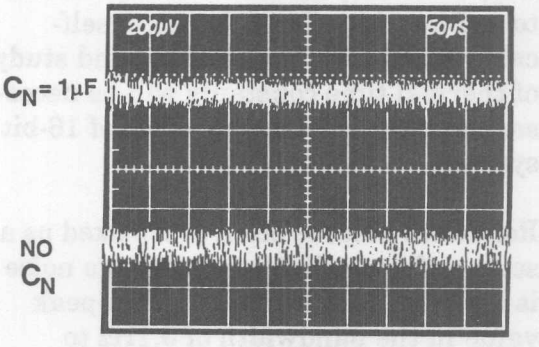
* LESS THAN JOHNSON NOISE IN A 100Ω RESISTOR

Figure 5.8

LOW REFERENCE NOISE IS CRITICAL FOR > 16-BIT ACCURACY



Solution: Bandwidth Limiting



VERTICAL SCALE: 200µV/div.
HORIZONTAL SCALE: 50µs/div.

Figure 5.9

A LOW NOISE DISCRETE BANDGAP REFERENCE

Monolithic voltage references have better stability but can rarely achieve the noise performance of a well-designed discrete circuit. An example of a reference circuit with excellent noise performance appears in Figure 5.10. Its performance parameters is summarized in Figure 5.11. The circuit's 100kHz wideband noise is 20μV rms.

The circuit uses low noise matched transistors (MAT-04) operating at high collector currents to minimize noise. Three of the transistors are connected in parallel to reduce noise further. The fourth forms the other leg of the bandgap core. Being monolithic, the four matched transistors also maintain identical temperatures, and therefore good drift characteristics. Biasing the bandgap core with high current minimizes the noise contribution from R3.

Care must be taken to shield the entire circuit thermally to minimize drift due to ambient temperature gradients - which may produce parasitic thermoelectric voltages. The circuit layout should also be compact. All resistors should be of the same type, with matched temperature coefficients. RN55C (1%, ±50 ppm/°C) type resistors work well. R1 and R2 are particularly sensitive because any mismatch changes the current ratio in the core, and produces a higher drift. Similarly, the ratio R4:R3 amplifies ΔV by the current ratio. Mismatch due to temperature coefficient variation in R3 and R4 introduces drift by affecting the Q1 and Q2 V_{BE}. Finally, R6, R7, and R8 amplify the 1.23V bandgap voltage to 5.000V. Mismatch in them will cause additional errors.

To calibrate the circuit, adjust R5 for a bandgap voltage of 1.230V at 25°C. Then adjust R7 for a +5.000V at the output. Despite its low noise the circuit has poor temperature stability compared to the AD588 monolithic device. The designer must decide which is more important: noise or stability.

The basic bandgap reference is not self-starting. Resistors R9 and R10 plus an NPN transistor (Q3) start the circuit. When the supply is turned on, there is no current in the bandgap core, and the op amp output is at 0V. The base voltage of Q3 reaches 3.9V, and its emitter rises to 3.2V pulling up the op amp output. At this point the core starts to conduct, the op amp moves to its linear operating point, and the output stabilizes at 5V. This turns off transistor Q3, so that it no longer affects the circuit.

DISCRETE DESIGN PROVIDES ULTRA LOW NOISE

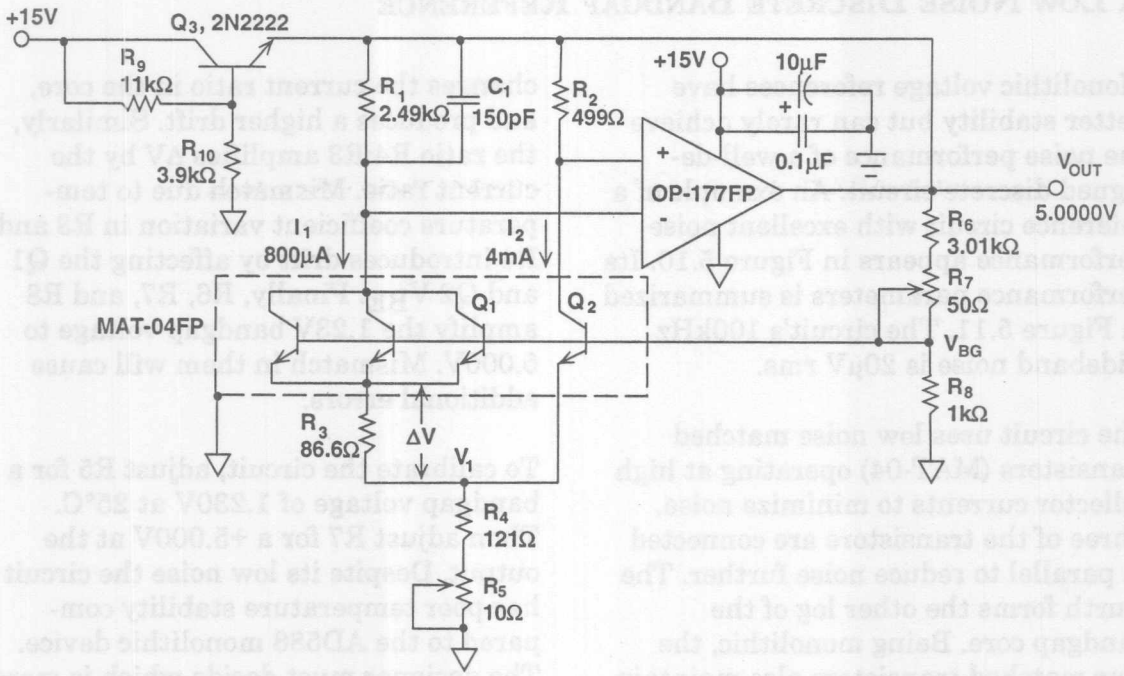


Figure 5.10

DESIGN EQUATIONS AND PERFORMANCE OF DISCRETE BANDGAP VOLTAGE REFERENCE

$$\Delta V = V_T \ln\left[\left(\frac{I_2}{I_1}\right)\left(\frac{A_1}{A_2}\right)\right],$$

WHERE A_1 = EMITTERS IN $Q_1 = 3$

A_2 = EMITTERS IN $Q_2 = 1$

$$V_1 = \left[\left(\frac{R_4}{R_3}\right)\left(\frac{I_2}{I_1}\right)\right]\Delta V = 7.0\Delta V, \quad V_{BG} = V_1 + V_{BE}(Q2) = 1.23V\ @\ 25°C$$

■ Output Voltage:	5.000V
■ Output Noise Voltage (0.1 to 10Hz)	1.6µV p-p
■ Noise Spectral Density @ 1kHz:	63nV/√Hz
■ Wideband Noise (BW = 100kHz):	20µV rms
■ Drift (-40°C ≤ T_A ≤ +85°C):	14 ppm/°C
■ Line Regulation (6 to 40V):	2 ppm/V
■ Load Regulation (0 to 10mA):	6 ppm/mA
■ Supply Current @ 15V:	8mA

Figure 5.11

AN ULTRA LOW NOISE REFERENCE CIRCUIT (REFERENCE 4)

Another approach to achieving ultra-low noise is to use extensive external filtering. The circuit in Figure 5.12 uses an ultra-low noise amplifier, the AD797, to buffer the AD587 10V reference. It also acts as low-pass filter with a 1Hz corner frequency. The combination produces exceptionally low noise.

COMBINING LOW-NOISE AMPLIFIER WITH EXTENSIVE FILTERING YIELDS EXCEPTIONAL NOISE PERFORMANCE

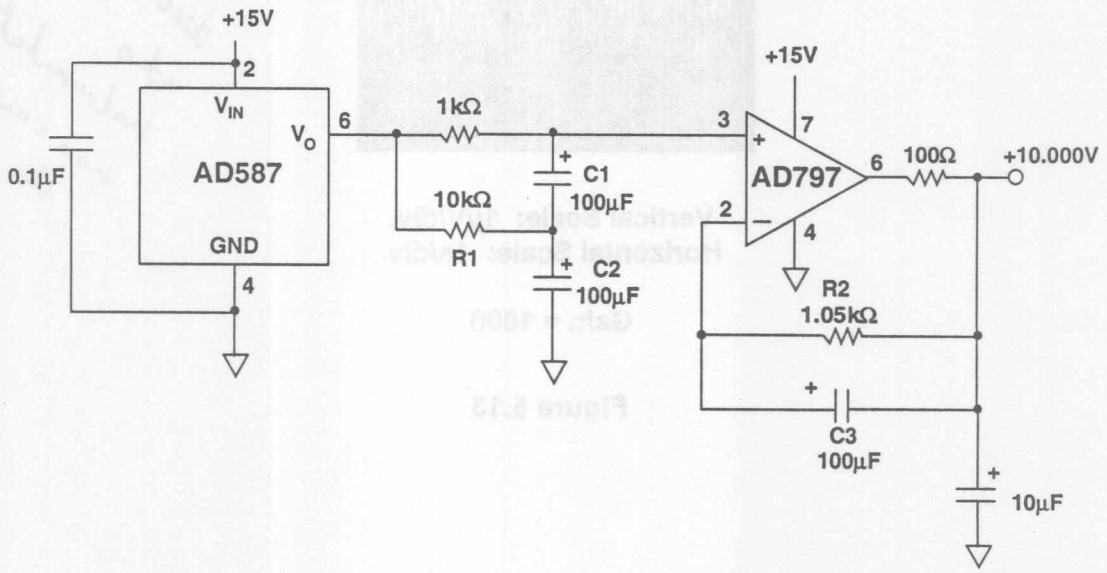
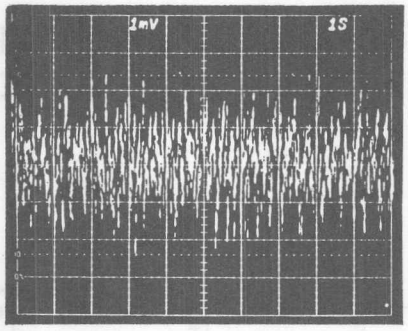


Figure 5.12

The unconventional arrangement of capacitors in the low pass filter ensure that the leakage currents of the capacitors and the bias current of the AD797, both of which are quite large, do not contribute to the DC errors in the system. C2 is biased to V_O by R1 so that the voltage on C1 is minimal, as is its leakage. R2 is a bias current compensation resistor and C3 acts as an AC bypass to it.

Figure 5.13 shows the noise level at the output. With the 1Hz low pass filter, the final output noise is 5µV peak-to-peak. This circuit will greatly enhance the signal to noise performance of a high resolution system and can provide an output drive current of 50mA.

1Hz LOW PASS FILTER REDUCES NOISE TO 5 µV p-p, WHILE AD797 INCREASES DRIVE TO 50mA



Vertical Scale: 1µV/div.
Horizontal Scale: 1s/div.

Gain = 1000

Figure 5.13

HEAVY LOADING AFFECTS REFERENCE DRIFT

- Load Regulation Limitations
- Self-Heating
- Solutions: Isolate Very Heavy Loads

  Use References Designed for Driving Medium Loads

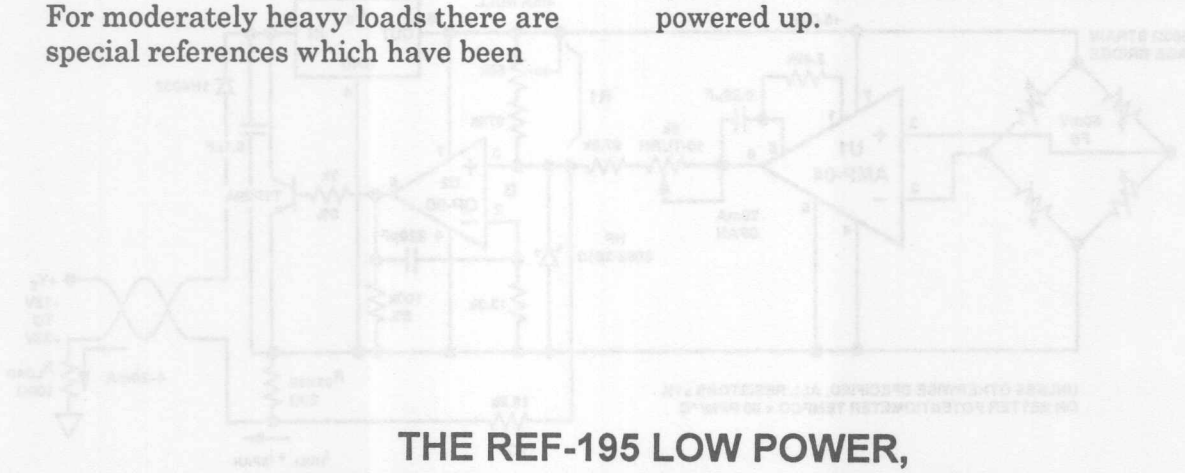
Figure 5.14

AVOID HEAVY LOADS ON REFERENCE OUTPUTS

For high precision applications, it is not advisable to put very heavy loads directly on the reference output. Increased output current will cause the reference to lose accuracy and also increases drift due to self-heating.

The simplest way to minimize reference voltage drift in the presence of very heavy loads is to buffer the reference output with an accurate current-booster amplifier.

For moderately heavy loads there are special references which have been developed to drive currents of several tens of mA without loss of accuracy. An example is the REF-195, whose key specifications appear in Figure 5.15. It will deliver at least 30mA and still offer high precision, it has very low drop-out (the voltage between input and output terminals) and can be shut down into a "sleep" mode with no output (and a graceful shutdown, and power up again afterwards) and a standby consumption of <5μA. It only draws 30μA of power (plus the load current, of course) when powered up.



THE REF-195 LOW POWER, HIGH OUTPUT, PRECISION REFERENCE

- Designed to Deliver High Current: 30 mA
- Tight Output Tolerance: ± 1mV max.
- Low Drift: 4 ppm/°C max.
- Ultra Low Power: 30 μA
- Low Drop-Out @ 10 mA Load: 0.3 V max.
- Has 5 μA Power Drain in Sleep Mode

Figure 5.15

The REF-195 makes an excellent reference / regulator for powering a 4-20mA current loop (Figure 5.16). The REF-195 provides the power to the amplifier circuit as well as the bias voltage for the strain-gauge bridge. The bridge signal is amplified by the AMP-04 single-supply instrumentation amplifier with a gain of approximately 40.

REF-195 POWERS 4-TO-20mA LOOP PLUS BRIDGE EXITATION

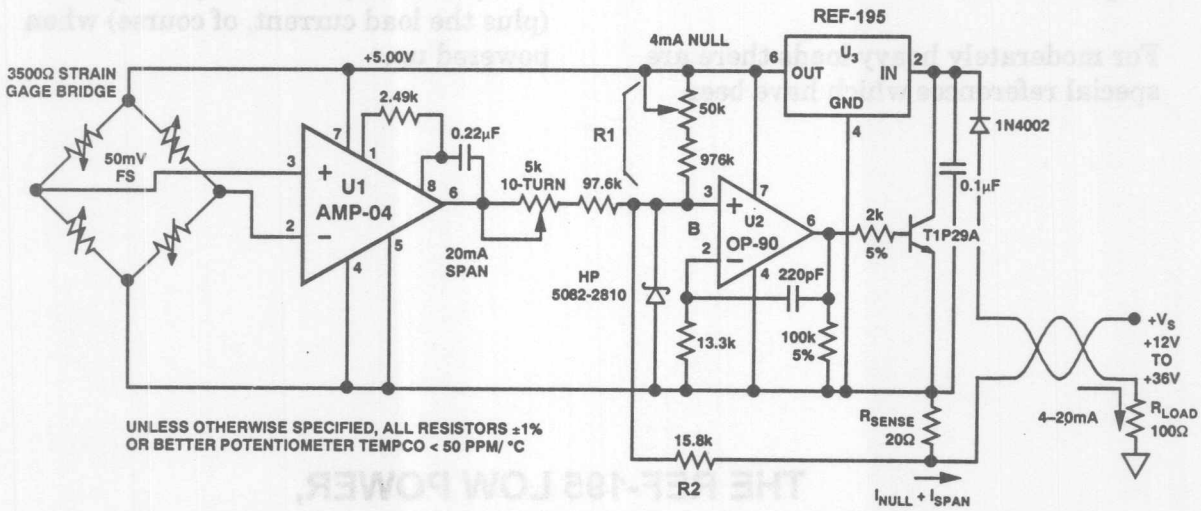


Figure 5.16

When the bridge signal output is zero, the AMP-04's output is also 0V relative to the floating reference. The 4mA output current is derived from the ratio of R1 to R2, the feedback resistor. This develops a 80mV across R_{SENSE}, the 20Ω current sense resistor (corresponding to 4mA output current). The low power consumption of the circuit allows the entire circuit to operate on the 4mA loop current so the entire circuit can be powered from a remote loop supply.

Pulse techniques to reduce power are made simple with the REF-195's shutdown ability. The circuit in Figure 5.17 is powered only during measurement. The bridge amplifier powers up and settles to better than 12-bits in under 400µs.

A PULSED STRAIN-GAUGE MEASUREMENT CIRCUIT HAS LOW POWER DRAIN AND PRECISION

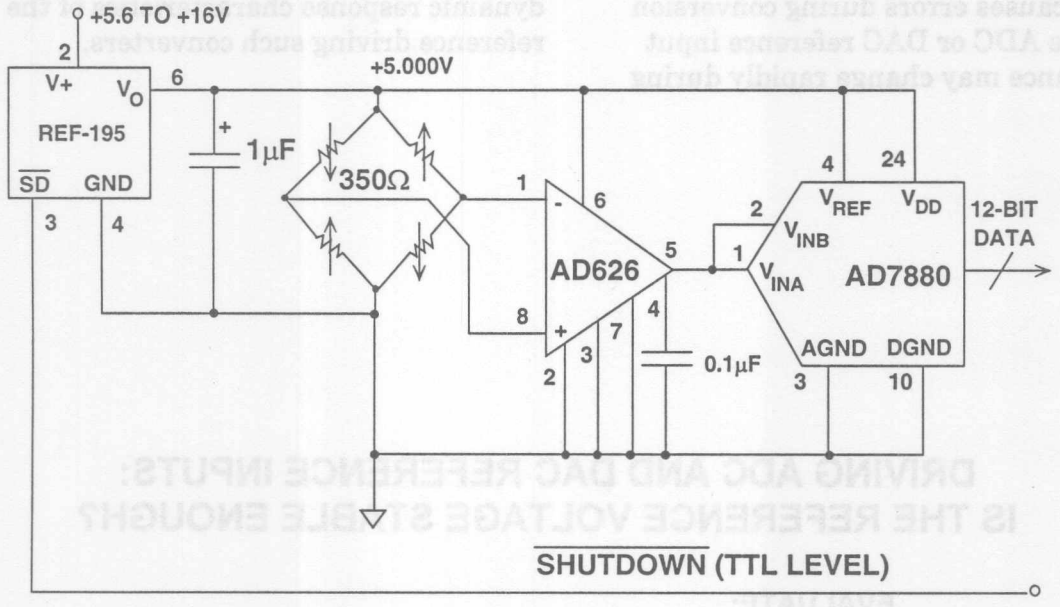


Figure 5.17

The AD680 is another reference which requires less than 250μA, and its features are shown in Figure 5.18.

THE AD680 LOW POWER, LOW COST 2.5V REFERENCE

- **Low Power Drain:** 250 μA max.
- **Low Drift:** 20 ppm/°C max.
- **Laser Trimmed Accuracy:** ± 5mV max.
- **Low Cost**

Figure 5.18

Driving the reference input of an ADC or DAC improperly can create noise which causes errors during conversion because ADC or DAC reference input impedance may change rapidly during conversion, disturbing the reference driving it. The user must evaluate the dynamic response characteristics of the reference driving such converters.

DRIVING ADC AND DAC REFERENCE INPUTS: IS THE REFERENCE VOLTAGE STABLE ENOUGH?

EVALUATE:

- **Initial Accuracy**
- **TC Drift**
- **Noise**
- **Dynamic Settling Characteristics**

Figure 5.19

For example, the reference input to a Sigma-Delta ADC may be the switched capacitor shown in Figure 5.20. The dynamic load causes current spikes in the reference as the capacitor is charged and discharged. As a result, noise may be induced on the ADC reference circuitry.

Although sigma-delta ADCs have an internal digital filter, transients on the reference input can still cause appreciable conversion errors. An example of sampling noise on a sigma-delta ADC reference is shown in Figure 5.21. The bottom trace shows the noise that is generated if the reference source impedance is too high. The dynamic load causes the reference input to shift by more than 5mV.

DYNAMIC LOAD EFFECTS OF DRIVING SIGMA-DELTA ADCs

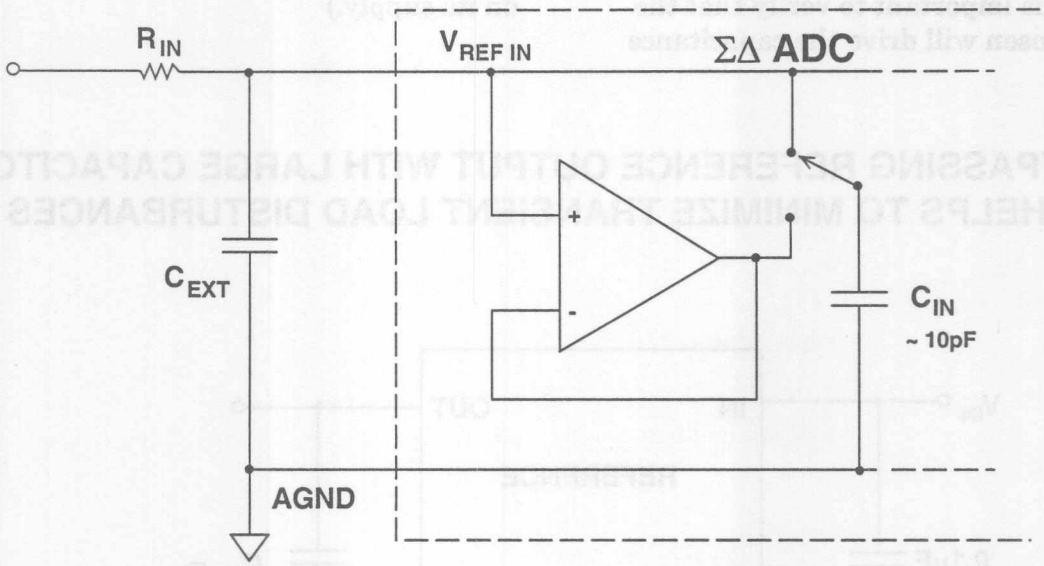
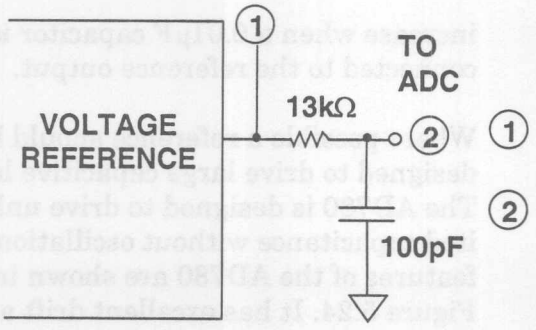
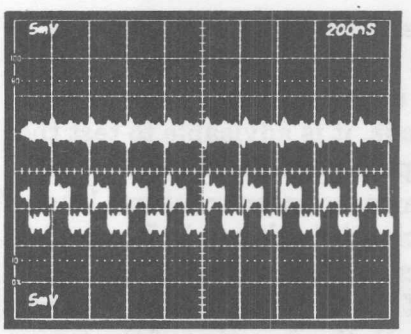


Figure 5.20

TYPICAL NOISE INDUCED AT THE REFERENCE INPUT OF A SIGMA-DELTA ADC





VERTICAL SCALE: 5mV/div.
HORIZONTAL SCALE: 200ns/div.

Figure 5.21

A bypass capacitor on the output of a reference may help it to cope with load transients, but many references are unstable with large capacitive loads, and it is important to verify that the one chosen will drive the capacitance required. (The input to all references should always be decoupled - with 0.1μF in all cases and with an additional 5-50μF if there is any LF ripple on its supply.)

BYPASSING REFERENCE OUTPUT WITH LARGE CAPACITOR HELPS TO MINIMIZE TRANSIENT LOAD DISTURBANCES

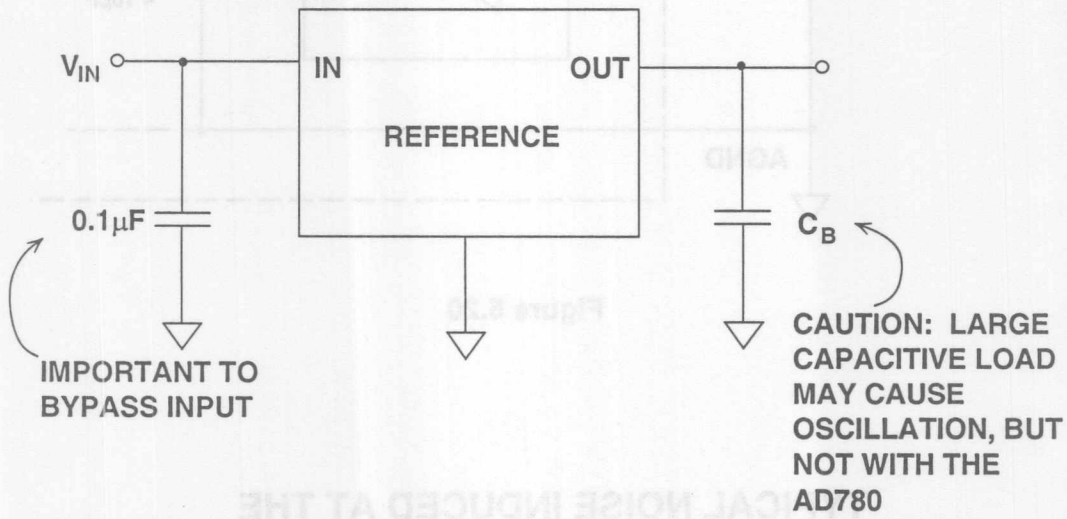


Figure 5.22

Since references do misbehave with transient loads, either by oscillating or by losing accuracy for comparatively long periods, it is advisable to test the pulse response of voltage references which may encounter transient loads. A suitable circuit is shown in Figure 5.23. In a typical voltage reference a step change of 1mA produces the transients shown. Both the duration of the transient, and the amplitude of the ringing increase when a 0.01μF capacitor is connected to the reference output.

Where possible a reference should be designed to drive large capacitive loads. The AD780 is designed to drive unlimited capacitance without oscillation. The features of the AD780 are shown in Figure 5.24. It has excellent drift and an accurate output in addition to low power consumption.

MAKE SURE REFERENCE IS STABLE WITH LARGE CAPACITIVE LOADS

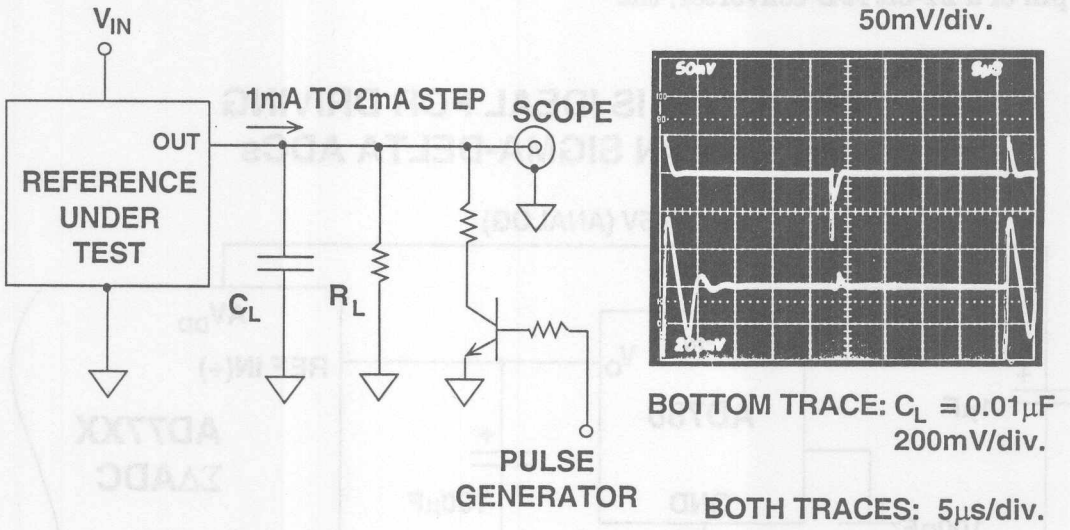


Figure 5.23

AD780 2.5V/3.0V HIGH PRECISION VOLTAGE REFERENCE DESIGNED TO DRIVE UNLIMITED CAPACITIVE LOAD

- **Ultra Low Drift:** 2 ppm/°C max.
- **Output Accuracy:** ± 1 mV max.
- **Low Noise (0.1Hz to 10Hz):** 4 µV p-p max.
- **Low Power:** 700 µA max.
- **Source and Sink Capability**

Figure 5.24

A reference device that can drive a large capacitive load can be used to minimize ADC reference noise. An example is shown in Figure 5.25, where the AD780 is shown driving the reference pin of a 21-bit A/D converter, the AD7710. At this resolution, even a little noise or drift can cause bad measurements. The 100µF reference bypass capacitor provides an exceptionally stable output.

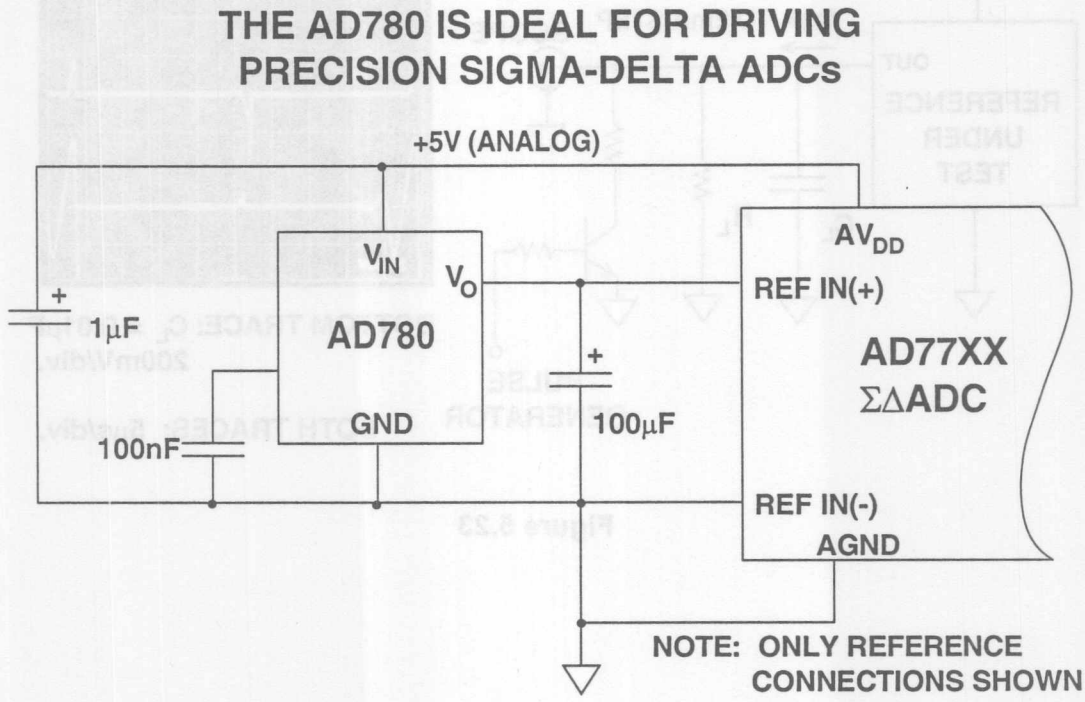


Figure 5.25

Large reference bypass capacitors are also useful when driving the reference inputs of successive-approximation ADCs. Figure 5.26 illustrates reference voltage settling behavior immediately following a "Conversion Start" command. A small capacitor (0.01µF) does not provide sufficient charge storage to keep the reference voltage stable during conversion, and errors may result. Decoupling with a >1µF capacitor maintains the reference stability during conversion.

SUCCESSIVE APPROXIMATION ADCs CAN PRESENT A DYNAMIC TRANSIENT LOAD TO THE REFERENCE

Solution: Bypass Reference Adequately

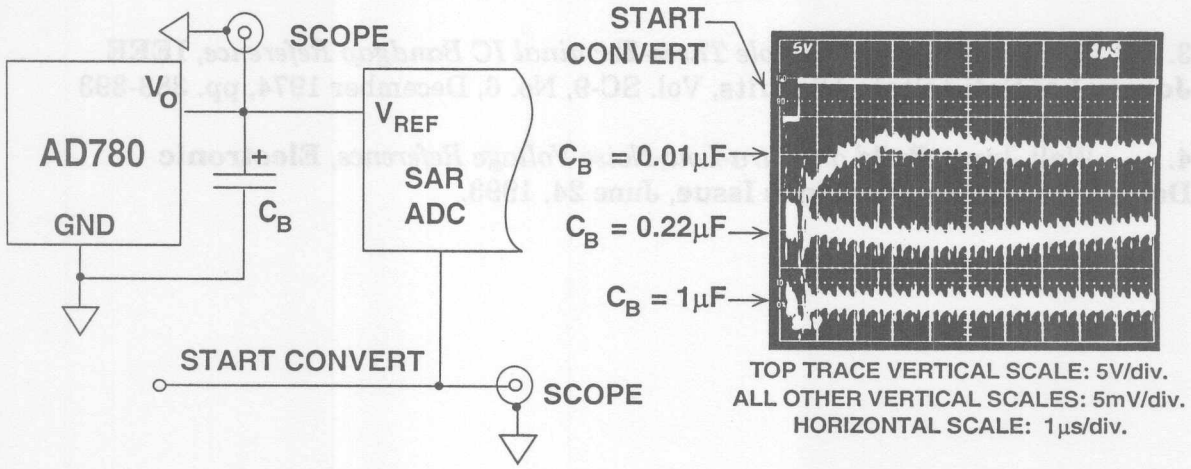


Figure 5.26

Where voltage references drive large capacitances it is important to realize that their turn-on time will be prolonged. Experiment may be needed to determine the delay before the output of the reference reaches full accuracy, but it will certainly be much longer than the time specified on the data sheet for the unloaded reference.

REFERENCES:

1. Adolfo Garcia, *Voltage-Reference Circuit Boasts Low Noise*, **EDN** March 30, 1992

2. **1990 High Speed Design Seminar**, Analog Devices

3. A. Paul Brokaw, *A Simple Three-Terminal IC Bandgap Reference*, **IEEE Journal of Solid State Circuits**, Vol. SC-9, No. 6, December 1974, pp. 388-393

4. Walt Jung, *Build an Ultra-Low-Noise Voltage Reference*, **Electronic Design Analog Applications Issue**, June 24, 1993.

SECTION 6

HIGH ACCURACY A/D CONVERSION

- SIGNAL CONDITIONING TRANSDUCER INPUT ADCs
- SINGLE-SUPPLY ADCs
- SERIAL OUTPUT ADCs
- COMPLETE DATA ACQUISITION ON A CHIP
- ULTRA-HIGH RESOLUTION DAS ON A CHIP

SECTION 6

HIGH ACCURACY A/D CONVERSION

Joe Buxton

SIGNAL CONDITIONING TRANSDUCER INPUT ADCs

The AD7710, AD7711, AD7712, and AD7713 are the first members of a family of sigma-delta converters designed for high accuracy, low frequency measurements. They have no missing codes at 24-bits and useful resolution of up to 21.5-bits. They all use the same sigma-delta core, and their main differences are in their analog inputs, which are optimized for different transducers.

The digital filter in the sigma-delta core may be programmed by the user for output update rates between 10Hz and 1kHz. The resolution is inversely proportional to the bandwidth. For example, for 21.5-bits of effective resolution, the output update rate cannot exceed 10Hz. The AD771x family is ideal for such sensor applications as those shown in Figure 6.1.

SIGNAL CONDITIONING, TRANSDUCER INPUT ADCs: THE AD7710, AD7711, AD7712, AD7713

- Ultra-High Resolution Measurement Systems
- Implemented Using ΣΔ Conversion
- Ideal for Applications Such As:
  - Weigh Scales
  - RTDs
  - Thermocouples
  - Strain Gauges
  - Process Control
  - Smart Transmitters
  - Medical

Figure 6.1

The AD771x family has a high level of integration which simplifies the design of data acquisition systems. The AD7710 (Figures 6.2 and 6.3) has two high impedance differential inputs that can be interfaced directly to many different sensors, including resistive bridges. The two inputs are selected by the internal multiplexer, which passes the signal to a programmable gain amplifier. The PGA has a digitally programmable gain range of 1 to 128 to accommodate a wide range of signal inputs. After the PGA, the signal is digitized by the sigma-delta modulator. The digital filter may be adjusted from 10Hz to 1kHz which allows various input bandwidths. To achieve this high accuracy, the AD771x family has four different internal calibration modes, including system and background calibration. All of these functions are controlled via a microcontroller compatible serial interface. A benefit of this serial interface is that the AD771x fits into a 24-pin package, giving it a small footprint for its high level of integration. All of the parts except the AD7713 can operate on a single +5V or dual ±5V supplies. The AD7713 is designed for single supply (+5V) low power applications only. The AD771x family has <0.0015% non-linearity.

All four devices in the AD771x family have identical structures of PGA, sigma-delta modulator, and serial interface. Their main differences are in their input configurations. The AD7710 has two low level differential inputs, the AD7711 two low level differential inputs with excitation current sources which make it ideal for RTD applications, the AD7712 has one low level differential input and a single ended high level input that can accommodate signals of up to four times the reference voltage, and the AD7713 is designed for loop-powered applications where power dissipation is important, the AD7713 consuming only 3.5mW of power from a single +5V supply.

THE AD771X-SERIES PROVIDES A HIGH LEVEL OF INTEGRATION IN A 24-PIN PACKAGE

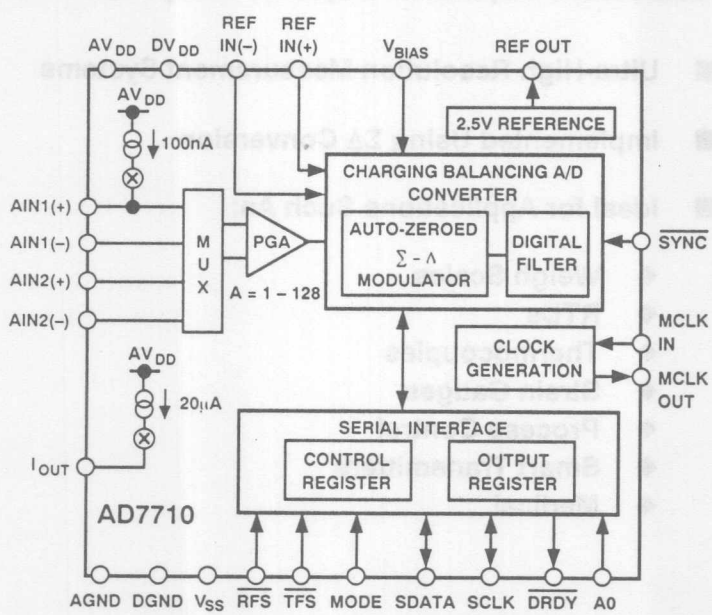


Figure 6.2

KEY FEATURES OF THE AD7710

- ±0.0015% Nonlinearity
- Two Channels with Differential Inputs
- Programmable Gain Amplifier (G = 1 to 128)
- Programmable Low Pass Filter
- System or Self-Calibration Option
- Single or Dual 5V Supply Operation
- Microcontroller Serial Interface

Figure 6.3

SUMMARY TABLE OF AD771X DIFFERENCES

- AD7710:
  - 2-Channel Low-Level Differential Inputs
- AD7711:
  - 1-Channel Low-Level Differential Input
  - 1-Channel Low-Level Single-Ended Input
  - Excitation Current Sources for 3 or 4-Wire RTDs
- AD7712:
  - 1-Channel Low-Level Differential Input
  - 1-Channel High-Level Single-Ended Input
- AD7713:
  - 2-Channel Low-Level Differential Inputs
  - 1-Channel High-Level Single-Ended Input
  - Excitation Current Sources for 3 or 4-Wire RTDs
  - Single 5V Operation Only
  - Low Power (3.5mW)
  - No Internal Reference

Figure 6.4

Because of the differences in analog interfaces each device is best suited to a particular sensor application. In other words, the sensor determines which converter should be used. Figure 6.5 lists the converters, and the sensors or applications to which they are best suited.

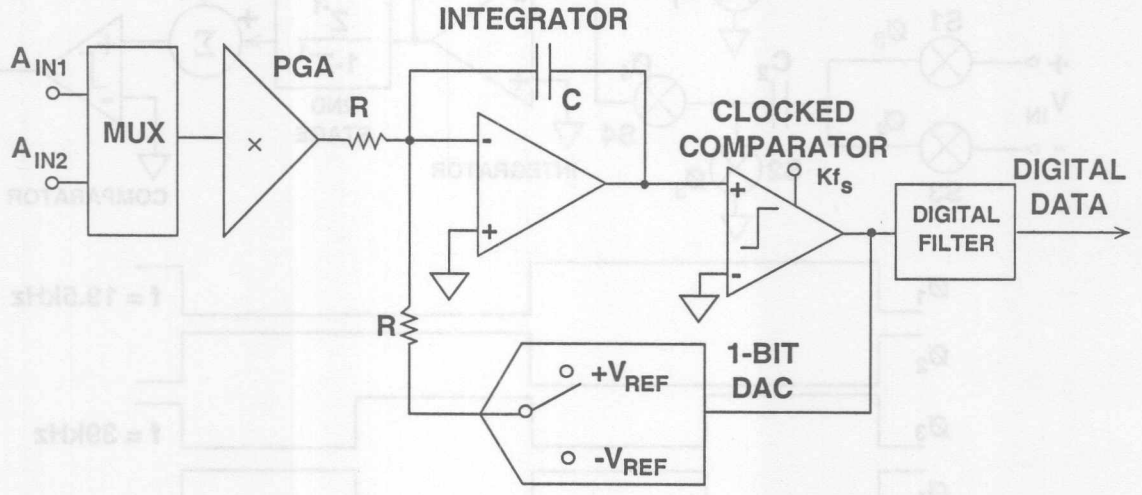
AD771X APPLICATIONS

- **AD7710:**
  - Weigh Scales
  - Thermocouples
  - Chromatography
  - Strain Gauge
- **AD7711:**
  - RTD Temperature Measurement
- **AD7712:**
  - Smart Transmitters
  - Process Control
- **AD7713:**
  - Loop-Powered Smart Transmitters
  - RTD Temperature Measurement
  - Process Control
  - Portable Instruments

Figure 6.5

Although the AD7710 is used as an example the following discussion applies to all the converters in the family (Figure 6.6). The modulator balances the signal input current to the integrator (derived from the input voltage applied to a resistor in the diagram, but quite often obtained by switched capacitor techniques in practical monolithic sigma-delta ADCs) with feedback current from the 1-bit DAC (a resistor and a changeover switch between $+V_{REF}$ & $-V_{REF}$) so that the net input current to the integrator, averaged over a long period, is zero. On each clock cycle the clocked comparator at the integrator output determines whether the output is above or below zero, and sets the DAC to bring the output back towards zero - the DAC only changes state on a clock.

THEORY OF OPERATION



Sigma-Delta Modulator Loop

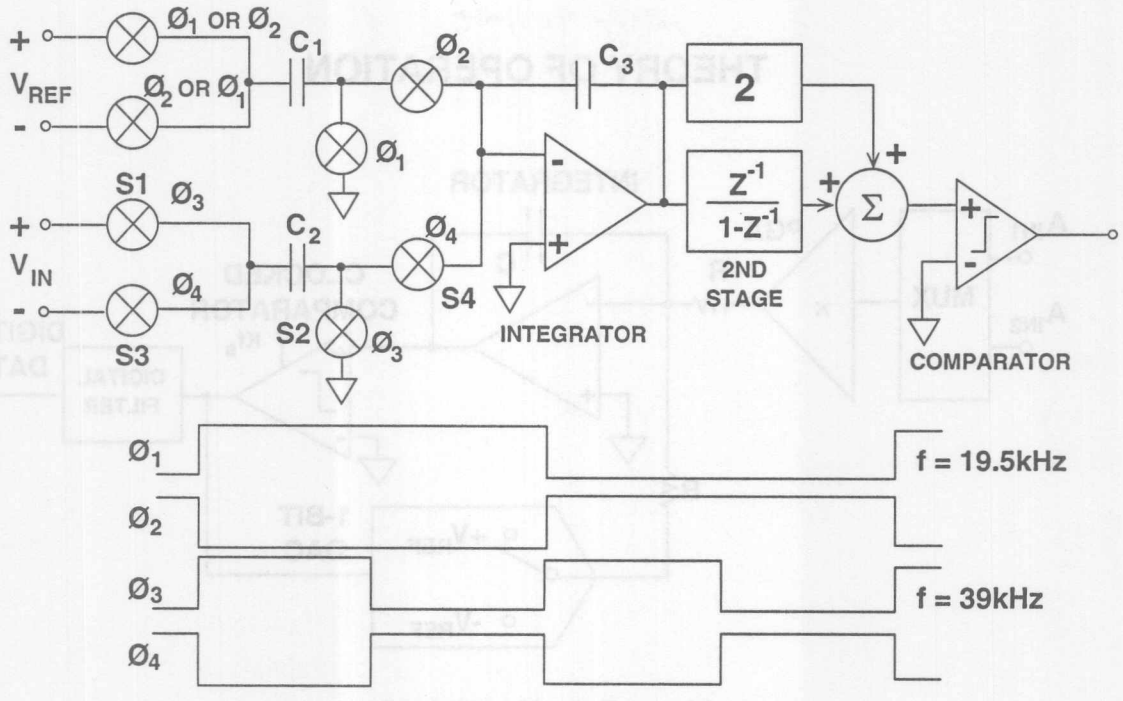
Figure 6.6

The output is therefore a synchronous bit stream. If it is fed to a counter, rather than to a digital filter, and integrated for an accurately timed period, we have a classical charge-balance ADC (which is closely related to the VFC plus frequency counter ADC), but very long integration periods are required for high resolution.

The sigma-delta ADC is also a charge-balance device, but the digital filter in the bit stream looks at rates of change as well as absolute numbers of 0s and 1s and thereby yields a high resolution conversion with a wider signal bandwidth and a higher output data rate. Understanding of the detailed operation of a sigma-delta ADC involves considerations of oversampling, noise shaping, and decimation and the interested reader should refer Section 14 of this book and References 1 & 3.

Up to this point the PGA has been shown as separate from the modulator. In fact it is part of the integrator. The differential signal input charges C2, which is then discharged into the integrator summing node (Figure 6.7). This is done by closing S1 and S2, and then, after opening them, closing S3 and S4. When the PGA has a gain of 1 this happens once per cycle of the basic 19.5kHz clock, but for gains of 2, 4 and 8 respectively it happens 2, 4 or 8 times per cycle. The integrator charge is balanced by switching charge in the same way from the reference into C1 and thence to the integrator summing node. The polarity of reference switched depends on the state of the comparator output.

ΣΔ MODULATOR INCLUDES A PGA FUNCTION



TIMING FOR GAIN OF 2

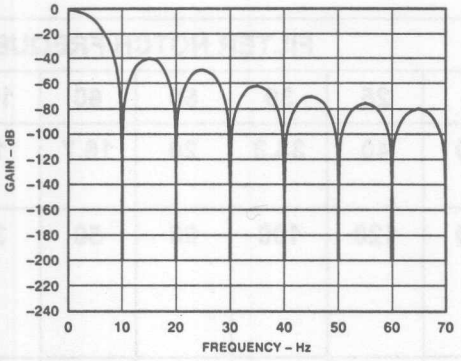
Figure 6.7

At a gain of 8 the sampling rate is 156kHz. Higher switching rates than this would not allow C2 sufficient time to charge, so for PGA gains greater than 8 the value of the reference capacitor, C1, is reduced, rather than the sampling rate being increased. Each time C1 is halved the gain of the system is doubled. The original value of C1 for gains of 1-8 is about 20pF, so for a gain of 16 it is 10pF and for a gain of 128 it is 1.25pF.

The digital filter has the $sinc^3$ response illustrated in Figure 6.8.The first notch in the filter response is programmable according to the formula:

$$f_{notch} = \left(\frac{f_{clkin}}{512}\right)\left(\frac{1}{\text{Decimal Value of Digital Code}}\right)$$

DIGITAL FILTER FREQUENCY RESPONSE



- Response Follows a $\text{sinc}^3 = \left(\frac{\sin x}{x}\right)^3$
- First Notch Frequency is Programmable and given by:

$$f_{notch} = \left(\frac{f_{clkin}}{512}\right)\left(\frac{1}{\text{Decimal Value of Digital Code}}\right)$$

- For f_{clkin} = 10MHz, 9.76Hz ≤ f_{notch} ≤ 1.028kHz

Figure 6.8

The notch frequency is 3.82 times the -3 dB frequency, so the notch frequency must be chosen so that the maximum signal frequency falls within the filter passband.

The lower the notch frequency the lower the noise bandwidth and therefore the higher the resolution of the converter. Moreover, the PGA gain will also set limits on the achievable resolution. With a 5V span 1 LSB in a 24-bit system is only 300nV - with a gain of 128 it is 2.3nV!

As is evident from their pipeline architecture, sigma-delta ADCs have a conversion time which is related to the bandwidth of the digital filter:- the narrower the bandwidth, the longer the conversion. For a 10Hz notch frequency the AD7710 has a 10Hz output data rate.

When the input to a sigma-delta ADC changes by a large step the entire digital filter must fill with the new data before the output becomes valid, which is a slow process. This is why sigma-delta ADCs are sometimes said to be unsuitable for multi-channel multiplexed systems - they are not, but the time taken to change channels can be inconvenient. In the case of the AD771X four conversions must take place after a channel change before the output data is again valid (Figure 6.9). The $\overline{\text{SYNC}}$ input pin resets the digital filter and, if it used, data is valid on the third output afterwards, saving one conversion cycle (when the internal multiplexer is switched the $\overline{\text{SYNC}}$ is automatically operated). The $\overline{\text{SYNC}}$ input also allows two AD771X ADCs to be synchronized.

THE RATE OF CONVERSION AND SETTLING TIME DEPENDS ON THE FILTER SETTING

	FILTER NOTCH FREQUENCY (Hz)								
	10	25	30	50	60	100	250	500	1k
CONVERSION TIME (ms)	100	40	33.3	20	16.7	10	4	2	1
MUX SWITCHING OR FULLSCALE WITH $\overline{\text{SYNC}}$, SETTLING TIME (ms)	300	120	100	60	50	30	12	6	3
ASYNCHRONOUS FULLSCALE SETTLING TIME (ms)	400	160	133.3	80	66.7	40	16	8	4

- Conversion Time = $\frac{1}{\text{Filter Notch Frequency}}$
- Digital Filter Requires Settling Time for Input Step Changes
- Use $\overline{\text{SYNC}}$ Input to Decrease Settling Time

Figure 6.9

Although the AD771X sigma-delta ADCs are 24-bit devices, it is not usually possible to obtain 24 bits of useful resolution, because noise limits the amount of useful data available. We thus confront the concept of "Effective Number of Bits" or ENOB. This is a measure of the useful signal-noise ratio of an ADC.

The full scale signal is the voltage difference between the most negative input the ADC will accept without overloading and the most positive one. The RMS noise is the amount that the output varies from conversion to conversion when a fixed input is applied to the ADC.

Noise may be generated by signal leakage and components (resistors and active devices) in the ADC. There is also intrinsic *quantization noise* which is inescapably linked to the analog-digital conversion process. Sigma-delta ADCs use special techniques to shape their quantization noise and thus reduce their oversampling ratio for a given ENOB, but they cannot eliminate quantization noise entirely. (Section 14 of this book and References 1 & 3)

DETERMINING EFFECTIVE RESOLUTION

- Effective Number of Bits (ENOB) = $\log_2\left(\frac{\text{Full Scale Signal}}{\text{RMS Noise}}\right)$
- Output RMS Noise = Effective Noise in the Digital Output Code
- ENOBs is Greatest at Low Filter Frequency and Low Gain

Figure 6.10

Figure 6.11 shows how RMS noise in an AD7710 varies with gain and notch frequency. Figure 6.12 gives the same results in terms of ENOB. Voltage noise drops with increasing sampling rate (remember that at gains of >8 the sample rate does not increase further) but rises, as we should expect, with increasing filter bandwidth. At higher bandwidths the dominant noise is the quantization noise, which occurs after the PGA and is therefore independent of gain. In general both noise and ENOB drop monotonically with increasing gain and increasing bandwidth (there is a small ENOB anomaly at 1kHz and gains between 2 and 32) but the drops are not linear for the reasons we have discussed: in some regions (e.g., 10Hz / gain = 1-8) ENOB does not vary much with gain, in others (e.g., 10-60 Hz / gain = 128) it does not vary much with bandwidth. In others it does vary with both.

NOISE VARIES AS A FUNCTION OF GAIN AND FILTER CUTOFF FREQUENCY

First Notch of Filter and O/P Data Rate	-3dB Frequency	Typical Output RMS Noise (μV)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz	2.62 Hz	1.7	1.0	0.5	0.36	0.36	0.36	0.36	0.36
25 Hz	6.55 Hz	4.9	2.2	1.2	0.6	0.36	0.36	0.36	0.36
30 Hz	7.86 Hz	6.1	2.4	1.2	0.84	0.5	0.36	0.36	0.36
50 Hz	13.1 Hz	7.5	3.8	2.0	1.0	0.6	0.5	0.5	0.45
60 Hz	15.72 Hz	8.5	4.0	2.0	1.0	0.6	0.5	0.5	0.45
100 Hz	26.2 Hz	13	6.4	3.7	1.8	1.1	0.9	0.65	0.65
250 Hz	65.5 Hz	130	75	25	12	7.5	4	2.7	1.7
500 Hz	131 Hz	600	260	140	70	35	25	15	8
1 kHz	262 Hz	3100	1600	700	290	180	120	70	40

- Quantization noise arises from digitization. After PGA, so it is independent of gain.
- Device noise is determined by kT/C noise. Decreases for gains up to 8.

Figure 6.11

EFFECTIVE RESOLUTION VERSUS GAIN AND FIRST NOTCH FREQUENCY

First Notch of Filter and O/P Data Rate	-3dB Frequency	Effective Resolution (ENOBs)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
10 Hz	2.62 Hz	21.5	21.5	21.5	20.5	19.5	18.5	17.5	16.5
25 Hz	6.55 Hz	20	20	20	20	19.5	18.5	17.5	16.5
30 Hz	7.86 Hz	19.5	20	20	19.5	19.5	18.5	17.5	16.5
50 Hz	13.1 Hz	19.5	19.5	19.5	19.5	19	18.5	17.5	16.5
60 Hz	15.72 Hz	19	19.5	19.5	19.5	19	18.5	17.5	16.5
100 Hz	26.2 Hz	18.5	18.5	18.5	18.5	18	17.5	17	16
250 Hz	65.5 Hz	15	15	15.5	15.5	15.5	15.5	15	14.5
500 Hz	131 Hz	13	13	13	13	13	12.5	12.5	12.5
1 kHz	262 Hz	10.5	10.5	11	11	11	10.5	10	10

- $\text{ENOBs} = \frac{2 \times V_{REF}}{\text{GAIN}} \bullet \frac{1}{\text{RMS NOISE}}$
- Highest resolution occurs at low gains and low frequency

Figure 6.12

It is important to distinguish between RMS and peak-to-peak noise. Noise in a sigma-delta ADC has a gaussian (or near gaussian) distribution. This means that if you wait long enough any value of peak noise will eventually occur and it is not possible to write a specification *absolutely* prohibiting a specified value of noise peak. For practical purposes the peak-to-peak noise is defined as 6.6 times the RMS noise, since such peaks occur less than 0.1% of the time. The noise specified in the ENOB table in Figure 6.12 is expressed in RMS terms. If a figure for "noise-free" code is required it will be 3-bits worse: 20-bits ENOB becomes 17-bits noise-free code, etc. Since most applications are concerned with noise *power*, however, the RMS ENOB figure is the more commonly used.

This does not mean that the original 24-bit resolution is pointless, however. Additional filtering, to narrower bandwidths than the internal filter is capable of, can further improve the resolution and ENOB at the expense of very long conversion times.

ESTIMATING NOISE-FREE CODES

- Determined Using Peak-to-Peak Noise
- Output RMS Noise × 6.6 = Peak-to-Peak Noise
- Factor of 6.6 is Approximately Equal to 3 bits
- Subtract 3 bits from Effective Resolution Given in Figure 6.12 to Determine Noise Free Codes
- Further Filtering Will Realize Figure 6.12 Values

Figure 6.13

The results in Figures 6.11 and 6.12 assume that the input and reference signals are noise free. Noisy inputs (and the reference is an input) reduce the effective resolution. For this reason, careful attention must be paid to external noise sources. Figure 6.14 lists aspects of board layout which may affect system noise and hence the ENOB of the AD7710. Many of these issues are discussed in detail in the 1992 Amplifier Applications Guide. If external amplifiers are used, low noise devices such as the OP-213 and AD797 should be chosen.

To determine if external amplifiers will lower the AD7710 system resolution,

the total additional noise (in the bandwidth 0.1 Hz to the cutoff frequency set in the AD7710) should be calculated and compared with the RMS noise figures given in Figure 6.11. (Uncorrelated noise adds by root sum of squares, so if the additional noise is <50% of the AD7710 noise it may be ignored, but if it exceeds this level its effect on system performance must be studied carefully.)

OPTIMIZING NOISE PERFORMANCE

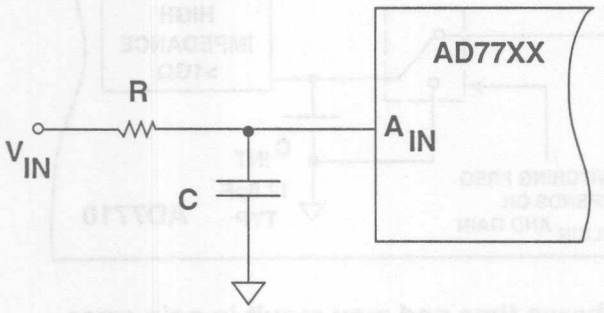
- Pay Attention to Layout!
- Use Ground Planes
- Keep Analog PCB Tracks Short
- Use Low Noise Amplifiers (AD797, OP-213, OP-177, AD707)
- Connect Analog and Digital Grounds of Converters Together at the Device and Connect them to Analog Ground
- Route Digital PCB Tracks Clear of Analog Tracks
- Filter Signal and Reference Inputs
- Minimize Reference Noise
- The Evaluation Board is an Example of Good Layout

Figure 6.14

An anti-aliasing filter on the input of the AD7710 will improve its noise performance because the modulator does not reject noise at integer multiples of the sampling frequency. (Figure 6.15) The internal analog front end does provide some filtering at these frequencies (the attenuation at 19.5kHz is approximately 70dB) but high level wideband noise can degrade system ENOB. A simple RC low-pass filter, ideally with a cut-off well below 19.5kHz, is generally sufficient, but the resistor must not be so large that it affects gain accuracy of the AD7710.

A simplified model of the analog input of the AD7710 is shown in Figure 6.16. It consists of a resistor of approximately 7kΩ connected to the input terminal and to an analog switch which switches an 11.5pF capacitor between the resistor and ground with a mark-space ratio of 50%. The switching frequency depends on f_{clkin} and the gain which is being used: with a gain of unity and the standard clock frequency of 10MHz the switching frequency is 19.5kHz, and at gains of 2, 4 and 8 or more it is 39, 78 and 156kHz respectively.

ANTIALIASING FILTER HELPS REDUCE NOISE



- Digital filter does not reject noise at integer multiples of f_s ($n \times 19.5kHz$, where $n = 1, 2, 3, \ldots$)
- RC Low Pass filter on the inputs prevents aliasing and limits noise
- Select R small enough to prevent gain error

Figure 6.15

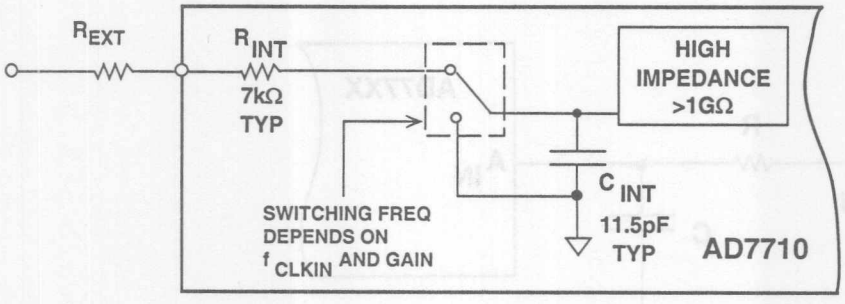
If the converter is working with an accuracy of 20-bits the capacitor must charge with an accuracy of 20-bits. The input RC time constant is 80ns. If the charge is to achieve 20-bit accuracy it must charge for at least 14× the time constant, or 1.13µs. Any external resistor in series with the input will increase the time constant, and the chart in Figure 6.16 shows acceptable values of series resistance necessary to maintain 20-bit performance.

To determine the minimum charge time for 20-bit performance with an external resistance R_{ext} we use the equation:

$$\text{Minimum Charge Time} = 14(R_{ext} + 7k\Omega) \times 11.5pF$$

The minimum charge time must be less than half the period of the switching signal used (it has a 50% duty cycle). The fastest switching frequency with the standard 10MHz clock is 156kHz, and half of that clock period is 3.2 µs, which allows a maximum R_{ext} of 12.8 kΩ. At lower gains R_{ext} may be larger.

ANALOG INPUT STRUCTURE



- R_{EXT} increases C_{INT} charge time and may result in gain error
- Charge time dependent on the input sampling rate and therefore gain
- Use following R_{EXT} values to maintain 20 bit accuracy:

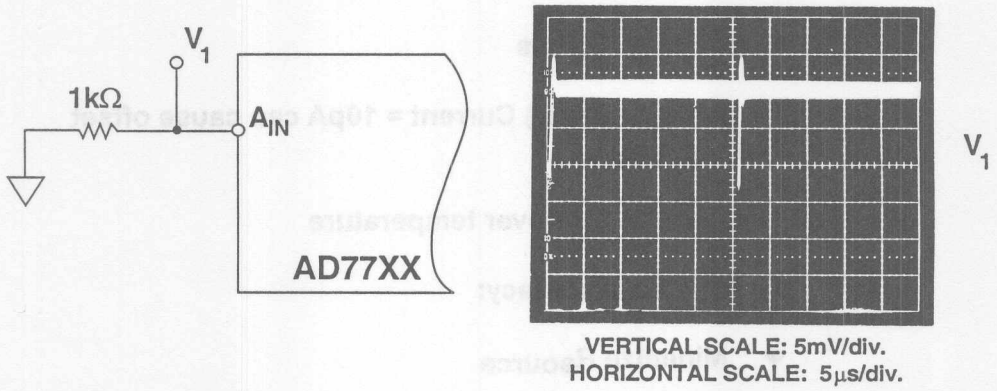
GAIN:	1	2	4	8-128
R_{EXT} :	<145kΩ	<70.5kΩ	<31.8kΩ	<13.4kΩ

Figure 6.16

It is not practical to use R_{ext} in conjunction with a capacitor to ground from the input pin of the AD7710 to make an anti-aliasing filter, unless the capacitor is dramatically larger than the 11.5pF C_{int}. This is because C_{int} is discharged on every sampling clock cycle and will recharge from the filter capacitor. Therefore, either the filter capacitor must be so large that charging C_{int} from it changes its voltage by less than an LSB at 20-bits (i.e. it is larger than 11.5μF), or the time constant $R_{ext}C_{ext}$ must be short enough for C_{ext} to recharge before the next clock cycle - in which case $R_{ext}C_{ext}$ does not make an anti-aliasing filter.

Some successive approximation and sub-ranging ADCs draw transient currents at their analog inputs which load their analog drive circuitry and cause errors. Often special drive amplifiers with low output impedance at the conversion clock frequency are necessary to avoid this problem, but these problems do not occur with the very small transient loads of the AD771X devices. The oscilloscope photograph in Figure 6.17 shows the transient current in an AD7710. It was taken with a 1kΩ resistor in series with the input to measure the change in current. This circuit produces a 15mV spike of less than 1μs duration. The peak pulse current is only 15μA, which permits the use of quite high impedance signal sources with no risk of degrading the ENOB.

INPUT TRANSIENT LOADING DOES NOT CAUSE CONVERSION ERRORS



- Transient settles quickly and does not affect conversion
- Inputs can accommodate high bridge resistances

Figure 6.17

The AD771x family was designed to simplify transducer interfacing. Many types of transducer can be connected directly to the input of one of the AD771x family without additional circuitry, but some care is necessary to achieve the best possible accuracy:- noise needs to be minimized (a simple capacitor across a resistive sensor may be all the filtering that is needed, but this must be checked - noise is particularly important because noise cannot be removed by the system calibration which eliminates gain and offset errors); transducer source impedance may affect charge times (as mentioned above); and bias currents flowing in high impedance transducers may cause errors, although these can be removed by system calibration. In general system calibration can remove most DC errors in systems using the AD771X family.

TRANSDUCER CONNECTION CONSIDERATIONS

- Filter Noisy Signals
- DC Leakage (bias) Current = 10pA can cause offset with R_{source}
- This causes drift over temperature
- To Maintain Accuracy:
  - Minimize R_{source}
  - Use differential inputs and balance R_{source}
  - Use system calibration

Figure 6.18

As discussed in Section 1, circuitry connected to transducers must generally be protected against over-voltage from ESD or noise pickup. If signals are likely to go outside the positive or negative supplies some form of clamp is necessary to keep them within them. Figure 6.19 shows a suitable circuit for protecting AD771X devices. The AD7710 has internal ESD protection diodes between the input and both supplies which conduct when the input exceeds either supply by more than about 0.6V. Excessive current in these diodes will vaporize metal tracks on the chip and damage the circuit, so an external resistor, R_p, is necessary to limit current to a safe 5mA during over-voltage events. R_p may be determined by a simple calculation:

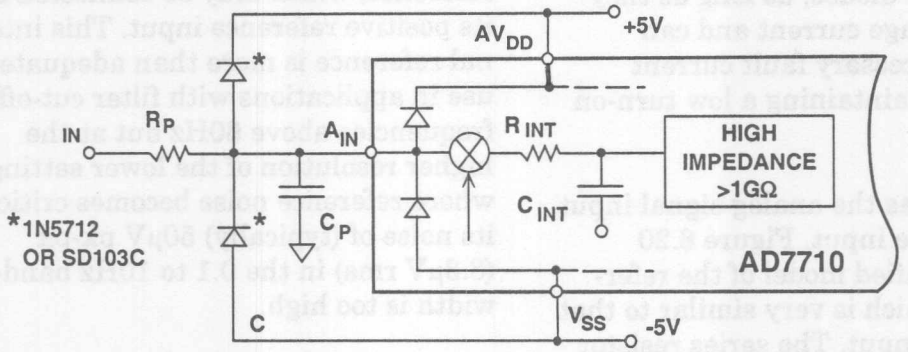
$$R_p = \frac{V_{max} - V_{supply}}{5\,mA}$$

R_p will contribute noise to the system (the basic Johnson noise equation applies:

$$e_n = \sqrt{4kTBR_p}$$

where k is Boltzmann's Constant, T is the absolute temperature and B is the bandwidth). If the noise due to R_p is too high, R_p can be reduced if external schottky diodes are used in addition to the diodes on the chip.

INPUT OVERVOLTAGE PROTECTION



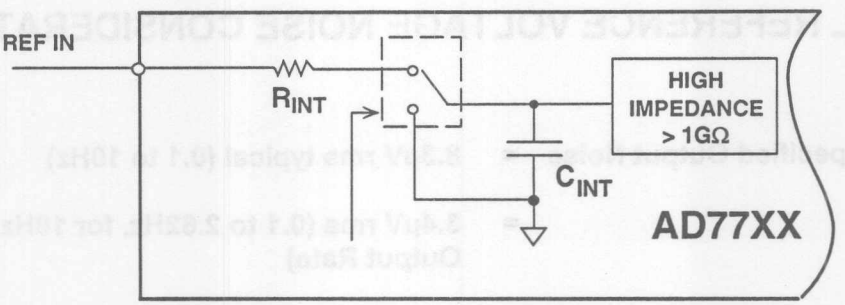
- Internal ESD protection diodes clamp input to within 0.6V of either supply.
- Limit current due to overvoltage to less than 5mA.

$$R_P = \frac{A_{inmax} - AV_{DD}}{5mA}, \text{ or } \frac{|A_{inmin}| - |V_{SS}|}{5mA}, \text{ whichever is greater.}$$

- External Schottkys can be added to reduce the size of R_P.
- Include C_P to filter noise due to R_P.

Figure 6.19

REFERENCE VOLTAGE CONSIDERATIONS



PGA GAIN	1	2	4	8	16	32	64	128
C_{INT} (pF)	20	20	20	20	10	5	2.5	1.25

- Antialiasing filter needed if reference is noisy
- Minimal transient load is similar to analog input

Figure 6.20

There are no special requirements for these schottky diodes, as long as they have low leakage current and can handle the necessary fault current levels while maintaining a low turn-on voltage.

As important as the analog signal input is the reference input. Figure 6.20 shows a simplified model of the reference input, which is very similar to that of the analog input. The series resistor is 5kΩ and the value of the capacitor depends on the gain setting. For gains of 1-8 the capacitor is 20pF. Above 8 the capacitor's value is halved for each doubling of gain.

An important consideration in choosing a reference for the AD7710 is noise. Many references have output noise which exceeds that of the AD7710 and causes reduced accuracy. Filtering will help in such cases but a low noise reference should be selected wherever possible.

The AD7710 has an internal 2.5V reference, which may be connected to its positive reference input. This internal reference is more than adequate for use in applications with filter cut-off frequencies above 60Hz but at the higher resolution of the lower settings, where reference noise becomes critical, its noise of (typically) 50μV pk-pk (8.3μV rms) in the 0.1 to 10Hz bandwidth is too high.

If the noise is 8.3μV (rms) in a 10Hz bandwidth it is 3.4μV in the 2.62Hz bandwidth associated with a 10Hz update rate. Since the AD7710 has an effective noise of 1.7μV rms this reference noise will increase the effective noise to 3.8μV rms and reduce the ENOB from 21.5 to 20.5. A low noise external reference is evidently necessary to improve resolution. (Actual measurements show that the degradation, though real, is a little less than this, but a better reference is still necessary.)

INTERNAL REFERENCE VOLTAGE NOISE CONSIDERATIONS

- Specified Output Noise = 8.3μV rms typical (0.1 to 10Hz)

  = 3.4μV rms (0.1 to 2.62Hz, for 10Hz Output Rate)

- Noise adds to device noise shown in Figure 6.11

  AD7710 Noise = 1.7μV rms (G = +1)

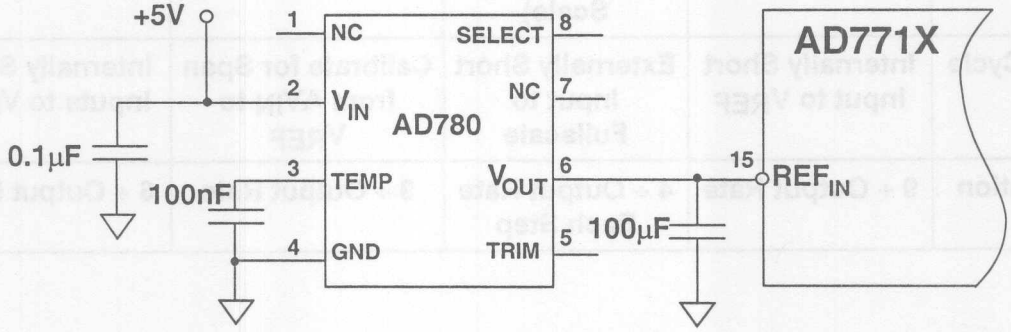
  $$\text{Total Noise} = \sqrt{(1.7\mu V)^2 + (3.4\mu V)^2} = 3.8\mu V \text{ rms, or } 25\mu V \text{ p} - \text{p}$$

- This reduces ENOB from 21.5 to 20.5 bits

Figure 6.21

The AD780 2.5V reference has noise of 316nV rms in the range 0.1 to 10Hz. This gives 0.1µV rms noise in the 2.62Hz bandwidth associated with a 10Hz update rate, which is negligible compared to the noise of the AD7710. With output rates of 1kHz or more, and cutoff frequency of 262Hz, the noise of the AD780 may be reduced by 50% if a 100µF capacitor is connected to its output (unlike many IC voltage references the AD780 is stable with all values of capacitive load).

USE A LOW NOISE EXTERNAL REFERENCE FOR OPTIMUM RESOLUTION



- AD780 has 100nV/√Hz noise at 10Hz
- Total noise for AD771X Notch Frequency of 10Hz:

  RMS Noise = (100nV/√Hz) √2.62Hz = 0.16µVrms
- Well below noise of AD771X

Figure 6.22

DC errors also affect conversion accuracy, but AD771X devices can calibrate themselves to correct DC errors. Every member of the family has four different calibration modes. These are summarized in Figure 6.23 and comprise Self Calibration, System Calibration, System-Offset Calibration, and Background Calibration. Each calibration cycle contains two conversions, one each for zero-scale and for full-scale calibration.

AD771X OFFERS 4 CALIBRATION OPTIONS

	SELF-CALIBRATION	SYSTEM CALIBRATION	SYSTEM OFFSET CALIBRATION	BACKGROUND CALIBRATION
1st Cycle	Internally Short Inputs to Ground	Externally Short Inputs to Ground (Zero-Scale)	Externally Short Inputs to Zero-Scale	Internally Short Inputs to Ground
2nd Cycle	Internally Short Input to V_{REF}	Externally Short Input to Fullscale	Calibrate for Span from AV_{IN} to V_{REF}	Internally Short Inputs to V_{REF}
Duration	9 ÷ Output Rate	4 ÷ Output Rate Each Step	9 ÷ Output Rate	6 ÷ Output Rate

Figure 6.23

To initiate a calibration cycle the appropriate code must be sent to the control register. After the code is sent, the AD7710 automatically conducts the entire operation, and clears the control register of the calibration command so that a separate command to stop calibration is not necessary. Since the filter in the sigma-delta converter must purge itself of its previous result for four output update cycles whenever the input sees a full-scale step the total calibration operation takes nine such cycles.

Self Calibration removes errors in an AD771X by connecting the input to ground and performing a conversion, and then connecting the input to Vref and performing another. The results of these conversions are used to calibrate the device.

Background Calibration is a variation of Self Calibration. The only difference is that when an AD771X is placed in Background Calibration mode, it continually calibrates itself at regular intervals without further instructions. This ensures that the AD771X remains calibrated regardless of drift. The Background Calibration cycle alternates calibration conversions with signal conversions: zero calibrate/ convert signal/full-scale calibrate/ convert signal/zero calibrate/etc. This provides continuous calibration but reduces the output data rate by a factor of six.

System Calibration is intended to calibrate all the elements prior to the ADC which may contribute to system errors, as well as the ADC itself. (For example an instrumentation amplifier

introduces errors into a system due to its own offset, drift and gain error. These errors can be removed by System Calibration.) However, System Calibration requires additional analog switches to connect *system* inputs to ground and a reference as well as to the original signal source. The first step in System Calibration requires external grounding of the system input terminal to calibrate out offsets. The second step requires that the input be connected to a reference, which calibrates gain error at full-scale. The System Calibration cycle requires the sending of two separate instructions to the control register as well as control of the analog switches at the system input. It must be repeated regularly to correct for drift with time and temperature.

The final calibration mode is System-Offset Calibration. This calibrates *system* offsets, and *the AD771X* gain. Again, it requires external analog switches at the system input, and separate instructions for zero and gain calibration. For the first cycle, the system input is connected to ground and the AD771X calibrates for system offsets. During the second cycle, the ADC input is connected to the reference for ADC gain calibration.

CALIBRATION ISSUES

- Always calibrate on power-up!
- Background calibration sequence: (Zero-Scale, Convert, Fullscale, Convert, Zero-Scale, Convert, . . .)

  This reduces the data rate by a factor of 6.
- $\overline{\text{DRDY}}$ signals when calibration cycle is complete by going low.
- $\overline{\text{DRDY}}$ may already be low if a conversion is taking place.

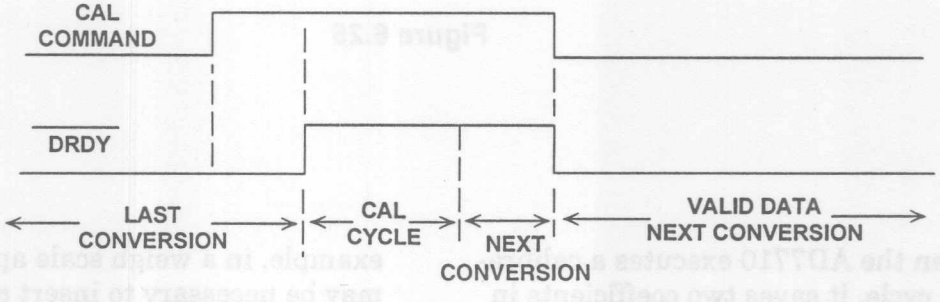


Figure 6.24

When calibration is complete $\overline{\text{DRDY}}$ goes low - but it does not necessarily go high as soon as the calibration command is sent to the ADC, there may be a delay of up to one output data cycle before it does so. Controllers should therefore look for a 0→1 transition, rather than the presence of a 0, on $\overline{\text{DRDY}}$ to signal the completion of a calibration after it has been commanded.

Calibration is crucial to achieving the rated accuracy of AD771X devices and

should be performed immediately after power-up and repeated regularly. A 2.5μV/°C temperature coefficient of input offset and a 2°C temperature change causes an lsb of error in a 20-bit 5V system. Any reference drift adds to the error. Frequent calibration ensures that temperature changes do not degrade the accuracy of conversions.

CALIBRATE OFTEN TO MAINTAIN ACCURACY

- Temperature Drift can cause errors
- Unipolar offset drift of 5μV is
  1 LSB in a 20 bit system (5V fullscale)
- Reference voltage drift adds to this error
- Therefore, to minimize drift errors, calibrate often.

Figure 6.25

When the AD7710 executes a calibration cycle, it saves two coefficients in internal registers. One register stores the full scale calibration coefficient, FSC, and the other stores the zero scale calibration coefficient, ZSC. Adjusting the calibration coefficients manually may be useful in some applications. For example, in a weigh scale application it may be necessary to insert an offset to account for a fixed weight. It is possible to read from and write to the calibration registers of members of the AD771X family, making adjustment of calibration coefficients a trivial task. (Figure 6.26)

MANUALLY ADJUSTING CALIBRATION COEFFICIENTS

- Perform a Self-Calibration Cycle for Desired Gain and Filter Settings
- Read Calibration Coefficients from Register
- Calculate New Coefficients Using Formulas in Figure 6.27
- Use Different Formula for Bipolar Case
- Write New Coefficients Back into Calibration Registers
- Reading and Writing to the Calibration Registers is Controlled by Operating Mode Bits, MD0 - MD2

Figure 6.26

The equations for adjusting calibration coefficients are given in Figure 6.27. The terms used are defined in Figure 6.28. The equations use the old calibration coefficients, the old data, and the desired new data. Before calculating new coefficients, a self calibration cycle should be performed at the gain and filter settings to be used to ensure that the old internal coefficients are current. To calculate the new full scale calibration coefficient, FSC_{NEW} the old full scale calibration coefficient, FSC_{OLD} must first be read from the register. Its value is multiplied by the ratio of the required full scale range to the old full scale range. The FSC is a gain coefficient. The formula to calculate the new zero scale calibration coefficient, ZSC_{NEW} is a little more complex, but the calculation is still straightforward and again based on the old coefficient, ZSC_{OLD} - plus the old data and the desired new data. Using these two simple formulas, the system software can quickly determine new calibration coefficients for a particular application, which may then be written into the calibration registers to replace the old coefficients. Reading and writing data in the calibration registers is controlled by the operating mode bits, MDO-MD2, in the control register.

CALCULATING CALIBRATION COEFFICIENTS

- $$FSC_{NEW} = FSC_{OLD}\left(\frac{FSR_{NEW} - ZSR_{NEW}}{FSR_{OLD} - ZSR_{OLD}}\right)$$
- Unipolar:

$$ZSC_{NEW} = ZSC_{OLD} - \left(\frac{ZSR_{NEW} \cdot FSR_{OLD} - ZSR_{OLD} \cdot FSR_{NEW}}{\frac{FSC_{OLD}}{2^{21}}(FSR_{NEW} - ZSR_{NEW})}\right)$$

- Bipolar:

$$ZSC_{NEW} = ZSC_{OLD} - \left(\frac{ZSR_{NEW} \cdot FSR_{OLD} - ZSR_{OLD} \cdot FSR_{NEW}}{\frac{FSC_{OLD}}{2^{20}}(FSR_{NEW} - ZSR_{NEW})}\right)$$

Figure 6.27

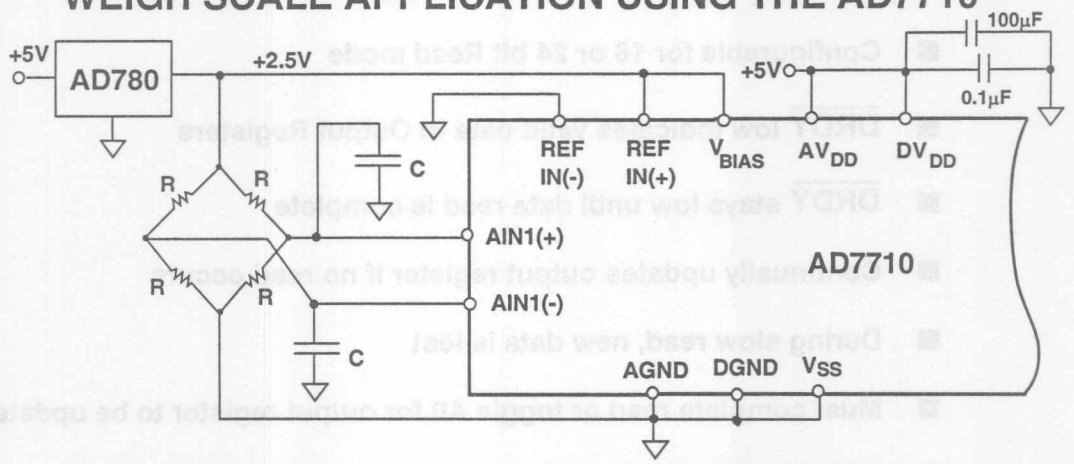
CALIBRATION COEFFICIENT TERMS DEFINED:

- FSC_{NEW} = New Fullscale Calibration Coefficient, Load into Register
- FSC_{OLD} = Old Fullscale Calibration Coefficient, Read from Register
- ZSC_{NEW} = New Zero Scale Calibration Coefficient, Load into Register
- ZSC_{OLD} = Old Zero Scale Calibration Coefficient, Read from Register
- FSR_{NEW} = New, Desired Fullscale Output Reading (Code)
- FSR_{OLD} = Old Fullscale Output Reading (Code)
- ZSR_{NEW} = New, Desired Zero Scale Output Reading (Code)
- ZSR_{OLD} = Old Zero Scale Output Reading (Code)

Figure 6.28

A typical application of the AD7710 is in a weigh scale (Figure 6.29). These generally use a resistive bridge as their sensing element and require resolution of at least 16-bits and often more. The AD7710 dramatically simplifies the design of such a system: the bridge is connected directly to its differential inputs, making an external instrumentation amplifier unnecessary. The excitation for the bridge, and the reference for the AD7710, are provided by an AD780, whose low noise helps to preserve the system ENOB. Because the system bandwidth is limited (both by the conversion rate selected and the filter capacitors on the bridge) the ENOB achievable is quite high (≈ 20-bits) but the conversion (and output data) rate is rather low at 10Hz.

WEIGH SCALE APPLICATION USING THE AD7710



- High impedance differential input interfaces directly to bridge
- External reference used for accuracy
- Wide range of impedances can be used for bridge
- Add capacitors to input to filter noise

Figure 6.29

The converters in the AD771x family all have the same serial interface, which is described in detail in the data sheet. They have a 24-bit control register that controls all their operations. Changing the PGA gain, starting a calibration, and changing the filter parameters are all accomplished by writing a 24-bit word to this register. On the other hand, data can be read either as a 16-bit or a 24-bit operation - one of the bits in the control register controls the size of the data word. The $\overline{\text{DRDY}}$ output indicates when a conversion is complete and valid data is available in the output register.

The output register is continually updated as new conversion take place, and if the data is not read it is overwritten by new data. However, if a conver-

sion finishes while data is being read from the output register, the new conversion results are lost. The benefit of this feature is that the data can be read slowly without any danger of its being corrupted by new conversion results. In fact, until all bits have been read from the output register, no new conversion results will appear, so a controller can read 8-bits from the register, service an unrelated interrupt, and return to read the remaining word of data without it being corrupted by the results of new conversions.

SERIAL INTERFACE ISSUES

- Configurable for 16 or 24 bit Read mode
- $\overline{\text{DRDY}}$ low indicates valid data in Output Registers
- $\overline{\text{DRDY}}$ stays low until data read is complete
- Continually updates output register if no read occurs
- During slow read, new data is lost
- Must complete read or toggle A0 for output register to be updated
- SCLK can run as slow as desired, remembering above
- Need to write all 24 bits to control register

Figure 6.30

Figure 6.31 shows an isolated 4-wire interface to the AD7713 using common opto-isolators. Over 6kV of isolation is possible. The $\overline{\text{TFS}}$, A0, and $\overline{\text{SYNC}}$ lines are tied together at the converter to minimize the number of control lines. Tying $\overline{\text{TFS}}$ to AO causes a write to the device to load data to the control register, and any read accesses the data register. The only restrictions of this method of control is that the controller cannot write to the calibration registers and cannot read from the control register. In many applications these capabilities are unnecessary. Four opto-isolators carry data and instructions from the controller to the ADC and a fifth, with a 74HC125 on each side of the isolation barrier, carries data to the controller. The AD7713 is ideal for this particular application because its low supply current minimizes the load on the isolated power supply.

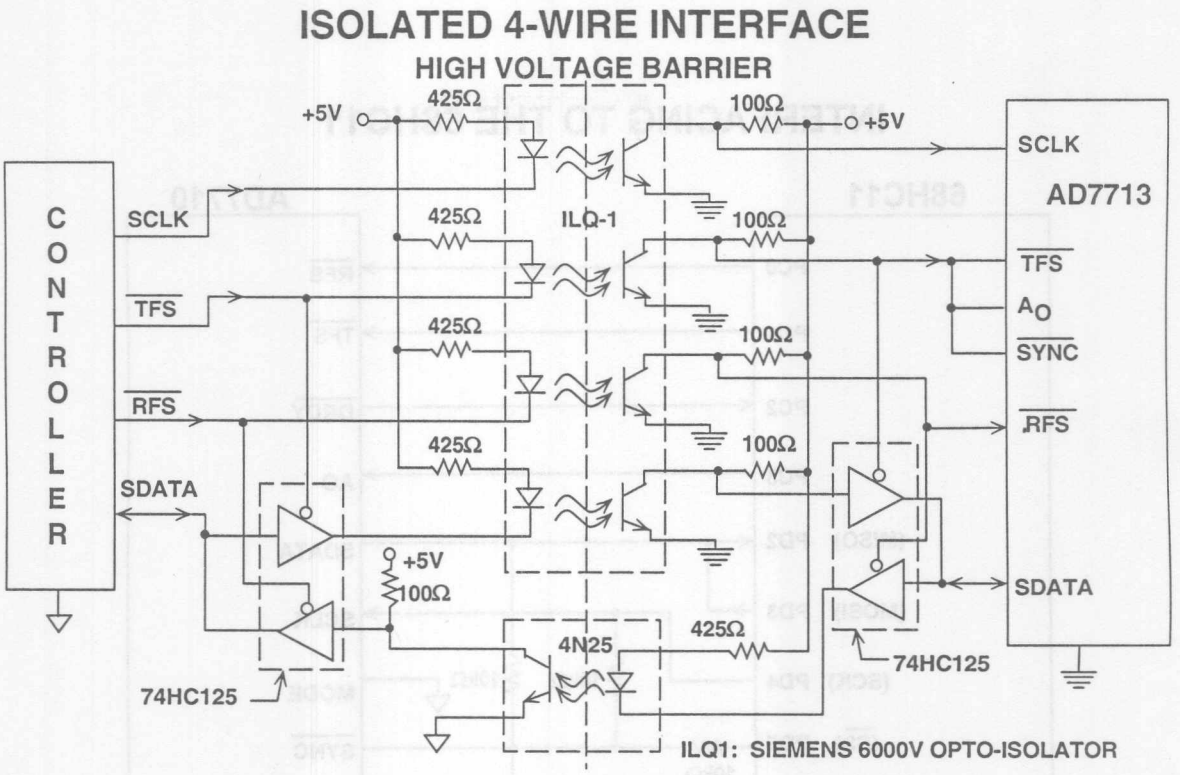


Figure 6.31

The AD771X family generally interfaces with some type of microprocessor. Their data sheet includes circuits and microcode for interfacing to the 8051 microcontroller and the ADSP-2105 DSP processor. Figure 6.32 shows how they may be interfaced to the 68HC11 microcontroller, and the code is included at the end of this section. The SPI serial port of the 68HC11 handles the sending and receiving of data to the AD771X, and pins PCO through PC3 control the different logic inputs. The 68HC11 should be configured in the master mode, as is explained in the assembly code at the end of this section.

INTERFACING TO THE 68HC11

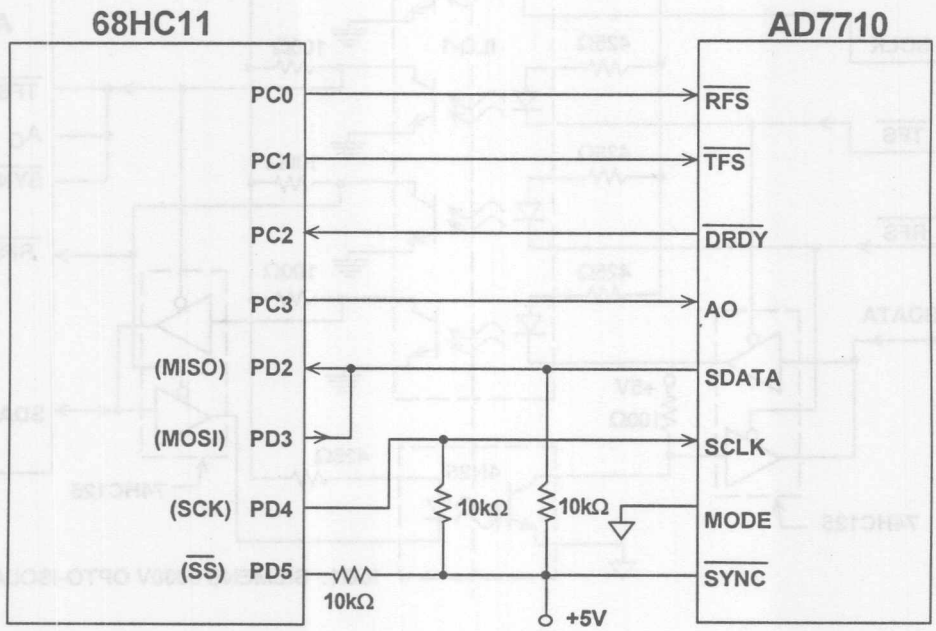


Figure 6.32

The AD771X sigma-delta converters are powerful tools for building high accuracy systems. Every one of them combines high resolution, system calibration, a programmable gain amplifier, and high impedance differential inputs with great ease of design. Their adjustable digital filters provides flexibility in the choice of data rates and resolution and their serial interface minimizes their pin count, so that they fit in a 24-pin skinny DIP package, providing a high degree of functionality in a small space.

MICROCODE FOR READING AND WRITING TO THE AD771X FAMILY FROM THE 68HC11 MICROCONTROLLER

```
* This program contains subroutines to read and write
* to the AD7710 family of ADCs from the 68HC11
* microcontroller.  These subroutines were developed for the
* 68HC11 Evaluation board, which is where the references to BUFFALO
* come from, in conjunction with the AD7710 Evaluation board.
* The following connections need to be made.
*  68HC11      AD7710
*  PC0         RFS
*  PC1         TFS
*  PC2         DRDY
*  PC3         A0
*  PD2,PD3     SDATA      10K pull-up resistor
*                         PD2 and PD3 attached together
*  PD4         SCLK       10K pull-up
*  PD5                    10K pull-up, no connection to AD7710
*
portc   equ    $1003
portd   equ    $1008
ddrd    equ    $1009
spcr    equ    $1028
spsr    equ    $1029
spdr    equ    $102a
ddrc    equ    $1007
*
```

```
        org     $C000
read    lds     #$CFFF    subroutine to read from the AD771X
*
        ldaa    #$fb      initialize port c ouputs:  11111011
        staa    ddrc      Set up drdy as input (PC2) and
*                         A0, RFS, TFS (PC3,PC0,PC1) as outputs
        ldaa    #$30      00110000
        staa    ddrd      MOSI is low for input,
*                         MISO is high, SCK as output
*
        ldaa    #$37      00110111
        staa    spcr      SPI system off, resets itself
*
        ldaa    #$77      01110111
        staa    spcr      Interrupts disabled, SPI system on,
*                         DWOM mode, 68hc11 is master,
*                         CPOL 0, CPHA 1, SCK=ECK/32
*
        ldy     #$1000
        bset    portc,y   $03   TFS and RFS set high
*
        bset    portc,y   $08   A0 high to read data
*                               set A0 low to read control reg.
*
        ldaa    spsr      Initial dummy read to clear port
        ldaa    spdr      and SPIF
*
        ldab    #$03      b counts to 0 when read finished
        ldx     #$00      x points to memory location where
*                         the data is stored. (24 bits wide)
*
pause   ldaa    #$04
        anda    portc
        bne     pause     Wait until DRDY is low
*
        bclr    portc,y   $01  Clear RFS for read
*
go1     staa    spdr      Start SCK
wait1   ldaa    spsr
        bpl     wait1     wait until SPIF flag is clear
        ldaa    spdr      and then read.
        staa    0,x       And then put in memory
*
        decb
        beq     fin1      if b=0 then finished reading
        inx               increment memory location for next byte
        jmp     go1
*
fin1    bset    portc,y   $09  set RFS and A0
*
        jmp     $e000     Return to BUFFALO
```

```
write   lds    #$cfff    subroutine to write to AD771X
        ldaa   #$fb
        staa   ddrc      Set up drdy as input (PC2) and
*                        A0, RFS, TFS (PC3,PC0,PC1) as outputs
        ldaa   #$37
        staa   spcr      SPI system off, resets itself
*
        ldaa   #$73
        staa   spcr      Interrupts disabled, SPI system on,
*                        DWOM mode, 68hc11 is master,
*                        CPOL=0, CPHA=0, SCK=ECK/32
        ldaa   #$38
        staa   ddrd      MOSI is high for output,
*                        MISO is low, SCK is high
        ldy    #$1000
        bset   portc,y   $03    Set TFS and RFS
*
        bclr   portc,y   $08    Set A0 low to write
*                               to control register
*
        ldab   #$03      b is 0 when write finished
        ldx    #$00      x points to memory location of
*                        start of 24 bit to be written
*
        bclr   portc,y   $02  clear TFS
*
go2     ldaa   0,x
        staa   spdr      write byte to serial port
*
wait2   ldaa   spsr
        bpl    wait2     wait until SPIF flag is clear
*
        decb
        beq    fin2      if b=0 then finished
        inx              points to memory location of next byte
        jmp    go2
*
fin2    bset   portc,y   $0a    set TFS and A0
*
        jmp   $e000      Return to BUFFALO
```

SINGLE SUPPLY ADCs

Single supply ADCs are an important type of Analog to Digital Converter. There are many systems where only one power supply is available, and it is convenient if the converters in the system can be run from that supply, rather than necessitating special, additional, power supplies. Single supply circuits are most commonly found in portable, battery powered devices, but do have many other applications. In the past, analog integrated circuits for complete single supply data acquisition systems were not available and designers were forced either to provide a second supply or work with artificial center rails or other ground substitutes. Today, however, ADI has a complete range of suitable analog integrated circuits, including ADCs, DACs, op amps and instrumentation amplifiers, that operate from a single supply. Single supply ADCs are generally either Sigma-Delta or Successive Approximation types.

SINGLE SUPPLY ADCs

- Often Required in Portable/Battery Powered Applications
- Simplify Power Supply Requirements
- Single Supply ADCs are Usually Either ΣΔ or SAR Type
- Have Reduced Input Signal Range
- What About 3V Operation?

Figure 6.33

Whenever single supply circuitry is used, the input signal range is reduced, and frequently halved. If a negative supply is unavailable signals within the circuit cannot drop below ground potential (inputs, under some circumstances, can do so). The dynamic range is thereby reduced and careful circuit design is necessary to ensure that accuracy is not lost.

Battery technology often dictates the supply possibilities in portable systems. The designer must choose the battery type and the number of cells, but his choices are limited. Despite this there are sufficient possibilities that single supply ICs may have to work over a wide range of supply voltages. In the past single supply systems have generally operated in the +5V to +12V range but today there is a growing demand for +3V operation. Analog ICs operating at +3V are still quite scarce, but ADI does offer ADCs, DACs and amplifiers that are fully characterized for +3V operation.

A comprehensive range of single supply ADCs is available from ADI, with a wide variety of accuracies and speeds. (Figure 6.34) The AD771X family, which we have just discussed, employs sigma-delta techniques in a high accuracy, single supply converter. Other devices, such as the AD1878/79 and AD1848/49 were designed for computer audio applications. In a computer there is almost always a single +5V supply, and frequently +12V or ±12V supplies are available as well. However, all of these supplies are extremely noisy, due to the digital environment. For any analog circuitry in the computer the noisy +12V supply is often reduced to +5V and heavily filtered to provide a noise-free analog supply. So the AD1878/9 and the AD1848/9 operate from a single +5V supply to provide high performance, high resolution audio A-D and D-A conversions. The AD7880 and AD789X converters are 12-bit high speed converters which operate from a single +5V supply, and the AD7883 is a 12-bit converter designed to operate from a +3V supply. There are also numerous 8 and 10-bit converters.

ADI OFFERS A WIDE SELECTION OF SINGLE SUPPLY ADCs

PART #	RESOLUTION (BITS)	SUPPLY RANGE (V)	THROUGHPUT (SAMPLES/SEC)	DIGITAL INTERFACE	COMMENTS
AD7710	21	+5 to +10	10 - 1,000	Serial	ΣΔ
AD7711	21	+5 to +10	10 - 1,000	Serial	ΣΔ
AD7712	21	+5 to +10	10 - 1,000	Serial	ΣΔ
AD7713	21	+5 to +10	10 - 1,000	Serial	ΣΔ
AD1879	18	+5	48,000	Serial	Stereo Audio ΣΔ
AD1878	16	+5	48,000	Serial	Stereo Audio ΣΔ
AD1848	16	+5	5,500 - 48,000	Parallel	Stereo ΣΔ Audio Codec
AD1849	16	+5	5,500 - ~~4,8000~~ 48000	Serial	Stereo ΣΔ Audio Codec
AD776	16	+5	100,000	Serial	ΣΔ
AD7880	12	+5	66,000	Parallel	
AD7890	12	+5	100,000	Serial	8 - Channel
AD7891	12	+5	100,000	Parallel	8 - Channel
AD7892	12	+5	100,000	Parallel	
AD7893	12	+5	100,000	Serial	8-Pin Package
AD7883	12	+3 to +3.6	50,000	Parallel	Lowest Supply Voltage

Figure 6.34

An important consideration in the design of a single supply data acquisition system is the input range of the converter. Ideally, the input range should be as wide as possible to maximize the dynamic range of the system. ADCs operating from dual supplies frequently have a bipolar input signal range:- the input is symmetrical about ground. However, in single supply circuits the input range is often limited to positive signals. To achieve the same resolution the magnitude of an lsb must be halved. For example a dual supply 16-bit converter with ±5 V inputs an LSB is $2^{-16} \times 10V$ or 153μV, while a single supply converter with an input range of 0-5V has an lsb of 76μV and

any errors such as DC offset, non-linearity, or noise must be halved to maintain resolution. High performance single supply amplifiers are necessary to do this:-the OP-213 offers extremely low drift and low noise; in addition to excellent DC accuracy, the OP-295 has a rail-to-rail output swing, which increases the dynamic range; the AD820 combines a rail-to-rail output with an FET input, making it an excellent amplifier for high impedance signal sources; and the OP-90/290/490 family are DC precision amplifiers that operate with only 10μA of supply current per amplifier.

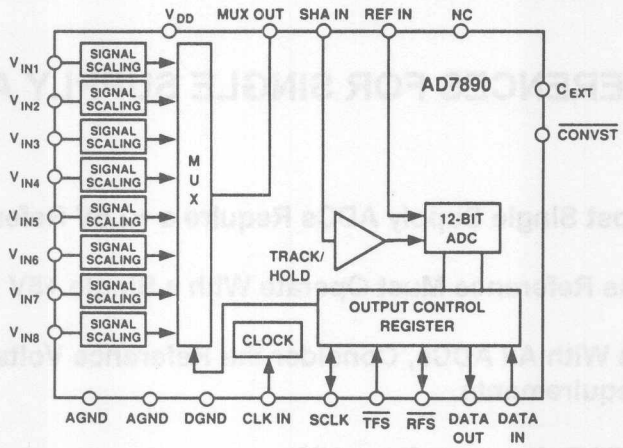
SINGLE SUPPLY ADC INPUT RANGE MAY BE LIMITED BY THE SUPPLY VOLTAGE

- Input Range Often Limited to the Supply Voltage
- For a +5V Supply, Input Range = 5V
- Smaller Input Ranges Reduce the Size of the LSB
- More Attention Needs to be Given to Input Errors
- If an Input Amplifier is Needed, Use a Single-Supply Op Amp Such as the OP-213, OP-295, AD820, or OP-90

Figure 6.35

The AD789x family of ADCs (Figure 6.36) achieves a signal span outside its supply by using thin film resistors in the input stages to attenuate the input signal by a factor of 8. These converters accept inputs of ±10V despite operating from a single +5V supply. The actual input range for the internal sample and hold amplifier and ADC is 0-2.5 V at the "SHA IN" pin and the internal ADC is no different from many other 5V ADCs, but the attenuator (signal scaling) network allows much higher input signals. External resistors can be employed with any ADC to reduce the signal range to the range of the converter; but by including accurate, thin film resistors on chip, the AD789x family ensures 12-bit accuracy and simplifies external circuit design. Not only does the input scaling attenuate the signal, it also attenuates any external errors by the same ratio, maintaining a constant signal to noise ratio.

AD789X-FAMILY UTILIZES INPUT SCALING FOR WIDE INPUT RANGE



- Thin Film Resistors on Input Allow ±10V Inputs
- Internal Signal to ADC is 0 to +2.5V
- Input Scaling Also Attenuates Such Input Errors as Noise and Offset

Figure 6.36

The most common reference for single supply ADCs is +2.5V, but +3V is also used. To be compatible with the ADC the reference must also operate from a single +5V supply (most 2.5V references meet this requirement, including the AD780 which can supply +2.5V or +3V). The reference chosen must meet the current and transient specifications of the ADC reference input. Of the single supply ADCs listed in this section of the seminar, the sigma-delta converters have the simplest reference requirements. The main considerations are the noise and accuracy, not the drive capabilities.

REFERENCES FOR SINGLE SUPPLY ADCs

- Most Single Supply ADCs Require a +2.5V Reference
- The Reference Must Operate With a Single +5V Supply
- As With All ADCs, Consider the Reference Voltage Drive Requirements
- 2.5V References from ADI:

  AD580, AD680, AD780, REF-03, REF-43

Figure 6.37

Digital ICs that operate from +3V are increasingly common. This creates a demand for analog circuits which will operate from the same supplies. ADCs which operate from +3V are still scarce, but are becoming more common. The AD7883 is a +3V 50kSPS successive approximation ADC with an integral track and hold amplifier (Figure 6.38 and 6.39). Its input range is V_{REF} or $\pm V_{REF}$ and it will operate with +2.5 or +3V references, but as it draws less than 3mA from its supply it is often operated with a common +3V supply to V_{DD} and reference inputs. It has also a *power saving* mode where it consumes less than 1mW. A suitable op-amp to use with the AD7883 is the OP-295 with its rail-to-rail output swing and guaranteed specifications at 3V.

THE AD7883 12-BIT, 50kSPS ADC GUARANTEES 3V OPERATION

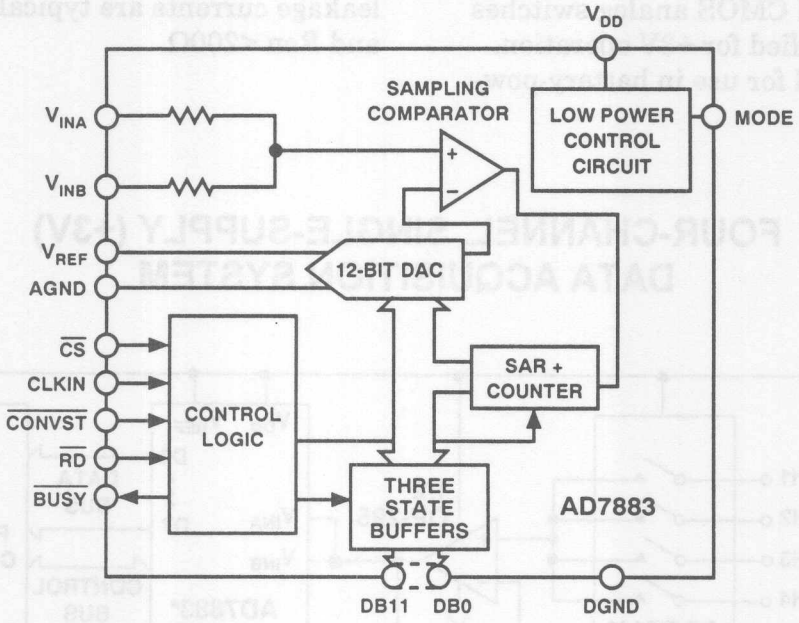


Figure 6.38

AD7883 12-BIT, 50kSPS, 3V ADC KEY FEATURES

- Guaranteed Specifications for 3V to 3.6V Supply Voltage
- 12-Bit SAR Converter
- 50kSPS Throughput Rate
- On-Chip SHA
- DC and AC Specifications
- Low Power: 8mW Typical, 1mW in Power Save Mode
- 24-Pin SOIC Package
- Bipolar or Unipolar Inputs

Figure 6.39

The block diagram of a +3V four channel data acquisition system (DAS) is shown in Figure 6.40. The ADG511 and ADG512 quad CMOS analog switches are fully specified for +3V operation. They are ideal for use in battery-powered instruments as their power requirement is only 3μW and their signal range includes their supply rails. Their leakage currents are typically 50pA, and Ron <200Ω.

FOUR-CHANNEL, SINGLE-SUPPLY (+3V) DATA ACQUISITION SYSTEM

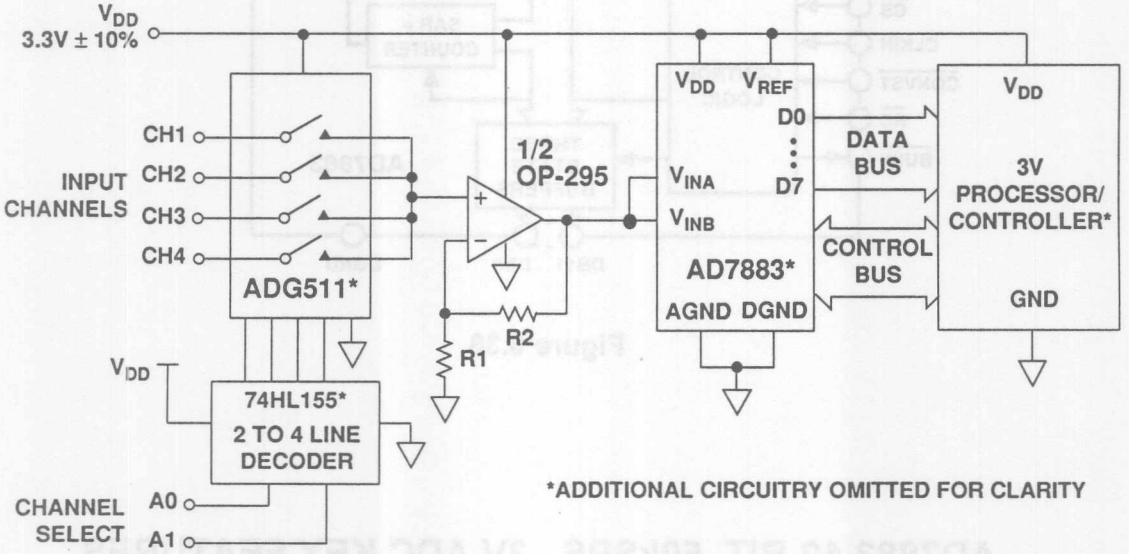


Figure 6.40

The input multiplexer comprises an ADG511 quad analog switch and a 74HL155 two-to-four line decoder. The digital inputs A0 and A1 select the input channel. The signal on the input channel is amplified by an OP-295, used in the non-inverting mode with a gain of [1 + R2/R1], and the amplifier output drives the AD7883, which performs the 12-bit A-D conversion. Figure 6.40 shows the same +3V used for both the supply and the reference, but a 2.5V reference could equally well be used if it is available. (A 2.5V reference could be provided from a 3V supply by using two AD589 two-terminal 1.235V references in series with 250Ω or by using one AD589 in series with 1kΩ and a buffer amplifier with a gain of 2 made from half of an OP-295 and two 10kΩ resistors.)

The gain resistors, R1 and R2, should be chosen to amplify the input signal sufficiently to use the entire dynamic range of the ADC - but without clipping.

The overall bandwidth of the system is limited by the op amp:- the multiplexer and the ADC have much higher bandwidths. Many low-power amplifiers have limited bandwidths and slew rates

and the OP-295 is typical. When powered with +3V its slew rate is only 0.03V/µs, its full-power bandwidth is about 3.8kHz, and its small-signal gain-bandwidth product is only 75kHz. As many transducers have very limited bandwidths the 3.8kHz full-power bandwidth is rarely an important limitation.

For wider bandwidth applications, the single-supply AD820 op-amp may be suitable. It has an FET input stage and a slew rate of 3V/µs, a full power bandwidth of about 380kHz and a gain bandwidth-product of 1.5MHz.

Figure 6.41 shows the results of an evaluation of the circuit. An FFT shows that with an input of 1.11kHz and an amplitude of 2.2V pk-pk, and a sampling rate of 61.44kSPS, the signal/(noise plus distortion) ratio was 67dB over the 30.7kHz Nyquist bandwidth and the THD was -72dBc.

SINGLE-SUPPLY DATA ACQUISITION SYSTEM FFT OUTPUT FOR 1.11kHZ INPUT SAMPLED AT 61.44kSPS YIELDS SNR OF 67dB

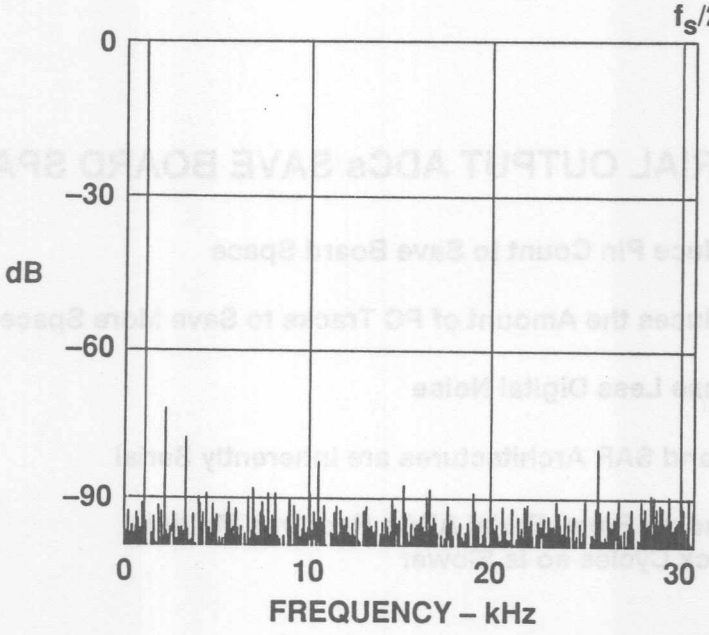


Figure 6.41

SERIAL OUTPUT ADCs

ADCs with a serial, rather than a parallel, interface are valuable when board space is limited, because their packages have fewer pins, and are therefore smaller, and because fewer PC tracks and fewer components are required to interface with them. Both sigma-delta and successive approximation ADCs produce serial data during the conversion process, and may be said to be inherently serial. The AD771X family of 24-bit sigma-delta ADCs provides a clear example of the benefits of serial interfaces:- despite their high resolution and complex functionality they are supplied in small 24 pin packages.

Of course intrinsically serial conversions are not always convenient, since the output data rate may be set by the conversion process and not by system requirements. It is often necessary to have complex logic in an inherently serial ADC with a serial output in order to alter the output data rate, to prevent update during readout, or to perform other necessary housekeeping functions.

Despite their advantages of size and convenience, there is no doubt that serial interfaces are slower than parallel ones, and in the fastest ADCs (which are usually flash or subranging types, which have a more parallel type of architecture) only a parallel interface will be fast enough. The system designer must make the final choice between simplicity and small size, and speed.

SERIAL OUTPUT ADCs SAVE BOARD SPACE

- Reduce Pin Count to Save Board Space
- Reduces the Amount of PC Tracks to Save More Space
- Cause Less Digital Noise
- ΣΔ and SAR Architectures are Inherently Serial
- Reading From Serial ADCs Requires Multiple Clock Cycles so is Slower

Figure 6.42

Figure 6.43 shows the wide selection of serial ADCs available from ADI. They range from 12-bits of effective resolution to 21 or more. They are all smaller than the corresponding parallel parts (if they exist). The ADC-170 and the AD7893 are conspicuously smaller, being 12-bit ADCs in 8 pin packages.

ADI OFFERS NUMEROUS SERIAL ADCs

PART #	RESOLUTION (BITS)	THROUGHPUT (SAMPLES/SEC)	NUMBER OF PINS	SUPPLY VOLTAGE (V)	COMMENTS
AD7710	21	10 - 1,000	24	+5	ΣΔ
AD7711	21	10 - 1,000	24	+5	ΣΔ
AD7712	21	10 - 1,000	24	+5	ΣΔ
AD7713	21	10 - 1,000	24	+5	ΣΔ
AD7703	20	4,000	20	±5	ΣΔ
AD7701	16	4,000	20	±5	ΣΔ
AD1879	18	48,000	28	+5	Stereo ΣΔ Audio
AD1878	16	48,000	28	+5	Stereo ΣΔ Audio
AD1849	16	5,500 - 48,000	44	+5	Stereo ΣΔ Audio Codec
AD1876	16	100,000	16	±12	Sampling ADC
AD677	16	100,000	16	±12	Switched Capacitor
AD776	16	100,000	20	+5	ΣΔ
AD7872	14	83,000	16	±5	Complete SAR
AD7890	12	100,000	24	+5	8 - Channel
AD7893	12	100,000	8	+5	Small Package
ADC-170	12	175,000	8	+5, -12	Small Package

Figure 6.43

COMPLETE DATA ACQUISITION SYSTEMS ON A CHIP

VLSI mixed-signal processing allows the integration of large and complex data acquisition circuits on a single chip. Most signal conditioning circuits including multiplexers, filters, PGAs and SHAs, may now be manufactured on the same chip as the ADC. This high level of integration permits data acquisition systems to be specified and tested as a single complex function.

ADVANTAGES OF AN INTEGRATED SOLUTION TO DATA ACQUISITION

- Built-In Signal Conditioning and ADC
- Multiple Input Channels with Multiplexer
- All System Errors are Characterized
- System Calibration is Easily Performed Internally or Externally
- Reduced Component Count

Figure 6.44

INTEGRATED DATA ACQUISITION SYSTEMS ARE USUALLY PROGRAMMABLE

- Gain Adjustment
- Filter Characteristic Adjustment
- Input Channel Selection

Figure 6.45

Such functionality relieves the designer of most of the burden of testing and calculating error budgets. The DC and AC characteristics of a complete data acquisition system are specified as a complete function, which removes the necessity of calculating performance from a collection of individual worst case device specifications. A complete monolithic system should achieve a higher performance at much lower cost than would be possible with a system built up from discrete functions. Furthermore, system calibration is easier and in fact many monolithic DASs are self calibrating.

With these high levels of integration, it is both easy and inexpensive to make many of the parameters of the device programmable. Parameters which can be programmed include gain, filter cutoff frequency, and even ADC resolution and conversion time, as well as the obvious digital/MUX functions of input channel selection, output data format, and unipolar/bipolar range.

The AD7890 is an example of a highly integrated monolithic data acquisition system. It has 8 multiplexed input channels with scaling, a SHA amplifier, an internal voltage reference, and a fast 12-bit ADC. Its block diagram is shown in Figure 6.46 and key specifications are summarized in Figure 6.47. Both AC and DC parameters are fully specified, simplifying the preparation of an error budget, and three types are available with three different standard input ranges:-

AD7890-10	±10 V
AD7890-5	0 to 5V
AD7890-2	0 to +2.5V

THE AD7890 12-BIT, 8-CHANNEL SAMPLING ADC WITH SERIAL OUTPUTS

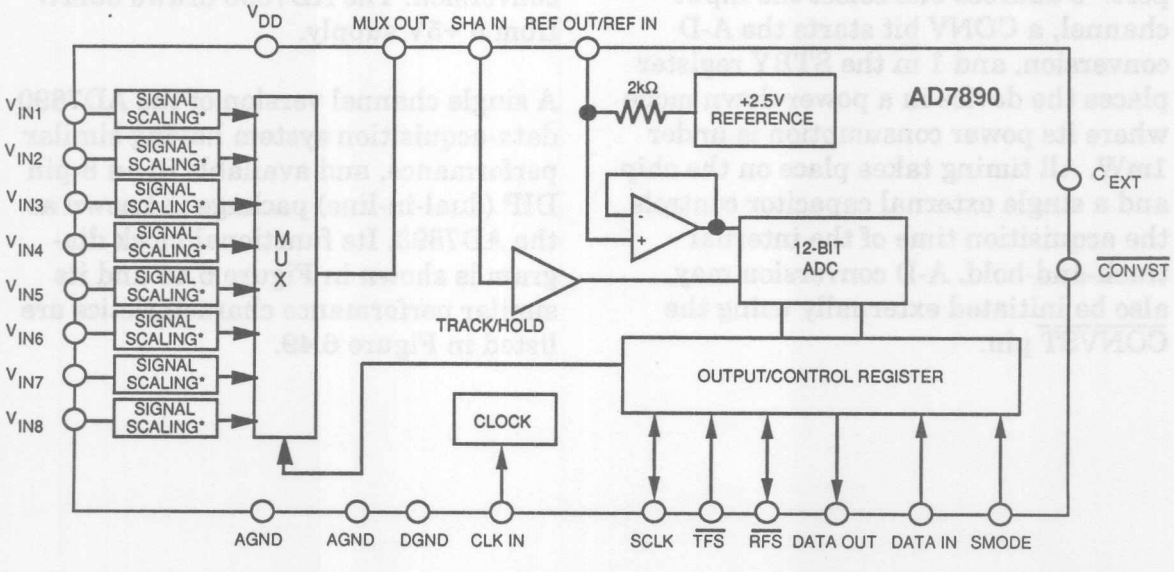


Figure 6.46

AD7890 SPECIFICATIONS

- ADC Conversion Time: 5µs
- SHA Acquisition Time: 2µs
- 100kSPS Throughput Rate
- AC and DC Specifications
- Single +5V Operation
- Low Power Drain:
  - Operational: 30mW
  - Power Down Mode: 1mW
- Standard Input Ranges:
  - AD7890 - 10: ± 10V
  - AD7890 - 5: 0 to +5V
  - AD7890 - 2: 0 to +2.5V

Figure 6.47

The input channel selection is via a serial input port. A total of 5 bits of data control the AD7890 via a serial port:- 3 address bits select the input channel, a CONV bit starts the A-D conversion, and 1 in the STBY register places the device in a power-down mode where its power consumption is under 1mW. All timing takes place on the chip and a single external capacitor controls the acquisition time of the internal track-and-hold. A-D conversion may also be initiated externally using the $\overline{\text{CONVST}}$ pin.

The AD7890 acquires a signal in under 2µs, and completes its 12-bit conversion in under 5µs. This allows a 100kSPS conversion. The AD7890 draws 30mW from a +5V supply.

A single channel version of the AD7890 data-acquisition system having similar performance, and available in an 8-pin DIP (dual-in-line) package is known as the AD7893. Its functional block diagram is shown in Figure 6.48 and its similar performance characteristics are listed in Figure 6.49.

AD7893, A SINGLE-CHANNEL VERSION OF THE AD7890 IN AN 8-PIN PACKAGE

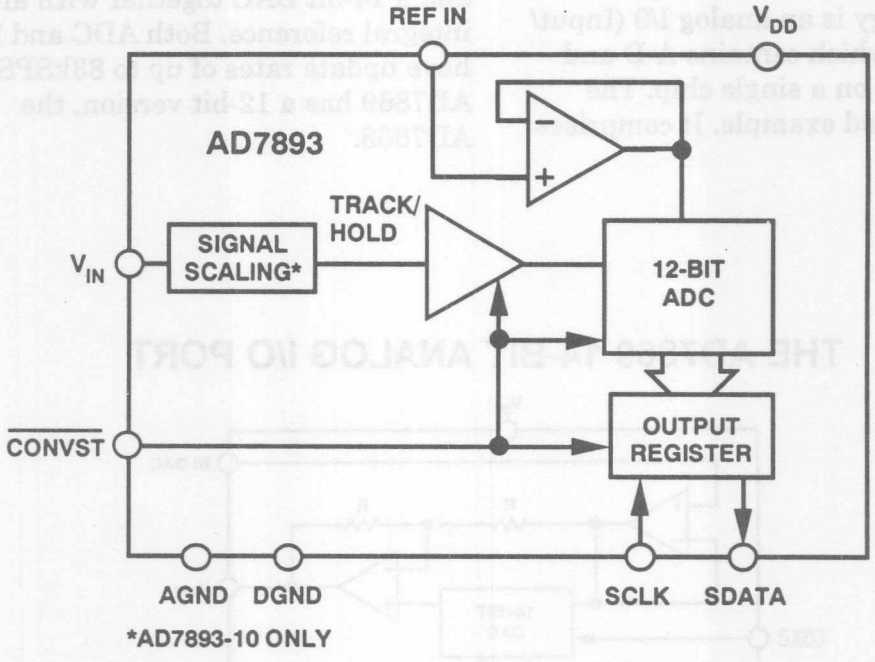


Figure 6.48

KEY FEATURES OF THE AD7893

- Conversion Time: 6µs
- SHA Acquisition Time: 1.5µs
- 117kSPS Throughput Rate
- Complete AC and DC Specifications
- Single +5V Supply Operation
- Low Power Drain: 30mW
- Small 8-Pin Minidip or SOIC Package

Figure 6.49

Another useful circuit which may be made with monolithic mixed signal VLSI technology is an analog I/0 (Input/ Output) port, which contains A-D and D-A converters on a single chip. The AD7869 is a good example. It comprises a 14-bit sampling ADC (i.e. with a SHA) and a 14-bit DAC together with an integral reference. Both ADC and DAC have update rates of up to 83kSPS. The AD7869 has a 12-bit version, the AD7868.

THE AD7869 14-BIT ANALOG I/O PORT

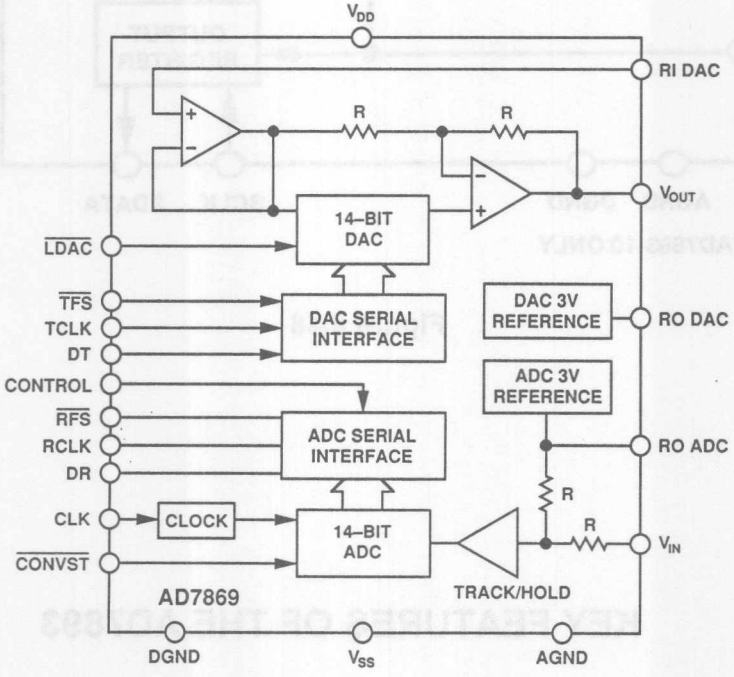


Figure 6.50

AD7869 I/O PORT KEY FEATURES

- 14-Bit ADC with SHA, 83kSPS Throughput Rate
- 14-Bit DAC with On-Chip Output Amplifier, 3.5µs Settling Time
- ± 5V Supply Operation
- Fully Specified for SNR and THD

Figure 6.51

The highest resolution monolithic DAS circuits available today have resolutions of well over 20-bits. The AD7716 is a quad sigma-delta ADC with 22-bit resolution and an over-sampling rate of 570kSPS. A functional diagram of the AD7716 is shown in Figure 6.52 and some of its key features in Figure 6.53. The device does not have a "start conversion" control input but samples continuously. The cutoff frequency of the digital filters (which may be changed during operation, but only at the cost of a loss of valid data for a short time while the filters clear) is programmed by data written to the DAS. The output register is updated at a rate which depends on the cutoff frequency chosen. The AD7716 contains an auto-zeroing system to minimize input offset drift.

AD7716 22-BIT QUAD SIGMA-DELTA ADC

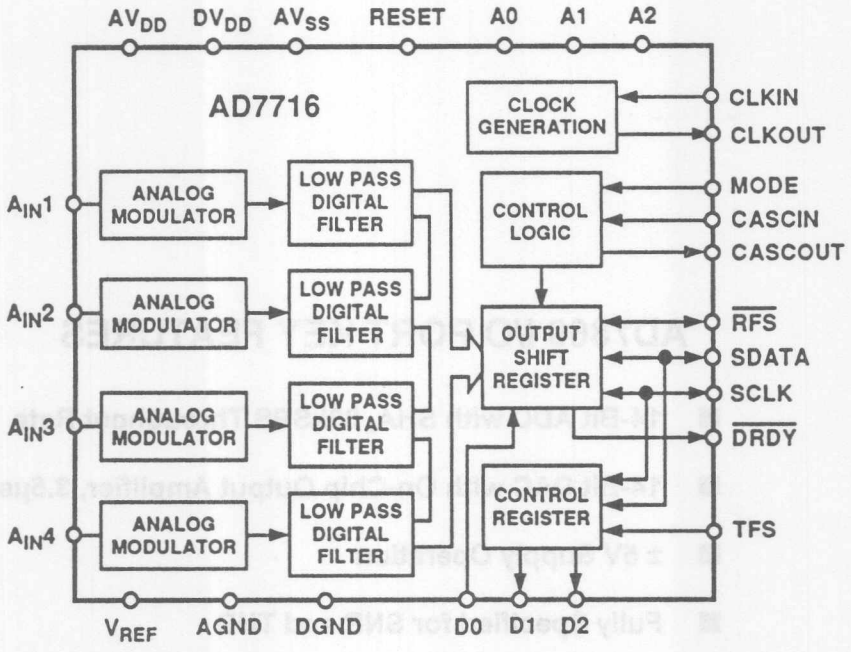


Figure 6.52

AD7716 QUAD SIGMA-DELTA ADC KEY FEATURES

- 22-Bit Resolution, 4 Input Channels
- ΣΔ Architecture, 570kSPS Oversampling Rate
- On-Chip Lowpass Filter, Programmable from 36.5Hz to 584Hz
- Serial Input / Output Interface
- ±5V Power Supply Operation
- Low Power: 50mW

Figure 6.53

REFERENCES

1. **Mixed Signal Design Seminar**, Analog Devices, 1991, Section 6.

2. **1992 Amplifier Applications Guide**, Analog Devices, 1992, Section 11

3. "A Non-Mathematical Introduction to SIGMA-DELTA ADCs" by James Bryant. Analog Devices Ltd., Walton-on-Thames, England. 1993

SECTION 7

THE AD1B60: AN INTELLIGENT, DIGITIZING SIGNAL CONDITIONER

- THE ANALOG STATE-OF-THE-ART
- WHAT ARE DIGITAL SIGNAL CONDITIONERS?
- AN EMBEDDED MICROCONTROLLER GIVES THE AD1B60 "INTELLIGENCE"
- BUILT-IN CIRCUITS MAKES ACQUIRING THE SENSOR SIGNALS SIMPLE
- COMMUNICATION PORTS
- DIGITAL COMMAND AND CONTROL
- CONVERSION MODES
- CALIBRATING THE AD1B60
- THE AD1B60 IN THERMOCOUPLE APPLICATIONS
- CONFIGURING THE AD1B60 FOR VOLTAGE INPUTS
- CONFIGURING THE AD1B60 FOR RTD APPLICATIONS
- USING THE AD1B60 IN AN INDUSTRIAL ENVIRONMENT
- SUPPLYING POWER TO THE AD1B60
- LAYOUT TECHNIQUES FOR MAXIMUM PERFORMANCE
- THE AD1B60 EVALUATION BOARD
- USING DIGITAL ALGORITHMS IN SIGNAL CONDITIONING CIRCUITRY

SECTION 7

THE AD1B60: AN INTELLIGENT, DIGITIZING SIGNAL CONDITIONER

Adolfo Garcia

The design of signal conditioning circuitry for industrial markets places extraordinary demands on the analog circuit designer. Customers frequently require levels of precision and stability that are difficult to obtain at the best of times to be obtained from low level signals contaminated with high levels of noise and interference. Over the years, engineers familiar with the requirements of these applications have developed a number of methodologies and techniques to meet their customers' demands.

Illustrated in Figure 7.1 is a block diagram of a typical measurement/control loop used in industrial processes. These processes vary and can range from setting and controlling temperature (the most frequently conditioned parameter) to robotics. These systems, programmed for autonomous operation, operate in a closed-loop under the control of computers. At the heart of the system is the sensor which is used to measure a variety of physical quantities: temperature, pressure, flow, humidity, or strain. While some of these sensors are active and generate a voltage or current (for example, thermocouples), most sensors are passive and require external excitation in the form of applied voltages (strain gauges) or currents (RTDs). Nearly all sensors share one feature — their outputs are low-level and vulnerable to interference when operating in high interference environments. In these applications, the sensor output must be conditioned by analog means (filtering, offset, and amplification) before A/D conversion. Galvanic isolation may also be required because of high potential differences between the sensor and the signal conditioning circuitry. Since systems are often controlled by a master computer, provisions for local data processing and communications may also be required. All these issues make the system designer's task challenging.

BLOCK DIAGRAM OF A MEASUREMENT/CONTROL PROCESS LOOP

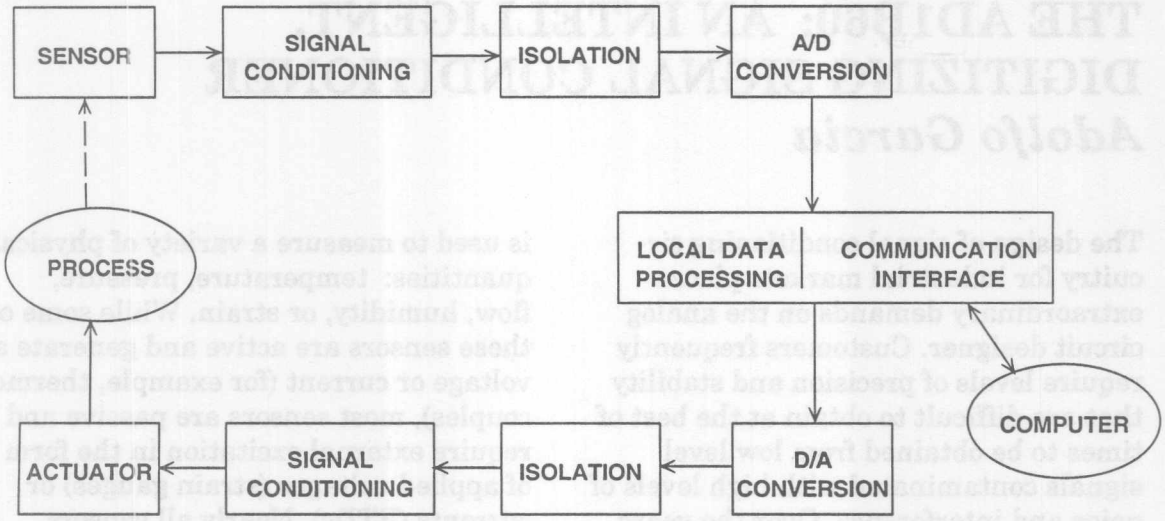


Figure 7.1

THE ANALOG STATE-OF-THE-ART

Classic analog signal conditioners are designed to accept signals from sensors such as thermocouples and RTDs, perform all necessary signal conditioning functions, and deliver an accurate representation of the physical input to the sensor as an output. The necessary signal conditioning functions may include: input fault protection, filtering, amplification, zero (or offset) suppression, linearization, cold-junction and/or lead wire compensation, scaling, et cetera.

To keep circuit costs down, the design of these measurement/control loops often use a single A/D converter to convert the outputs of a number of sensors. As shown in Figure 7.2, analog conditioners may include the following circuits: an analog multiplexer, a programmable gain amplifier (PGA), a precision voltage reference, an analog-to-digital converter, and a microcontroller to control the analog circuits and to facilitate the digital interface between itself and the host computer. The analog signal conditioner requires, at a minimum, half a dozen integrated circuits, passive components, custom software, and PC board. These are expensive.

PREVIOUS STATE OF THE ART

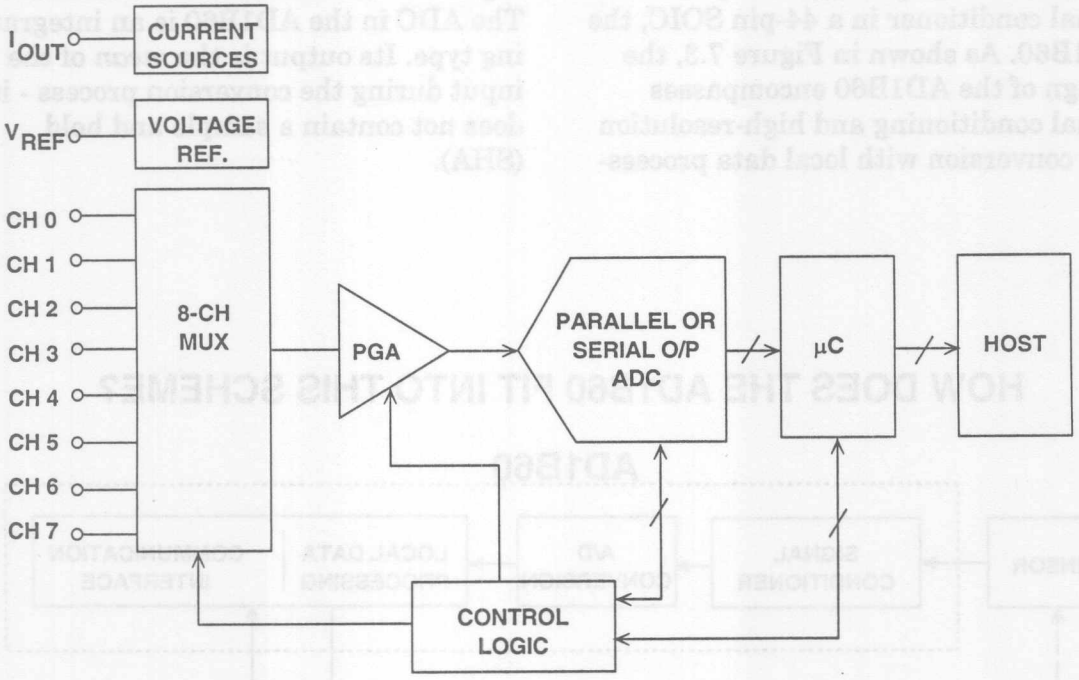


Figure 7.2

The nature of the signal conditioning art is being changed by the introduction of small, inexpensive single-chip microcontrollers. These devices have become inexpensive enough to incorporate into signal conditioning circuitry as an integral element of the component design. Incorporating these microcontrollers adds the advantages of lower cost, greater flexibility, and higher accuracy when compared to traditional analog signal conditioning approaches. A new class of signal conditioning products, called digital signal conditioners, have appeared in the marketplace as a result of this change of philosophy.

WHAT ARE DIGITAL SIGNAL CONDITIONERS?

Digital signal conditioners are identified by their use of a digital output format where an RS-232, RS-485, or even a frequency output replaces the usual analog 4–20mA or 0–10 volt output signal. The use of a digital output format may be an advantage over more traditional analog output formats. Because digital interfaces can be more readily isolated and multiplexed and are far more resistant to the noise and interference often found in industrial environments. However, the real advantage of digital signal conditioning lies not in the form of the interface, but in the ability of digital circuitry to augment or supplant many of the functions heretofore accomplished exclusively by analog means.

To reflect this change in signal conditioning philosophy, Analog Devices has

designed a first-generation digital signal conditioner in a 44-pin SOIC, the AD1B60. As shown in Figure 7.3, the design of the AD1B60 encompasses signal conditioning and high-resolution A/D conversion with local data processing and a communications interface. The ADC in the AD1B60 is an integrating type. Its output is the *mean* of the input during the conversion process - it does not contain a sample and hold (SHA).

HOW DOES THE AD1B60 FIT INTO THIS SCHEME?

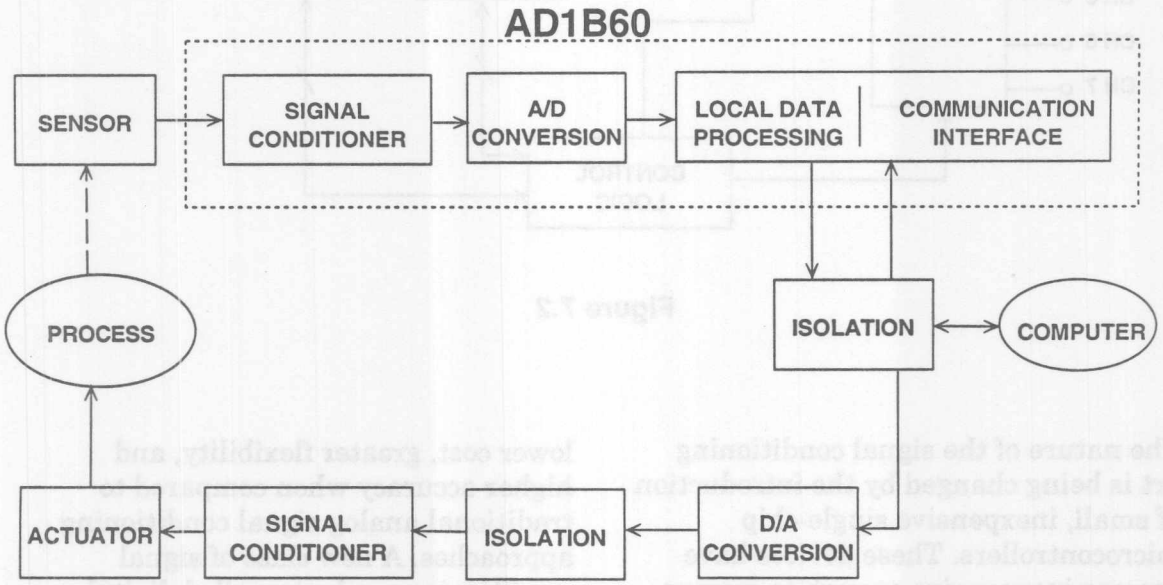
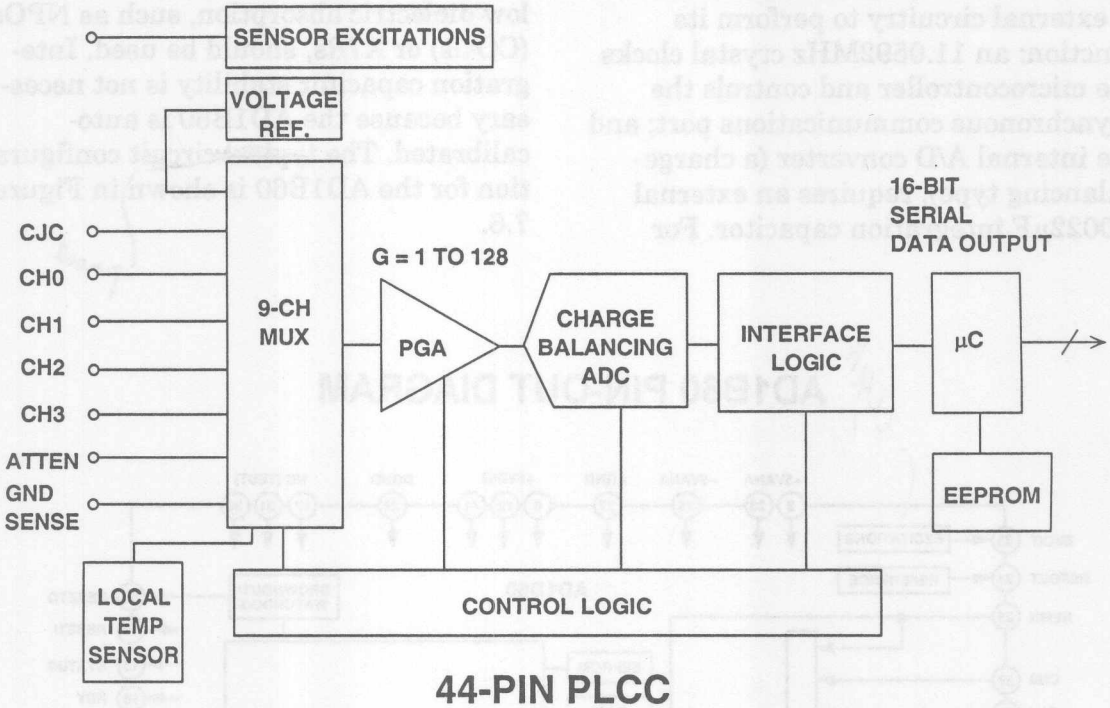


Figure 7.3

As shown in Figure 7.4, the AD1B60 is a single part which contains a mask-programmed microcontroller (with EEPROM memory) and a front-end analog/digital ASIC. The primary application of the AD1B60 is a user-configurable digitizing signal conditioner for RTDs, thermocouples, and low- and high-level voltage signals. The custom BiCMOS ASIC includes a 9-channel multiplexer, a low-drift voltage reference, a programmable-gain amplifier, a charge-balancing converter, and all the required logic circuitry to permit communication and control via a serial digital interface. Key features of the AD1B60 are summarized in Figure 7.5.

AD1B60 SIMPLIFIED BLOCK DIAGRAM



44-PIN PLCC

Figure 7.4

FEATURES OF THE AD1B60 "INTELLIGENT DIGITIZING SIGNAL CONDITIONER"

- User-configurable inputs (Thermocouples, RTDs, etc.)
- Four modes of CJC for TCs - including open TC detection
- Lead compensation for 3 and 4-wire RTDs plus excitation
- Accuracy: 1°C for TCs and RTDs
- Embedded micro-controller and EEPROM
- Digitally controlled configuration and calibration
- Output in Engineering Units (°C, V, etc.)
- Asynchronous and synchronous communication ports

Figure 7.5

The AD1B60 requires a small amount of external circuitry to perform its function: an 11.0592MHz crystal clocks the microcontroller and controls the asynchronous communications port; and the internal A/D converter (a charge-balancing type), requires an external 0.0022μF integration capacitor. For highest performance capacitors with low dielectric absorption, such as NPOs (COGs) or X7Rs, should be used. Integration capacitor stability is not necessary because the AD1B60 is auto-calibrated. The typical circuit configuration for the AD1B60 is shown in Figure 7.6.

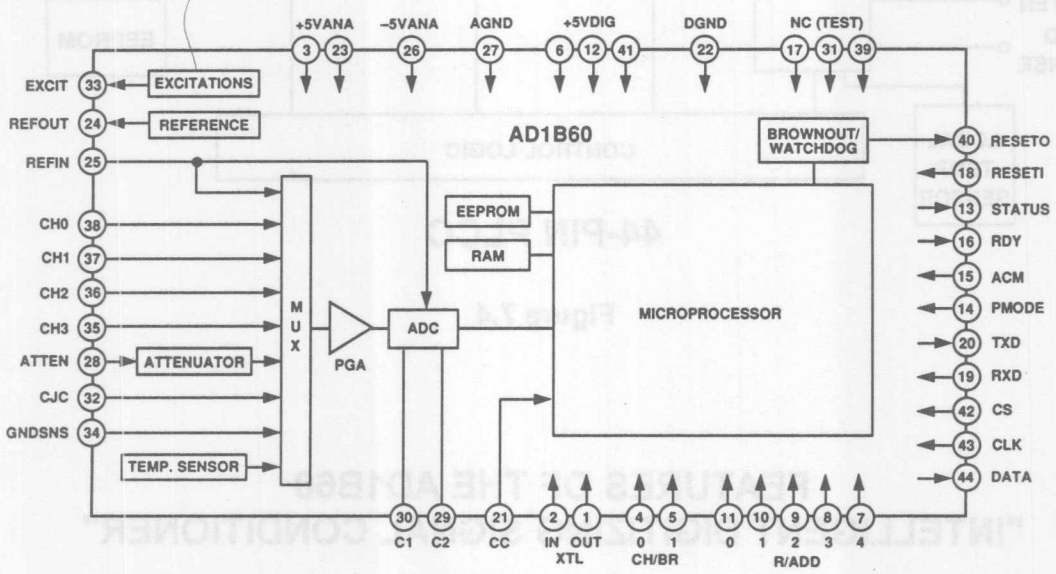


Figure 7.6

AN EMBEDDED MICROCONTROLLER GIVES THE AD1B60 "INTELLIGENCE"

Circuit drift over time and temperature, circuit effects over the full-scale span, variation of resistors over time and temperature, and many other issues must be addressed if an industrial sensor circuit design is to be a success. In addition, such a design must provide cold-junction compensation in thermocouple applications and lead-wire compensation in remotely-located RTD applications.

The microcontroller internal to the AD1B60 contains custom software for controlling the individual analog functions and scaling and linearizing the sensor data — the chart in Figure 7.7 outlines the built-in routines programmed into the AD1B60. Details of the techniques and algorithms used for the built-in functions can be found in the Appendix.

THE AD1B60'S INTERNAL MICROCONTROLLER BUILT-IN ROUTINES

- Auto Zero
- Lead-Wire Compensation for RTDs
- Cold Junction Compensation for Thermocouples
- Data Scaling
- Data Linearization for RTDs, Thermocouples, etc.
- Input Span Compensation
- Addressing and CRC

Figure 7.7

The output from this part is a completely conditioned digital representation of the input, and includes linearization and scaling. The output data is represented directly in engineering units (for example, °C, mV, etc.) using single-precision IEEE floating point format. A 16-bit integer format result is also available. By combining analog signal conditioning *and* local intelligence in the form of a microcontroller, the AD1B60 can used in remotely-located applications. These applications include industrial temperature measurement systems, process control systems, multi-channel thermocouple systems, and analytical instruments where signal conditioning at the sensor is desired.

One function of particular importance is automatic span compensation. The AD1B60 measures both the input signal and the voltage reference with respect to ground at the appropriate gain. The result is a function of the *ratio* of the two measurements. This eliminates ADC drift terms. The voltage reference may be the internal reference or an external precision reference.

The AD1B60 also compensates for temperature drift of the RTD current excitation source. During the AD1B60 manufacturing process the temperature drift of the current source is measured along with an on-board temperature sensor. The correction coefficient is stored in EEPROM, and all RTD readings are adjusted to eliminate thermal drift.

Since the intended use for the AD1B60 is to provide a complete sensor-to-digital interface, the analog front end of the device was designed to work with a

number of passive and active sensors. The AD1B60 accepts a wide range of input signals from devices which include seven types of thermocouples and two types of RTDs. Low-level voltage sources up to ±2 V can be applied to input channels CH0 through CH3 while high-level signals up to ±10 V can be applied to the device through the AD1B60's internal 5:1 attenuator. The AD1B60's high input impedance of > 10MΩ allows almost any sensor source impedance level.

As previously mentioned, the AD1B60 provides the algorithms required for scaling and linearizing sensors of the types shown in Figure 7.8. Summarized in Figure 7.9 are the ranges, accuracies, and resolutions for each of the built-in sensor routines.

One clear advantage of the AD1B60 over traditional analog signal conditioners is its flexibility in handling different sensor types. For sensors not included in the built-in routines, a linearization algorithm can be created for *any* sensor. The sensor's characteristic polynomial coefficients are coded into a custom linearization algorithm which can be downloaded on command into the AD1B60's EEPROM. Thus, for sensors such as Type N thermocouples and subranges, the AD1B60 is the ideal signal conditioning device. The AD1B60 can accommodate two user-defined linearization algorithms.

THE AD1B60 ACCEPTS A MULTITUDE OF SENSORS AND INPUT RANGES

- **Thermocouples: Type J, K, T, E, R, S, B**
- **Platinum 100Ω RTD: $\alpha = 3.85 \times 10^{-3}$, $\alpha = 3.92 \times 10^{-3}$**
- **Low-Level V_{in}: ±10mV, ±20mV, ±50mV, ±100mV, ±200mV, ±500mV, ±1V, ±2V**
- **High-Level V_{in}: ±5V, ±10V**
- **Downloadable Ranges: Two User-Defined Ranges**

Figure 7.8

THE AD1B60'S BUILT-IN ALGORITHMS LINEARIZE THERMOCOUPLE AND RTD OUTPUTS

Thermocouple Type	Temperature Range	Accuracy/Resolution (Typ)
J	0°C ≤ T ≤ 760°C	± 0.25°C / ± 0.15°C
K	0°C ≤ T ≤ 1000°C	± 0.55°C / ± 0.2°C
T	–100°C ≤ T ≤ 400°C	± 0.25°C / ± 0.15°C
E	0°C ≤ T ≤ 1000°C	± 0.2°C / ± 0.1°C
R	500°C ≤ T ≤ 1750°C	± 1.00°C / ± 0.55°C
S	500°C ≤ T ≤ 1750°C	± 1.15°C / ± 0.6°C
B	500°C ≤ T ≤ 1800°C	± 1.15°C / ± 0.7°C

100Ω RTD Type	Temperature Range	Accuracy / Resolution
α = 3.85 mΩ/Ω/°C	–200°C ≤ T ≤ 800°C	± 0.2°C/± 0.15°C
α = 3.92 mΩ/Ω/°C	–200°C ≤ T ≤ 800°C	± 0.2°C/± 0.15°C

Figure 7.9

BUILT-IN CIRCUITS MAKES ACQUIRING THE SENSOR SIGNALS SIMPLE

Besides its multiplexer, PGA, and A/D converter, an analog signal conditioner must also provide ancillary circuits. Outlined in Figure 7.11, the ancillary analog circuits include digitally-controlled current sources for RTD and thermistor excitation, open thermocouple detection, and an internal 5:1 attenuator for high-level input signals. The AD1B60 digital functionality is enhanced by the addition of a brownout detector and a watchdog timer.

To add current sources to an analog signal conditioner requires precision resistors and operational amplifiers. The AD1B60 simplifies the process by incorporating digitally controlled current sources. Accuracy is guaranteed for all sensors due to the sequential calibration process.

High-level signals are applied to the AD1B60 through a 5:1 attenuator whose nominal resistance is 50kΩ. To avoid source loading errors, the source impedance in this case should be low: it may be advisable to buffer the source with a precision operational amplifier to ensure low source impedance.

ADDITIONAL FUNCTIONALITY USING THE AD1B60'S BUILT-IN CIRCUITS

- RTD Current Source Excitation
- CJC Thermistor Exitation
- Open Thermocouple Detection
- 5:1 Attenuator for High Level Signals
- Brownout Detector / Watchdog Timer

Figure 7.10

BUILT-IN CIRCUITS REDUCE OVERALL COMPONENTS COUNT

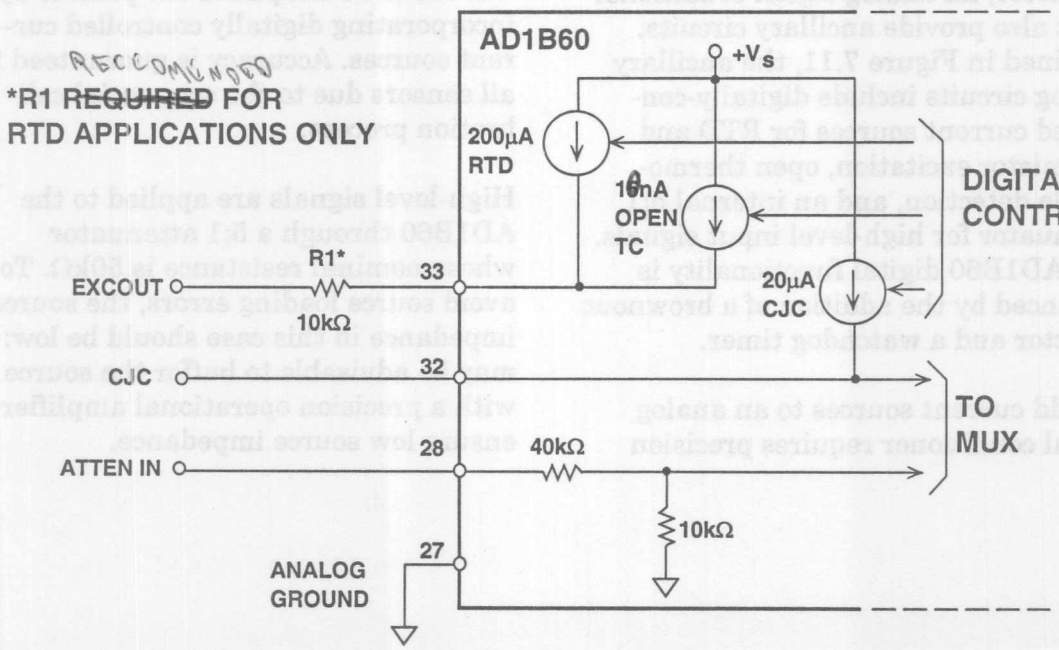


Figure 7.11

To enhance the digital functionality of the AD1B60, a brownout detector and a watchdog timer were added to the internal control circuitry. These functions force the device to a power-up default configuration and are very useful in the event of a power failure or other abnormal operating condition. The brownout detector is designed to reset the AD1B60's microcontroller if the supply voltages to the device drop below the following trip points:

+5 V Digital ≈ +3.5V
+5 V Analog ≈ +3.9V
–5 V Analog ≈ –3.9V

The operation of the brownout detector is illustrated in Figure 7.12. The trip points are intentionally set well below the customary –5% range to avoid nuisance trips due to noise. Digital output data is valid after resets when the Data Valid flag in the AD1B60's ADSTAT byte is set to logic "1". However, the amount of time before data becomes valid depends on the input sensor range and integration time.

The watchdog timer automatically resets the AD1B60 in the event of a microcontroller failure. During normal operation, the microcontroller is programmed to strobe the watchdog timer every 20ms. In the event that the microprocessor stops for any reason (for example, a power glitch), the watchdog timer initiates a reset sequence.

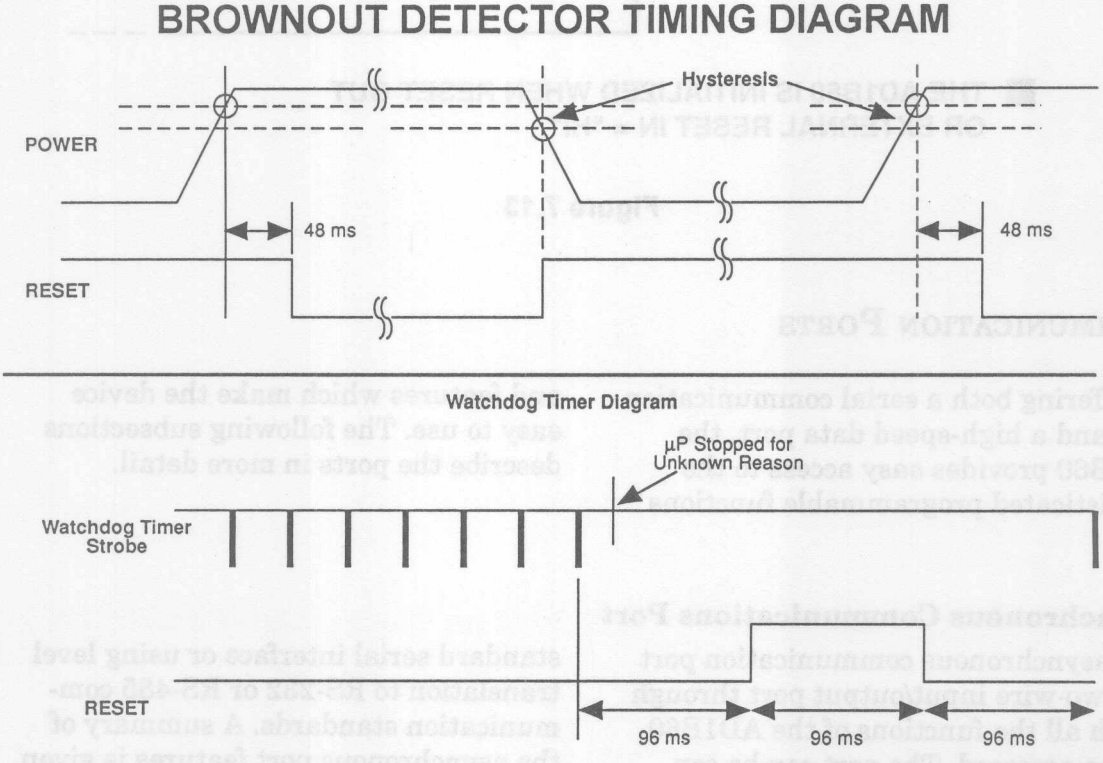


Figure 7.12

Normally, the AD1B60's RESET OUT (pin 40) is connected to its RESET IN (pin 18); however, there are some applications where an asynchronous reset may be required. In those applications, an OR-gate can be inserted between these two pins to provide asynchronous, system-level reset.

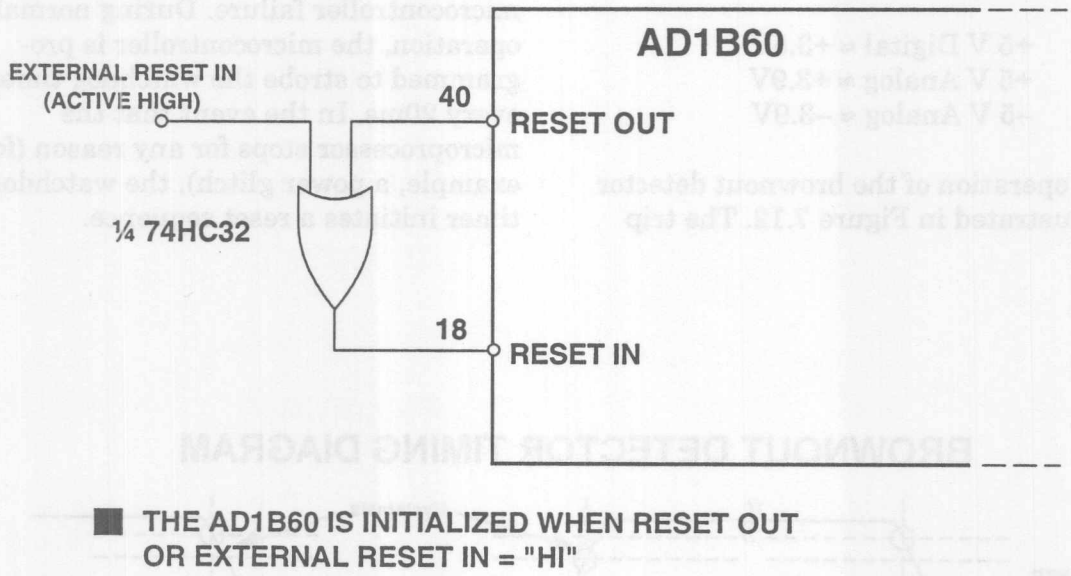


Figure 7.13

COMMUNICATION PORTS

By offering both a serial communication port and a high-speed data port, the AD1B60 provides easy access to the sophisticated programmable functions and features which make the device easy to use. The following subsections describe the ports in more detail.

Asynchronous Communications Port

The asynchronous communication port is a two-wire input/output port through which all the functions of the AD1B60 can be accessed. The port can be connected to a host using its industry-standard serial interface or using level translation to RS-232 or RS-485 communication standards. A summary of the asynchronous port features is given in Figure 7.14.

FEATURES OF THE AD1B60 ASYNCHRONOUS COMMUNICATION PORT

- Fast, 2-wire, Input/Output -- Up to 19.2 kBaud
- Direct connection to embedded microcontrollers
- Communication to PCs via RS-232 and RS-422/485
- User Selectable Baud Rates
- Supports up to 32 AD1B60s with CRC
- 16-bit Integer and Floating Point Data Format
- Simple Binary Protocol
- Command Set

Figure 7.14

The asynchronous port operates at 2400, 4800, 9600, or 19200 baud using the following convention: eight bits, no parity, one stop bit. The baud rate is user-selectable, and break detection is supported as an absolute means of resetting the communications routines.

The asynchronous port supports addressability and cyclic redundancy error checking (CRC) which allows up to 32 AD1B60s to share a "party line" and to exist in remote locations from the host system. Addressing and error checking can be enabled by setting the state of the Advanced Communication Mode (ACM) on pin 15 to logic "1." If the state of the ACM pin is logic "0," address and CRC values are ignored.

The host computer system initiates all communication with the AD1B60: messages are sent over the asynchronous port using a simple binary protocol. Reading converted data, changing configuration parameters in memory, or calibrating the device can be done using the AD1B60 Command Set which is based on this binary protocol. Commands can be sent to the device through the RxD pin (pin 19). Data and device status can be retrieved from the TxD pin (pin 20).

High-Speed Data Port

The high-speed data port is a fast, 3-wire, output-only synchronous port. It is double-buffered and completely independent of the asynchronous port. This allows access to both ports simultaneously, if required. Features of the high-speed data port are summarized in Figure 7.15.

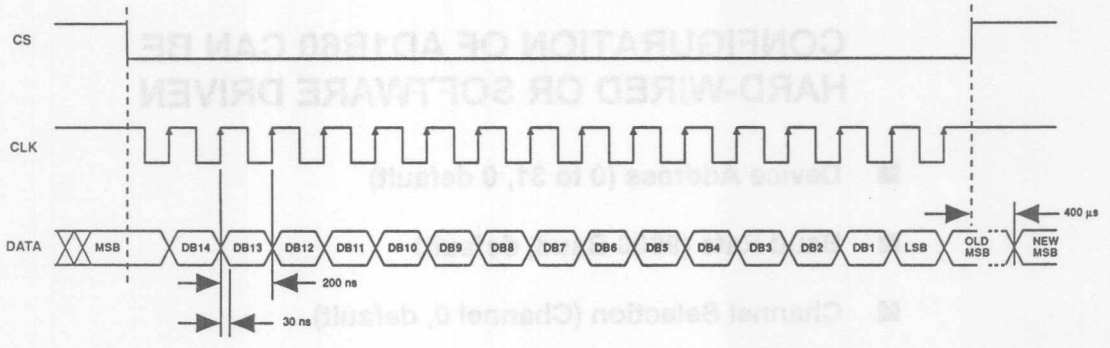
FEATURES OF THE AD1B60 HIGH-SPEED DATA PORT

- Fast, 3-wire Output-Only Port
- Double buffered
- Independent of Asynchronous Port
- 16-bit data at 200ns/bit
- Output Buffer Updated at *Start* of *Every* Conversion

Figure 7.15

The data port consists of two CMOS inputs (CS and CLK, pins 42 and 43, respectively) and one CMOS output (DATA, pin 44). The data port becomes active when CS is set to logic "0". Data can retrieved from this port in 16-bit integer format as fast as 200ns/bit. The timing diagram of the data port is illustrated in Figure 7.16. The AD1B60 updates the buffer at the start of every conversion, thus data can be read at any time. To read data from the high-speed port, both CS and CLK must be initially set to logic "1." At this time, the state of the DATA output is the MSB of the output word. This is useful for checking the sign bit without reading the entire sixteen-bit word. To read each bit, CS is set to logic "0," and then CLK is cycled. A new bit shifts out on each rising edge of CLK. After the 16-bit data has been read, CLK is set to logic "1" and then the port is disabled by setting CS to logic "1." Whenever CS changes state, CLK must be at logic "1." to avoid metastability problems

AD1B60 HIGH-SPEED DATA PORT TIMING DIAGRAM



- CS and CLK are CMOS Inputs
- DATA is a CMOS Output
- State of DATA when CS = HI is the MSB
- Data is Recirculated @ 16th Clock Edge
- Update Has Up to 400 µs Latency

Figure 7.16

For bipolar analog inputs, converted data from the port is represented in 16-bit, twos complement format. For thermocouple and RTD applications, the converted data is represented in 16-bit, offset binary format.

DIGITAL COMMAND AND CONTROL

The AD1B60 can be configured through the asynchronous port using its command set or in hardware by setting the appropriate inputs. The AD1B60's power-up default settings are shown in Figure 7.17. For more detailed information regarding the operation of the AD1B60 under hardware configuration, consult the AD1B60 Data Sheet.

The most flexible way to configure and control the AD1B60 is to use the command set, in this way input ranges can be calibrated and converted data/device status can be read. Figure 7.18 lists the AD1B60 Command Set. Where applicable, the numerical format for communicating with the AD1B60 is based on the 4-byte IEEE floating point standard. For more detailed information regarding the command set and examples of the floating point format, consult the AD1B60 User's Guide.

CONFIGURATION OF AD1B60 CAN BE HARD-WIRED OR SOFTWARE DRIVEN

- Device Address (0 to 31, 0 default)
- Baud Rate (9600 Baud, default)
- Channel Selection (Channel 0, default)
- Input Range (Type J Thermocouple, default)
- Integration Time (100ms, default)
- CJC Mode (Thermistor, default)
- RTD Configuration Mode (3-wire)

Figure 7.17

THE AD1B60s COMMAND SET ALLOWS CONFIGURATION AND CONTROL VIA SOFTWARE

Command	Function
WR_EPM_PARS	Alters Default Values in EEPROM
WR_RAM_PARS	Alters the Current Value of the Configuration Parameters
RD_RAM_PARS	Reads Back the Current Values of the Configuration Parameters
LOAD_RNG	Loads Input Range into EEPROM (Requires 8 bytes)
GET_RNG	Reads Back Input Range from EEPROM (Requires 8 bytes)
WR_CJC	Downloads External CJC into RAM
RD_CJC	Reads Back Current Value of the CJC from RAM
SEL_CH	Selects an Input Channel
CAL	Initiates Calibration Cycle
RD_INTDATA	Reads Converted Data in 16-bit Integer Format and Conversion Status
RD_FPDATA	Reads Converted Data in Floating Point Format and Conversion Status

- Floating Point Format Used Is 4-Byte IEEE Standard

Figure 7.18

CONVERSION MODES

The AD1B60 allows the designer control over the conversion process. Two modes of operation are available: a continuous conversion mode and a triggered conversion mode. There are three signals involved in the conversion process: the convert command input (CC, pin 21), integration status output (RDY, pin 16), and conversion status output (STATUS, pin 13). For continuous conversions, the CC input is set to logic "1." In this mode, the AD1B60 converts continuously with an updated result available every 2 integration times. Conversions continue until CC is cleared to logic "0." When CC is cleared, the AD1B60 completes the current signal and background conversions at which time it waits (in "idle" mode) for CC to go high before starting another conversion.

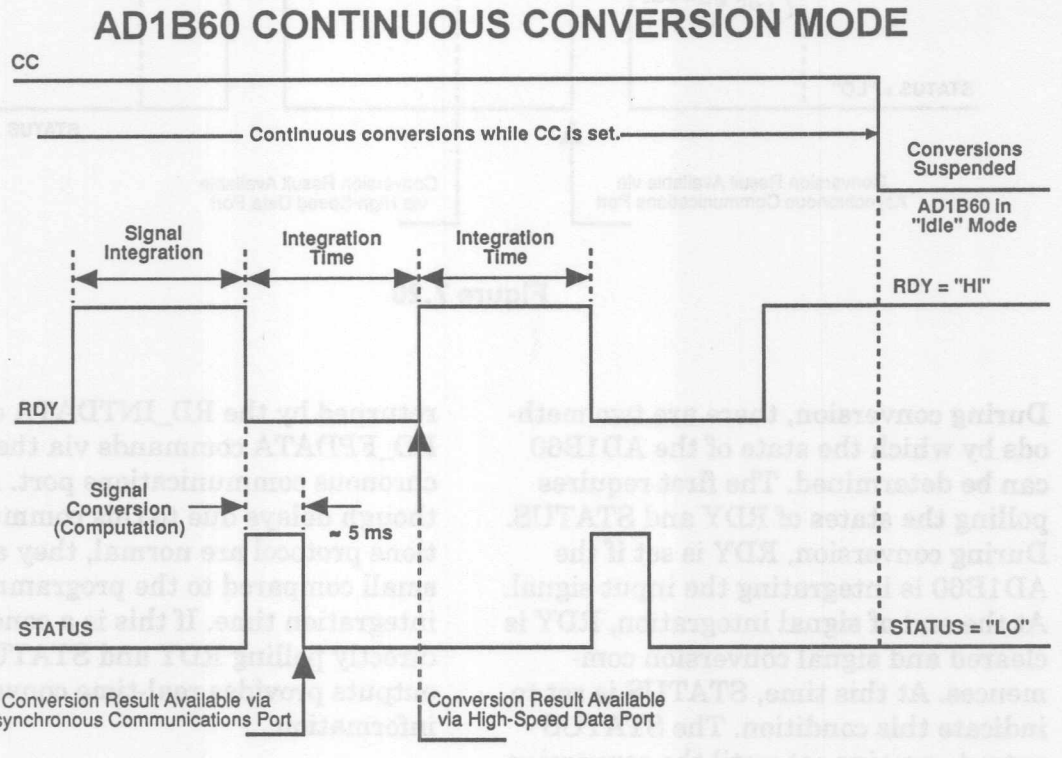


Figure 7.19

In the triggered conversion mode, the AD1B60 is in its "idle" state. In this state, the integration status output, RDY, is at logic "1" and the conversion status output, STATUS, is at logic "0." When CC goes to logic "1," the AD1B60 integrates and converts the input data. The device continuously converts its input signals until CC is cleared. This conversion mode is particularly useful in applications where synchronous data conversion is required. The ADC in the AD1B60 is an integrating type. Its output is the *mean* of the input during the conversion process - it does not contain a sample and hold (SHA).

AD1B60 TRIGGERED CONVERSION MODE

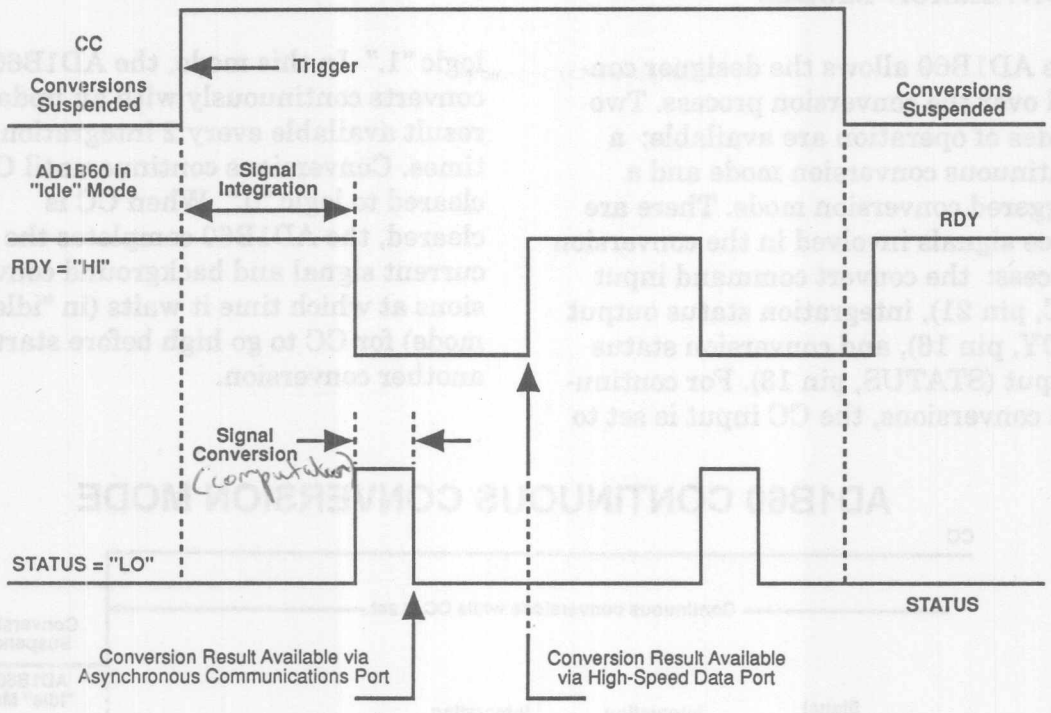


Figure 7.20

During conversion, there are two methods by which the state of the AD1B60 can be determined. The first requires polling the states of RDY and STATUS. During conversion, RDY is set if the AD1B60 is integrating the input signal. At the end of signal integration, RDY is cleared and signal conversion commences. At this time, STATUS is set to indicate this condition. The STATUS output remains set until the conversion process is over. When both RDY and STATUS outputs are at logic "0," the result of the conversion is available at the asynchronous communication port of the AD1B60. When RDY goes high again, the output data is then available at the high-speed data port.

The second method to determine the status of the conversion process is by polling the status of the ADSTAT byte returned by the RD_INTDATA or RD_FPDATA commands via the asynchronous communications port. Although delays due to this communications protocol are normal, they are small compared to the programmed integration time. If this is a concern, directly polling RDY and STATUS outputs provides real-time conversion information.

The rate at which the conversions take place depends upon the input range and the integration times programmed into the AD1B60. Figure 7.21 illustrates the relationship between conversion rate and integration time for various sensor configurations. For integration times of 33ms or longer, the conversion rate is constant regardless of input sensor configuration.

CONVERSION RATE IS USER-SELECTABLE

INTEGRATION TIME	CONVERSIONS/SEC CJC = THERMISTOR	CONVERSIONS/SEC WITHOUT CJC	CONVERSIONS/SEC K TYPE THERMISTOR
2ms	90	100	48
5ms	78	87.5	44
33ms	14.8	14.8	14.8
40ms	12.3	12.3	12.3
50ms	9.9	9.9	9.9
60ms	8.3	8.3	8.3
100ms*	5*	5*	5*
200ms	2.5	2.5	2.5

* Factory default setting

Figure 7.21

CALIBRATING THE AD1B60

Although the AD1B60 is calibrated at the factory prior to shipment, the user may choose to calibrate the device for the desired application. The calibration procedure, outlined in Figure 7.22, is sequence-dependent and requires a precision voltage source and two precision resistors, a 250Ω resistor for RTDs and a 100kΩ resistor for thermocouples. The accuracy of the AD1B60's calibration depends upon the accuracy of the reference excitation or resistance. Although calibration accuracy of the AD1B60 does not depend on integration time, using a 200ms integration time for the calibration procedure is recommended to ensure the best resolution and noise rejection. This is the preferred method even though the application may use a shorter integration time.

CALIBRATION OF AD1B60 IS PERFORMED OVER THE ASYNCHRONOUS PORT

Step	Input Range	Reference Excitation	Circuit Configuration
1	± 2 V	+ 2.00000 V	CH0 to Analog GND
2	± 1 V	+ 1.00000 V	CH0 to Analog GND
3	± 500 mV	+ 0.50000 V	CH0 to Analog GND
4	± 200 mV	+ 0.20000 V	CH0 to Analog GND
5	± 100 mV	+ 0.10000 V	CH0 to Analog GND
6	± 50 mV	+ 50.000 mV	CH0 to Analog GND
7	± 20 mV	+ 20.000 mV	CH0 to Analog GND
8	± 10 mV	+ 10.000 mV	CH0 to Analog GND
9	± 10 V	+ 10.00000 V	Attenuator to Analog GND
10	Type J TC	100.000 kΩ	CJC Input to Analog GND
11	100Ω Pt RTD, α = 0.00385 Ω/Ω/°C	250.000 Ω	4-wire RTD Configuration (CH1 to CH3)

- AD1B60 is Factory Calibrated
- Calibration Sequence is Sequence Dependent
- Not All Calibration Steps Are Required

Figure 7.22

Since the calibration procedure is sequence-dependent, calibration for certain input ranges depends on the prior calibration of one or more voltage ranges. For example, if the AD1B60 is intended to be used in thermocouple applications, calibration step #11 can be skipped; however, steps #1 through #10 cannot be skipped. The following steps illustrate the calibration sequence:

1. Configure the AD1B60 for each calibration step using the WR_RAM_PARS command. For example, to calibrate the AD1B60 for Step #1, set the input range RAM value to ±2V.

2. Apply the specified reference excitation for that particular calibration step. For example, apply a +2.00000V reference to Channel 0.

3. Wait until the Data Valid flag in ADSTAT goes high.

4. Wait 1 second to allow the AD1B60 to acquire a stable reading.

5. Execute the CAL command.

6. Wait until the CAL flag in ADSTAT goes low.

7. Repeat Steps 1 through 6 for the remaining input ranges, as necessary.

THE AD1B60 IN THERMOCOUPLE APPLICATIONS

The commonest temperature sensors in industrial applications are thermocouples. Their rugged construction and low cost explain their popularity. However, the outputs of these sensors are nonlinear and require cold-junction, or ice-point, compensation to produce the correct measurement. The AD1B60 includes cold-junction compensation as one of its internal routines and offers four options for cold-junction compensation (CJC):

1. A 10kΩ, NTC Thermistor (Betatherm 10K3A1)

2. An external 1mV/K temperature sensor (AD592 + 1kΩ resistor)

3. An analog cold-junction compensator (AC1226)

4. A downloaded cold-junction temperature value

Figure 7.23 shows how the thermocouple, and the thermistor used for cold-junction compensation, are connected to the AD1B60 for temperature measurement. The thermocouple is connected between CH0 and GNDSENSE with the thermistor and the thermocouple's cold junction in close thermal proximity. Thus, if the ambient temperature of the cold junction changes, the thermistor registers the change in temperature, allowing the AD1B60 to compensate for it. In this mode of cold-junction compensation, the AD1B60 provides the excitation current for the thermistor from CJC IN (pin 32). For open thermocouple detection, a 15nA current source is available at EXCOUT (pin 33) where it can be connected to the thermocouple's positive (+) lead. In the event of an open thermocouple, the output of the PGA saturates, and the AD1B60's output data stream will indicate an upscale fault condition. To avoid errors, the thermocouple's negative (–) terminal and the GNDSENSE pin should form a "star" connection with the analog ground. This is because GNDSENSE is actually an input.

In the second example, illustrated in Figure 7.24, the AD592, a monolithic temperature sensor whose output current exhibits a temperature coefficient of 1μA/K, works with a 1kΩ precision resistor to provide the cold-junction compensation. For optimum performance, the TCR of the precision resistor should be no greater than ± 10 ppm/°C. Like the thermistor, the AD592 must be in close thermal proximity to the thermocouple's cold junction to avoid measurement error. Again, a "star" connection to the analog ground should be formed with the thermocouple's negative terminal, the return end of the 1kΩ precision resistor, and the AD1B60's GNDSENSE pin.

USING A THERMISTOR FOR COLD-JUNCTION COMPENSATION

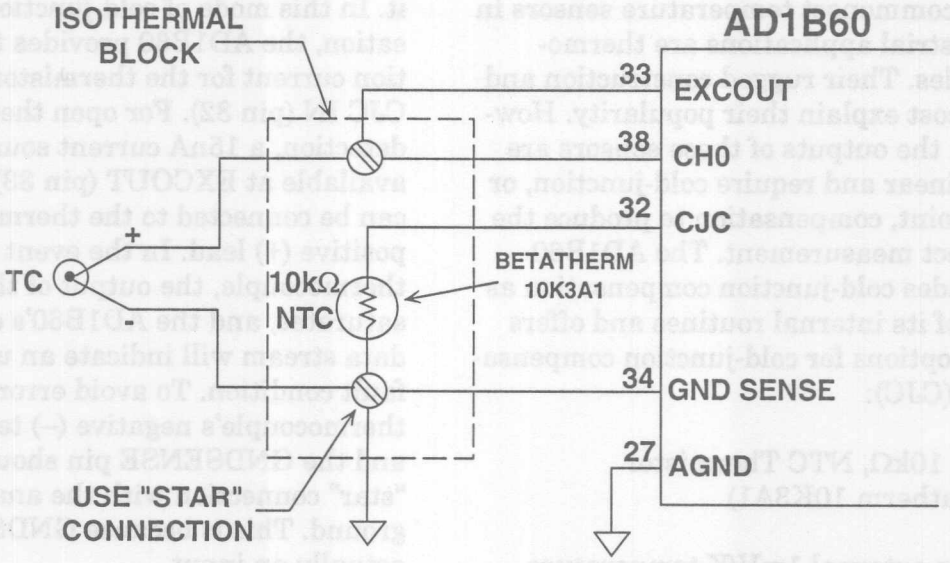
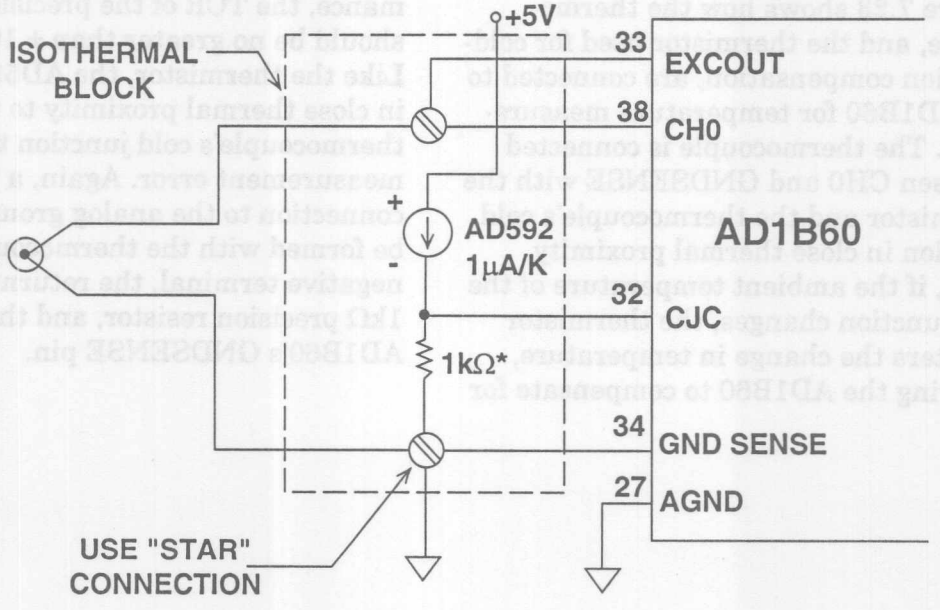


Figure 7.23

USING THE AD592 TEMPERATURE SENSOR FOR COLD-JUNCTION COMPENSATION



*PRECISION RESISTOR: 0.01% OR BETTER.
TCR ≤ 10ppm/°C

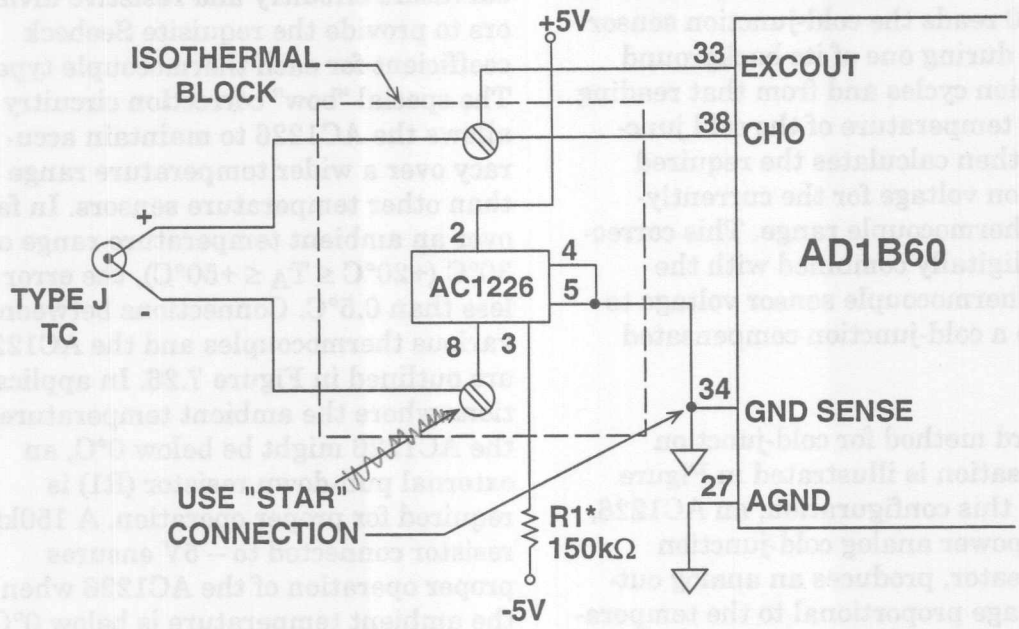
Figure 7.24

When either the thermistor CJC mode or the mV/K mode is selected, the AD1B60 reads the cold-junction sensor voltage during one of its background conversion cycles and from that reading obtains temperature of the cold junction. It then calculates the required correction voltage for the currently-active thermocouple range. This correction is digitally combined with the actual thermocouple sensor voltage to produce a cold-junction compensated value.

The third method for cold-junction compensation is illustrated in Figure 7.25. In this configuration, an AC1226, a micropower analog cold-junction compensator, produces an analog output voltage proportional to the temperature of the cold junction. This voltage is then subtracted from the thermocouple's terminating junction voltage at the input of the AD1B60. Since the subtraction occurs at the input to the AD1B60, no algorithmic correction is required, and the internal CJ compensation is disabled in this mode. To ensure accurate compensation, the negative (–) terminal of the thermocouple is directly connected to the corresponding pin on the AC1226 at the cold junction. The AC1226 compensator is specifically designed for use with type E, J, K, R, S, and T thermocouples, and is packaged in an 8-pin DIP. The compensator contains special curvature circuitry and resistive dividers to provide the requisite Seebeck coefficient for each thermocouple type. The special "bow" correction circuitry allows the AC1226 to maintain accuracy over a wider temperature range than other temperature sensors. In fact, over an ambient temperature range of 30°C (+20°C ≤ T_A ≤ +50°C), the error is less than 0.5°C. Connections between various thermocouples and the AC1226 are outlined in Figure 7.26. In applications where the ambient temperature of the AC1226 might be below 0°C, an external pull-down resistor (R1) is required for proper operation. A 150kΩ resistor connected to – 5V ensures proper operation of the AC1226 when the ambient temperature is below 0°C.

The fourth method of providing cold-junction compensation is to download a value into the AD1B60's RAM through the asynchronous port using the WR_CJC command from the command set. This mode is useful in applications where a single cold-junction compensator is used for multiplexing a number of sensors or where a higher accuracy device is used for CJC sensing. In this mode, acceptable values for user-defined CJC range from –25°C ≤ T_{CJC} ≤+85°C, and the CJ variable is initialized to 0°C upon power-up/reset.

USING THE AC1226 COLD-JUNCTION COMPENSATOR WITH THERMOCOUPLES



*R1 NOT REQUIRED IF AC1226 TEMPERATURE ≥ 0°C

Figure 7.25

CIRCUIT CONNECTION BETWEEN THE AC1226 AND VARIOUS THERMOCOUPLES

Thermocouple Type	Connect TC (–) to AC1226 Pin #
E	1
J	8
K	7
R	6
S	6
T	7

Figure 7.26

When the AD1B60 is used in thermocouple applications, the issues in Figure 7.27 must always be remembered. In applications where more than one thermocouple may be used the AD1B60 may be configured for different thermocouple input ranges. For example, CH0 could be configured for a Type T thermocouple while CH1 is configured for a Type K thermocouple. Up to 12 integration times are needed for valid data in these applications. Data may be verified by checking the status of the DATA VALID bit in the ADSTAT byte. If the application requires multiplexing between like thermocouples (therefore equal input ranges), then up to 3 integration times are needed for valid data. The channel bits in the ADSTAT byte may be used to check for valid data.

ISSUES TO CONSIDER WHEN MEASURING THERMOCOUPLES

- Up to 4 thermocouples can be multiplexed
- One CJC can be used for 4 thermocouples
- Open thermocouple detection using internal 15nA current source
- CJC readings updated every 5 signal conversions (10 absolute conversions)
- Open thermocouple detection on 1 thermocouple only

Figure 7.27

In applications where a number of thermocouples are used, open thermocouple detection can be applied to only one channel. To provide open circuit detection for all thermocouples, the circuit illustrated in Figure 7.28 can be used.

THREE RESISTORS MAKE A SIMPLE OPEN TC DETECTOR

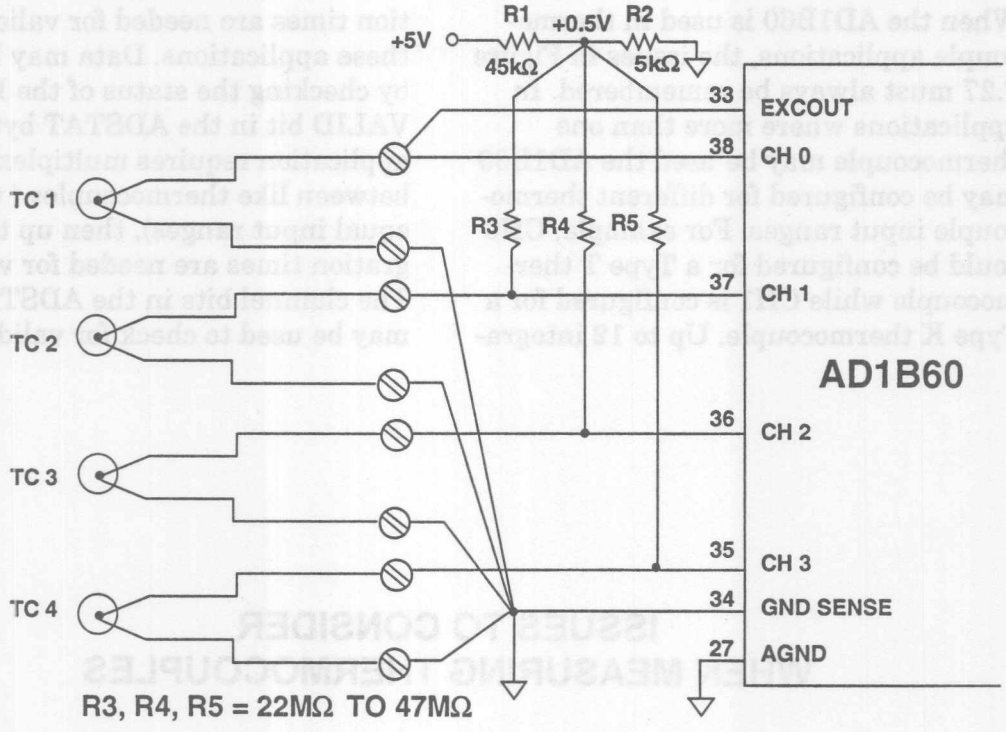


Figure 7.28

In this circuit, R1 and R2 form a voltage divider whose output is set to +0.5V. For each thermocouple, a resistor between 22MΩ to 47MΩ is used to inject a very small current into the positive terminal. In the event of an open thermocouple, that input channel goes towards +5V — a potential sufficiently high to saturate the output of the PGA. This sets the overflow flag in the AD1B60's ADSTAT byte.

CONFIGURING THE AD1B60 FOR VOLTAGE INPUTS

The AD1B60 can be configured with low- or high-level input signals. Figure 7.29 shows how to configure the device for low-level voltage inputs. Low-level signals are signals in the range of $\pm 10mV \leq V_{IN} \leq \pm 2V$. To minimize errors, a "star" connection is used to connect all the signal returns together at one point to the analog ground. When the AD1B60 is configured in this mode, the CJC IN channel remains active, therefore it can operate as a "phantom" 5th temperature channel when a thermistor or a mV/K source is connected to it.

CONNECTING LOW LEVEL (< ±2V) INPUT SIGNALS TO THE AD1B60

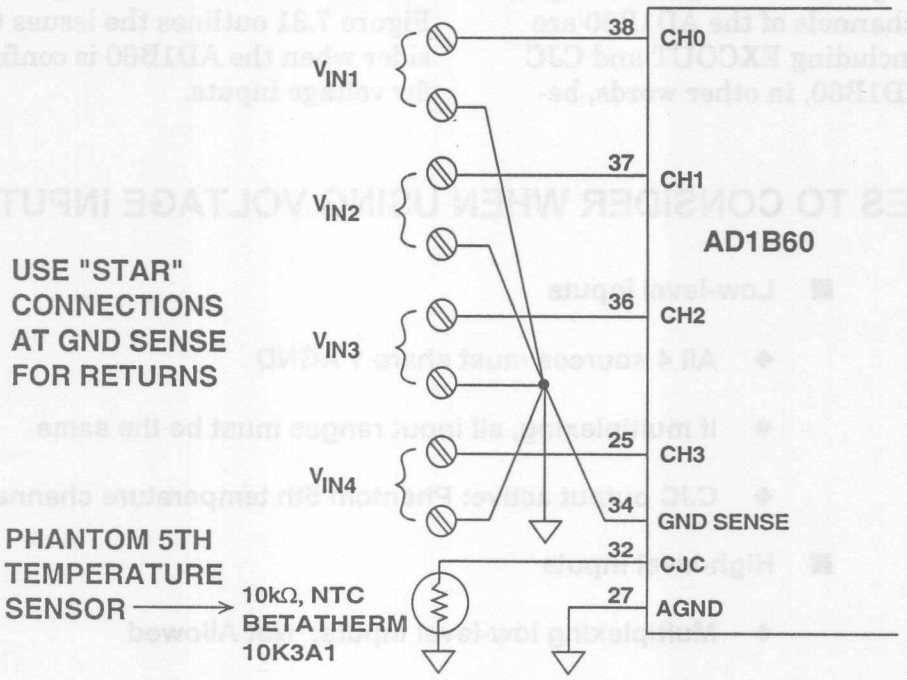


Figure 7.29

Configuring the AD1B60 for operation with a high-level input is also straightforward and is illustrated in Figure 7.30. A high-level input is any signal in the range of $\pm 5V \leq V_{IN} \leq \pm 10V$. The signal is applied to the internal 5:1 attenuator at the Attenuator Input pin (pin 28) of the AD1B60; hence, only one high-level voltage input source is allowed to the AD1B60.

CONNECTING HIGH LEVEL (< ±10V) INPUT SIGNALS TO THE AD1B60

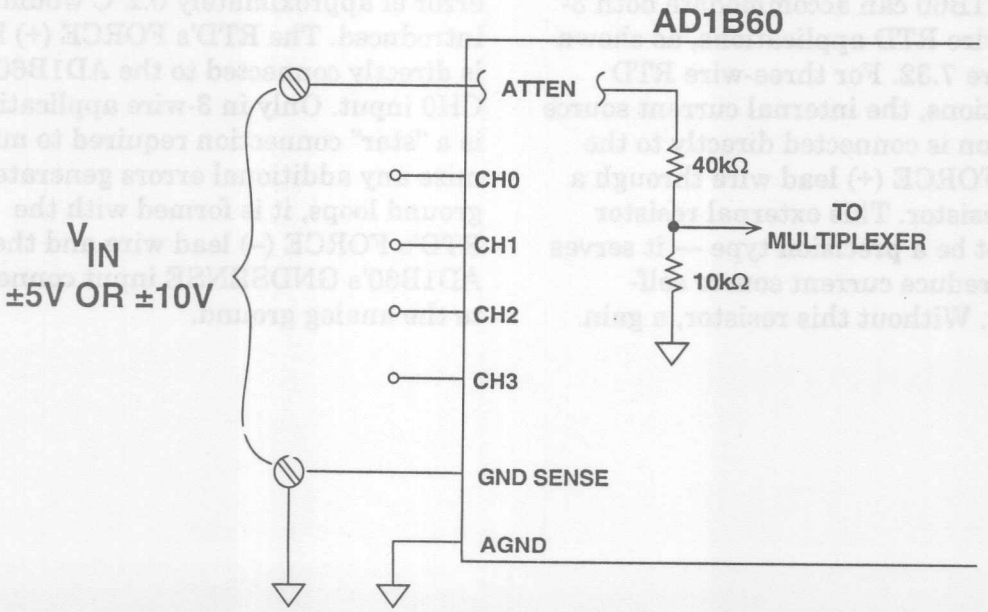


Figure 7.30

When configured for a high level input, all other channels of the AD1B60 are disabled including EXCOUT and CJC IN. The AD1B60, in other words, becomes dedicated to this single input. Figure 7.31 outlines the issues to consider when the AD1B60 is configured for voltage inputs.

ISSUES TO CONSIDER WHEN USING VOLTAGE INPUTS

- Low-level inputs
  - All 4 sources must share 1 AGND
  - If multiplexing, all input ranges must be the same
  - CJC output active: Phantom 5th temperature channel
- High-level inputs
  - Multiplexing low-level inputs: Not Allowed
  - Multiplexing RTDs: Not Allowed
  - 50kΩ Input Impedance
  - Dedicated

Figure 7.31

CONFIGURING THE AD1B60 FOR RTD APPLICATIONS

The AD1B60 can accommodate both 3- and 4-wire RTD applications, as shown in Figure 7.32. For three-wire RTD applications, the internal current source excitation is connected directly to the RTD's FORCE (+) lead wire through a 10kΩ resistor. This external resistor need not be a precision type — it serves only to reduce current source self-heating. Without this resistor, a gain error of approximately 0.2°C would be introduced. The RTD's FORCE (+) lead is directly connected to the AD1B60's CH0 input. Only in 3-wire applications is a "star" connection required to minimize any additional errors generated by ground loops, it is formed with the RTD's FORCE (–) lead wire and the AD1B60's GNDSENSE input connected to the analog ground.

CONFIGURING THE AD1B60 FOR RTDs IS EASY

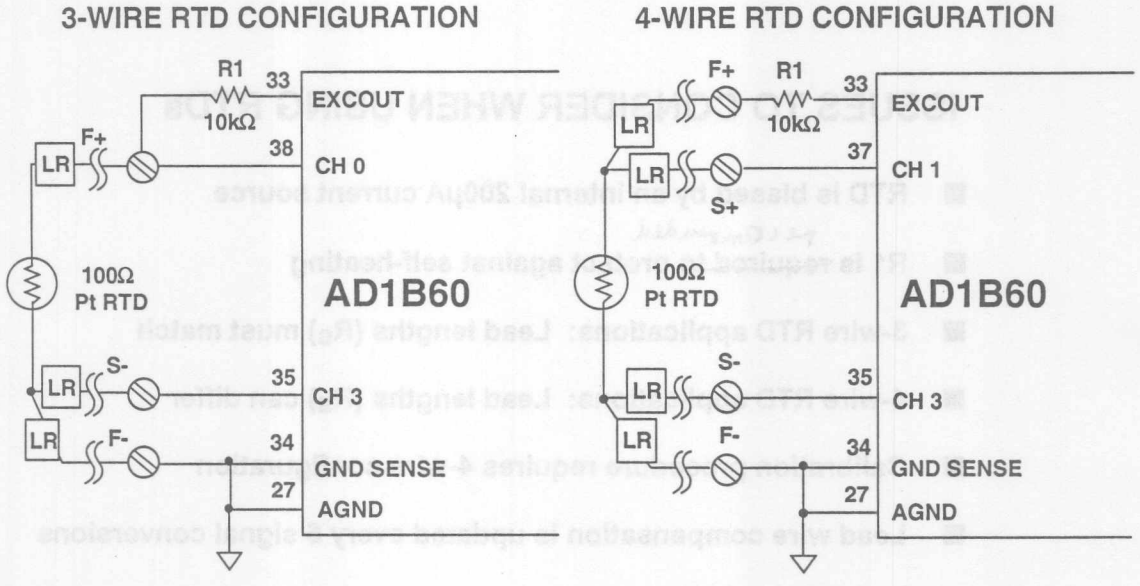


Figure 7.32

In four-wire applications the RTD FORCE(+) lead goes to the 10kΩ resistor, its SENSE(+) to CH1, and its SENSE(-) to CH3. There is no star connection, and FORCE(-) goes to GNDSENSE and AGND.

When the AD1B60 is configured for RTD applications, issues to consider during the design are outlined in Figure 7.33. Although the AD1B60 provides compensation for lead resistances up to 40Ω, total, the lead-wire resistances in 3-wire RTD applications must match; in fact, every 38.5mΩ mismatch in lead resistance will introduce an error of 0.1°C in the reading. No such lead-wire resistance matching is required in four-wire applications. To calibrate the AD1B60 for RTD applications, the 4-wire configuration is used with a precision 250Ω resistor substituted for the RTD.

ISSUES TO CONSIDER WHEN USING RTDs

- RTD is biased by an internal 200μA current source
- R1 is ~~required~~ recommended to protect against self-heating
- 3-wire RTD applications: Lead lengths (R_S) must match
- 4-wire RTD applications: Lead lengths (R_S) can differ
- Calibration procedure requires 4-wire configuration
- Lead wire compensation is updated every 5 signal conversions

Figure 7.33

USING THE AD1B60 IN AN INDUSTRIAL ENVIRONMENT

The circuit illustrated in Figure 7.34 shows how the AD1B60 might be used in an industrial environment where remote operation is required. The application requires that the AD1B60 be close to the thermocouple cold junction to minimize ground sense errors. In this circuit, an isolated power supply is used to provide power for the AD1B60 and the optocouplers. The low supply currents of the AD1B60 make the design of the isolated power supply undemanding. To communicate with the host system, optocouplers provide a high-speed, galvanically isolated digital interface.

In general, industrial environments place difficult requirements on integrated circuits. It is well known that these environments, where large voltage transients generated by heavy machinery or power failures are commonplace, wreak havoc on integrated circuits. It is also well known that devices constructed on CMOS-based processes are generally more susceptible to damage from these large transients than integrated circuits built with bipolar devices. Even though the ASIC in the AD1B60 is a custom CMOS device, it was designed to be "protectable"; that is, the design of the AD1B60's analog input circuitry allows for the addition of input protection circuitry without sacrifice of accuracy.

AN ISOLATED THERMOCOUPLE SIGNAL CONDITIONING APPLICATION CIRCUIT

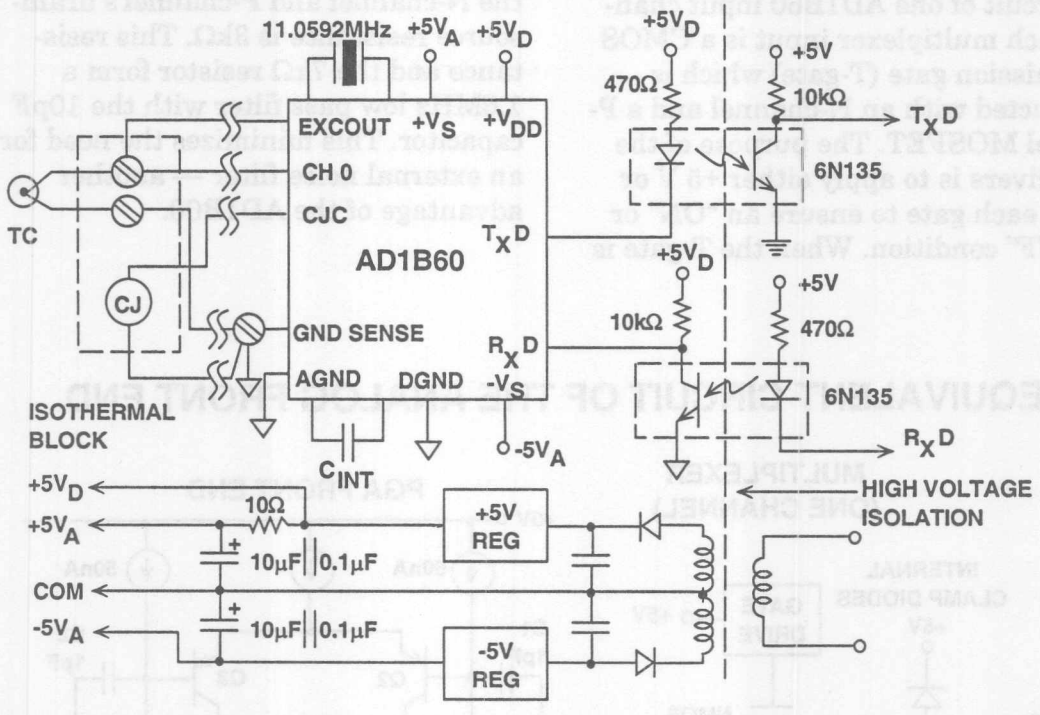


Figure 7.34

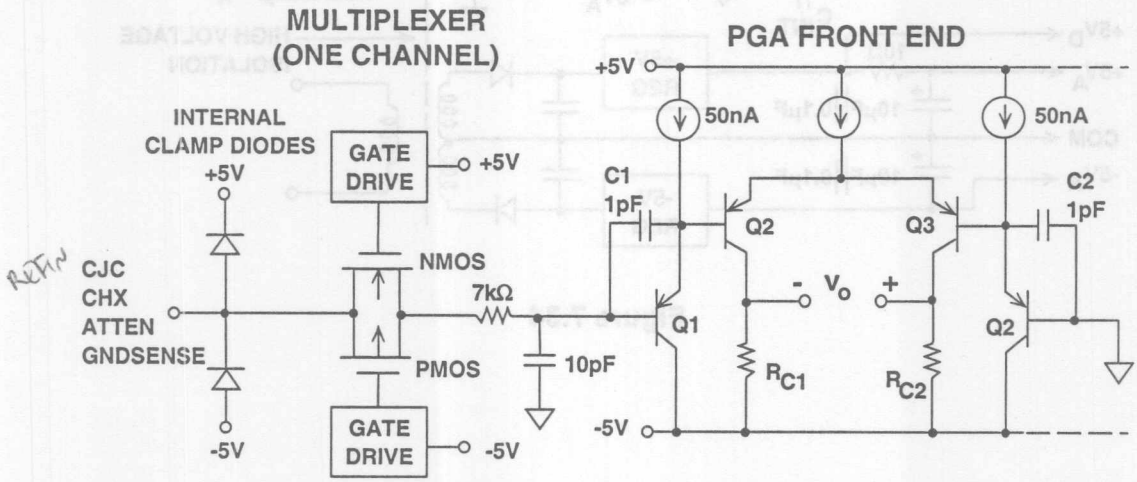
OPERATING THE AD1B60 IN HOSTILE ENVIRONMENTS

- Industrial environments wreak havoc with ICs
- CMOS is more susceptible than bipolar
- The AD1B60 is designed to be protected easily

Figure 7.35

Illustrated in Figure 7.36 is the equivalent circuit of one AD1B60 input channel. Each multiplexer input is a CMOS transmission gate (T-gate) which is constructed with an N-channel and a P-channel MOSFET. The purpose of the gate drivers is to apply either +5 V or –5V to each gate to ensure an "ON" or an "OFF" condition. When the T-gate is turned on, the parallel combination of the N-channel and P-channel's drain-source resistance is 3kΩ. This resistance and the 7kΩ resistor form a 1.6MHz low pass filter with the 10pF capacitor. This minimizes the need for an external noise filter — another advantage of the AD1B60.

EQUIVALENT CIRCUIT OF THE ANALOG FRONT END



- Multiplexer switch: NMOS/PMOS T-gate, Ron ≈ 3kΩ
- Ron + Low-Pass Filter: f_{3dB} = 1.6MHz
- PGA input bias current < 3na
- C1, C2 added to reduce RF rectification

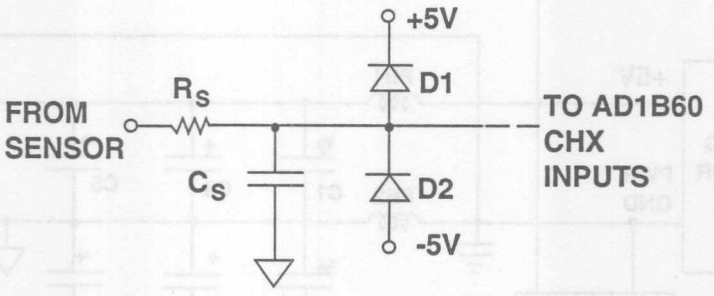
Figure 7.36

The input signal is then applied to the PGA whose input circuitry consists of a resistively-loaded PNP differential pair. To minimize input bias currents (and, thus, increase the input impedance), the differential pair is buffered by PNP emitter followers biased at 50nA. As a result of buffering the input differential pair, the AD1B60's input bias currents are typically 0.5nA (3nA, maximum). These low input bias currents permit the use of external fixed resistors for filtering or current limiting, if required. Capacitors C1 and C2 bypass the base-emitter transistor junctions of Q1 and Q2 at high frequencies. This high frequency bypass technique prevents the input emitter followers from rectifying high frequency noise. As discussed earlier in the seminar, RF rectification in bipolar transistors depends upon the ambient temperature and quiescent

current levels. Shunting the high frequency away from the junction proved to be an effective measure against high frequency interference. The values for C1 and C2 were determined empirically to limit high frequency interference without causing circuit instability. This technique worked well to filter noise up to 20MHz. Above that frequency the low pass filter formed by the T-gate's ON resistance, the 7kΩ resistor, and the 10pF capacitor rejects any high frequency interference. Last, clamp diodes connected to the analog supplies protect the input multiplexer channels against small transient overvoltages. However, in hostile environments where large transients could be applied to the AD1B60's inputs, additional external protection circuitry must be used.

The circuit illustrated in Figure 7.37 is an example of an inexpensive circuit for protecting the AD1B60's analog inputs against transient overvoltages. External diodes, D1 and D2, clamp the inputs safely to the supply voltages. To prevent parasitic transistor action, D1 and D2 should be low-leakage schottky diodes or low-leakage FETs. Low-leakage devices are required here because leakage currents double for every 10°C rise in ambient temperature and leakage currents generate offset errors.

PROTECTING THE AD1B60 ANALOG INPUTS FROM TRANSIENT OVERVOLTAGE CONDITIONS



- D1, D2: Low leakage Schottky diode, Type 5082-2835, or Low-Leakage JFETs, Type J202
- Limit diode current < 10mA
- Choose Rs ≅ V_{ov} /10mA; $P_D = V_{ov}^2/Rs$
- For filtering, limit Cs + C_{D1} + C_{D2} < 47pF

Figure 7.37

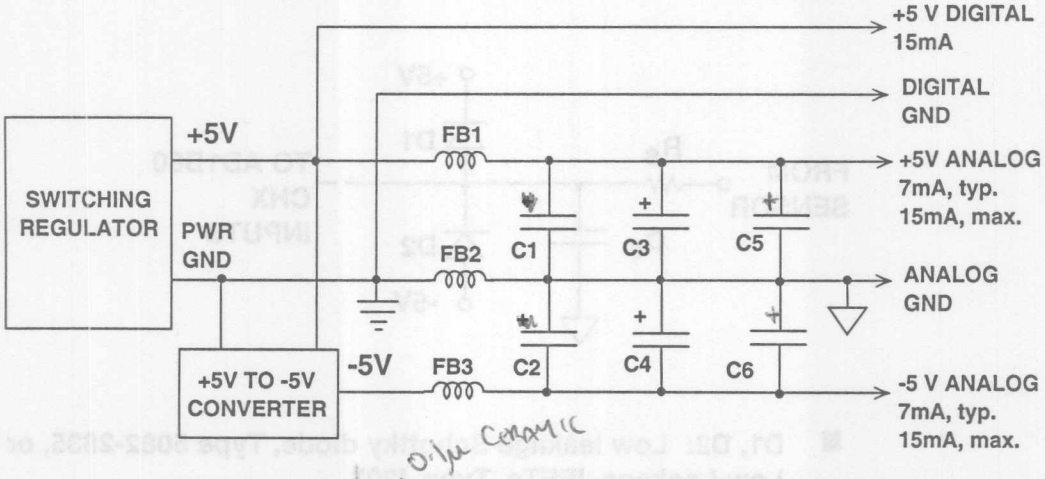
To limit diode current to 10mA, a resistor, R_S, can be used in series with the AD1B60 input. The value and power rating of the resistor depend upon the level of overvoltage protection required. If a series resistance is used in any of the AD1B60's inputs, an equal-valued resistance must be added to the GNDSENSE input to avoid errors due to resistive imbalance. For additional high-frequency filtering, an external capacitor, C_S, can be used. When an external capacitor is added to any AD1B60 input the sum of the diode capacitances plus the external capacitor should be less than 47pF, otherwise measurement errors may result from to multiplexer charge pumping.

SUPPLYING POWER TO THE AD1B60

There are no special requirements for power supplies for the AD1B60 since it only dissipates about 120mW. However, the AD1B60 does contain both analog and digital circuitry in the same package, and it is important to prevent any digital interference from coupling into the analog supply lines. Also, the digital +5V supply must not be allowed to exceed the analog +5V by more than 200mV. Otherwise, parasitic transistor action will occur.

The circuit shown in Figure 7.38 illustrates the techniques used to generate an analog-quality power supply from a +5V switching regulator. Switchers have a well-earned reputation for generating a great deal of noise over a wide range of frequencies. Ideally they ought not be used; however, their small size, high efficiency, and low cost have made them very popular and it is hard to avoid them.

SUPPLY POWER TO THE AD1B60 FROM A +5V SWITCHING REGULATOR



- FB1, FB2, FB3: 2 Turns, Fair-Rite #2677006301 Ferrite Beads
- C1, C2: ~~100µF Low ESR Electrolytic~~
- C3, C4: 10 - 22µF Tantalum
- C5, C6: ~~0.1µF Ceramic~~

Figure 7.38

The –5V supply is generated from a DC/DC converter, and the filter topology is a differential L-C type with separate power supply feeds for +5V, –5V, and common. With the values shown, the filter can easily handle 100mA of load current without saturating the ferrite cores. For lowest noise, all electrolytic capacitors should be low a ESR- (Equivalent Series Resistance) type.

LAYOUT TECHNIQUES FOR MAXIMUM PERFORMANCE

Oftentimes overlooked, the physical layout of a circuit plays almost as important a role as properly filtering the supply feeds. The performance of an AD1B60 can be compromised if the layout is not well thought out. Summarized in Figure 7.39 are the techniques to follow to achieve maximum performance from an AD1B60 or from any other high performance analog circuit.

USE PROPER LAYOUT TECHNIQUES TO MAXIMIZE PERFORMANCE

- Keep Analog Input Lead Lengths Short
- Bypass +Vs and -Vs with 10µF/0.1µF to AGND
- Bypass +Vd with 10µF/0.1µF to DGND
- Use Separate AGND and DGND Planes
- Tie AGND to DGND at One Point Only
- 2-Layer PC Board Works Best
- AD1B60 Evaluation Board Available

Figure 7.39

THE AD1B60 EVALUATION BOARD

A device such as the AD1B60 requires great care to achieve the highest level of performance. Analog Devices offers an evaluation kit for the AD1B60. The evaluation package includes an evaluation board, a menu driven program, and an extensive users guide. The self-contained, ready-to-use evaluation board includes an AD1B60 IC and an RS-232 serial communications port for direct connection to an IBM PC™, PC/XT™, PC/AT™, or compatible host computer system running PC-DOS™ operating system. Figure 7.41 is a simplified schematic diagram of the AD1B60 evaluation board used in a thermocouple application. Details for operating the evaluation board can be found in the AD1B60 Users Guide.

EVALUATION BOARD MAKES THE AD1B60 EASY TO USE

- RS-232 Serial Port Connector Provided For Easy PC Hookup
- Menu Driven Program Included
- Extensive AD1B60 Users Guide Available
- Downloadable Range Library Included

Figure 7.40

AD1B60 THERMOCOUPLE APPLICATION

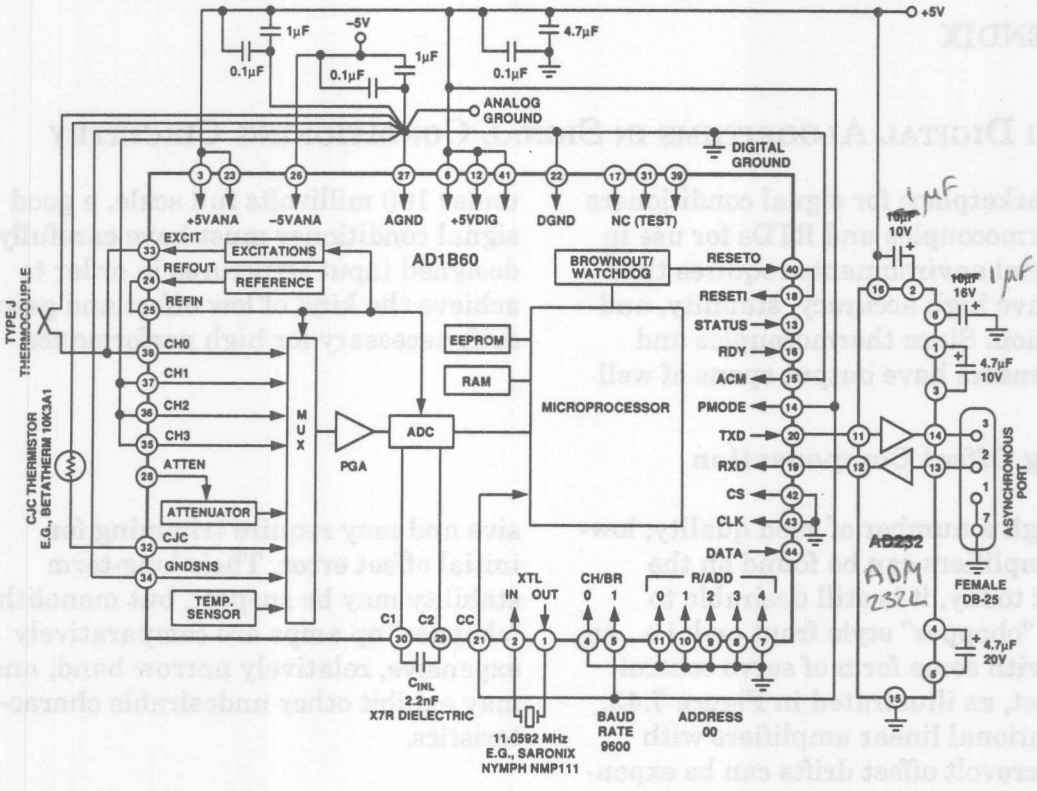


Figure 7.41

APPENDIX

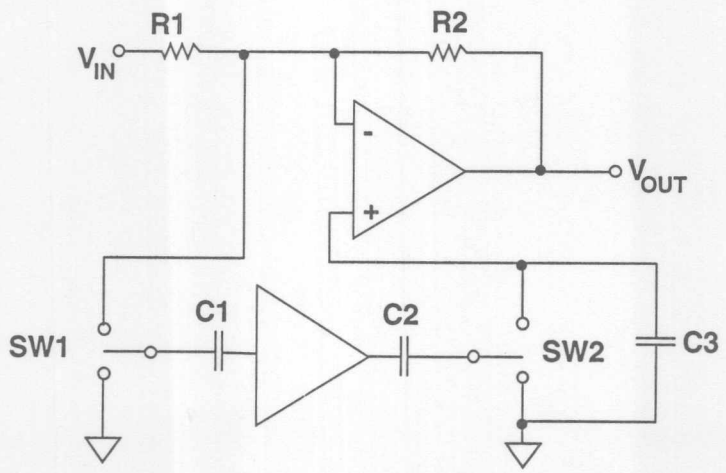
USING DIGITAL ALGORITHMS IN SIGNAL CONDITIONING CIRCUITRY

The marketplace for signal conditioners for thermocouples and RTDs for use in industrial environments requires that they have high accuracy, stability, and resolution. Since thermocouples and RTD sensors have output spans of well under 100 millivolts full scale, a good signal conditioner must have carefully designed input structures in order to achieve the kind of low offset and gain drift necessary for high performance.

Analog Offset Compensation

Although a number of good quality, low-drift amplifiers can be found on the market today, it is still desirable to have a "chopper" style front end; i.e., an input with some form of servo control for offset, as illustrated in Figure 7.42. Conventional linear amplifiers with sub-microvolt offset drifts can be expensive and may require trimming for initial offset error. Their long-term stability may be suspect, but monolithic "chopper" op amps are comparatively expensive, relatively narrow band, and may exhibit other undesirable characteristics.

ANALOG OFFSET COMPENSATION



CHOPPER STABILIZED AMPLIFIER

Figure 7.42

In a digital signal conditioner where A/D conversion is provided, the stability of a "chopper" op amp can easily be achieved by the addition of a simple multiplexer at the input. Instead of continuously chopping the input signal, a digitizing conditioner can alternately convert the input signal and a sample of true ground, as shown in Figure 7.43.

DIGITAL OFFSET COMPENSATION

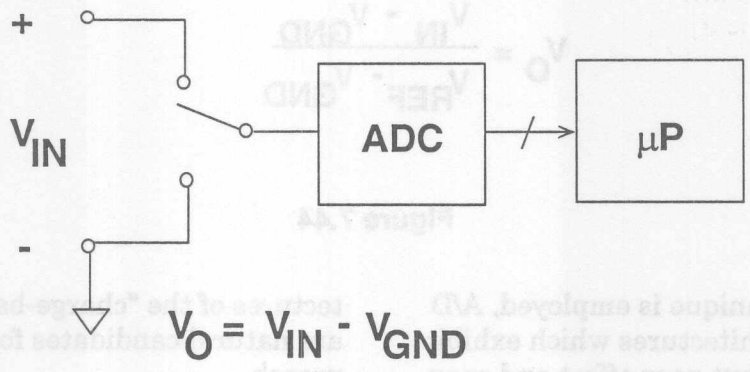


Figure 7.43

As long as the source impedances are reasonably well-matched, the microcontroller can simply subtract the value of the reading obtained at the ground sense input from the reading obtained at the signal input. Thus: $V_{OUT} = V_{IN} - V_{GND}$.

Since the offset is continuously sampled, the amplifier need not exhibit particularly good offset performance. Furthermore, the relatively slow offset sampling rate in this kind of system is not important, because whatever op amp is used it will drift quite slowly.

The same concept can be extended to include a servo control of the span. In most A/D converters, there are at least two separate components of span drift: the first is the drift of the voltage reference used by the converter, and the second is the drift of gain elements (i.e., resistors) within the converter itself.

As shown in Figure 7.44, an additional multiplexer input by which the reference voltage can be sampled allows all span error terms other than that of the reference to be canceled.

SPAN AND OFFSET COMPENSATION

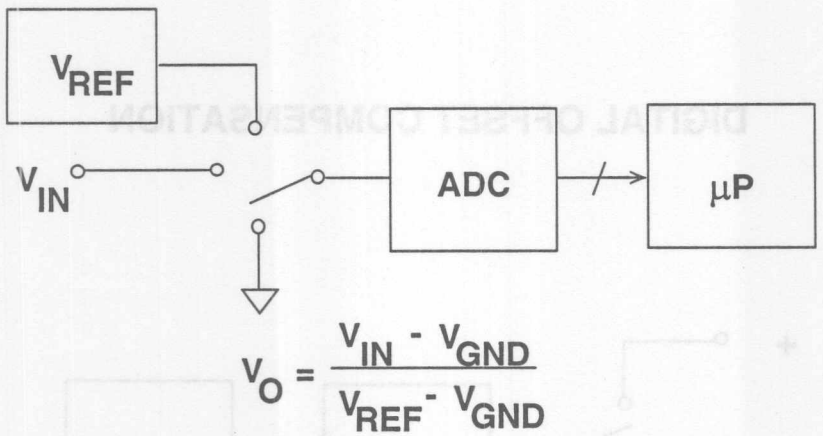


Figure 7.44

When this technique is employed, A/D conversion architectures which exhibit good linearity but poor offset and span stability can be considered. ADC architectures of the "charge-balancing" type are natural candidates for this approach.

Digital Calibration

Since most industrial measurements require absolute, rather than relative accuracy, all signal conditioners must contain some provision for calibration. In the simplest case, some means of adjusting the gain will be required, either at the factory or in the application.

Conventional analog signal conditioners can be calibrated in a number of different ways. Signal conditioners sold with a specified accuracy limit, and without any user-accessible trims, may be calibrated at the factory with fixed resistors, potentiometers, or even with laser-trimmed resistors networks. Some types of analog signal conditioners have user-accessible trim potentiometers, usually beneath a cover or other type of access panel.

However, trim controls can be a problem in the actual application. In particular, potentiometers can lose their precise setting under vibration and may also be susceptible to contamination by the environment.

Digital signal conditioners avoid the use of explicit calibration hardware via the use of digital calibration. The equation in Figure 7.44 can be modified to incorporate a span calibration factor, K_{SPAN}, which allows for the correction of full-scale error when multiplied with the output as shown in Figure 7.45.

DIGITAL SPAN CALIBRATION

$$V_{OUT} = K_{SPAN}\left(\frac{V_{IN} - V_{GND}}{V_{REF} - V_{GND}}\right)$$

$$K_{SPAN} = \frac{V_{REF(NOMINAL)}}{V_{REF(ACTUAL)}}$$

Figure 7.45

Once this algorithm has been implemented in the design, the voltage reference need not be precise since the nominal error can be compensated. However, to prevent measurement errors, the reference voltage must be stable.

The actual value of K_{SPAN} can be derived automatically. By forcing K_{SPAN} to unity and by performing a single conversion on a full-scale reference standard, the resulting output will simply be the reciprocal of the required calibration value.

The value for K_{SPAN} is stored in EEPROM (Electrically Erasable Programmable Read Only Memory). The use of EEPROM allows for K_{SPAN} to be changed to compensate for any long term drift of the reference.

Gain Correction for Gains Greater Than Unity

Although the algorithms described above were applied to unity-gain applications, the same techniques can be extended to applications requiring higher gains (such as thermocouple and RTD applications).

It is possible to use the circuit of Figure 7.44 with a fixed high gain amplifier preceding the A/D converter. However, scaling the voltage reference is necessary to match the effective full-scale input voltage. As a result, two drift error terms appear:

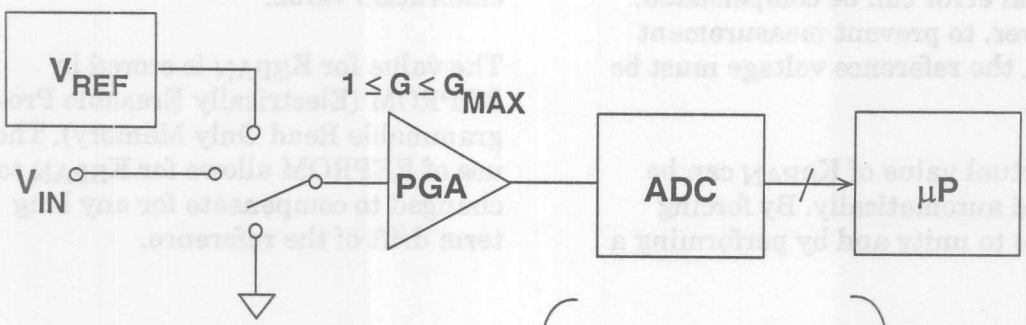
1) The drift of the reference attenuator, and

2) The drift of the gain-setting resistors in the amplifier.

An improved approach is to use a programmable gain amplifier in place of the fixed-gain amplifier, as shown in Figure 7.46. The lower limit of the PGA's gain range is set to unity. In this arrangement, two measurements are taken of the ground potential: one at unity and one at desired signal gain.

By applying both of these measurements, the algorithm now relates the measurements at the desired signal gain to the ratio of the span at the signal gain to the span at unity. Only one uncompensated drift term remains: the relative temperature coefficient of resistance of the thin-film network used in the PGA.

MULTIPLE GAIN COMPENSATION



$$\text{FOR } G = 1: \quad V_{OUT} = K_{SPAN} \times \left(\frac{V_{IN} - V_{GND@UNITY}}{V_{REF} - V_{GND@UNITY}} \right)$$

$$\text{FOR } G \ge 1: \quad V_{OUT} = K_{SPAN} \times K_{GAIN} \left(\frac{V_{IN} - V_{GND@SIGNAL\ GAIN}}{V_{REF} - V_{GND@UNITY}} \right)$$

Figure 7.46

This equation requires the introduction of a second calibration factor, K_{GAIN}, which accounts for the absolute gain error of the PGA at the signal gain. In practice, K_{SPAN} and K_{GAIN} can be combined into a single calibration factor to conserve both EEPROM space and execution time.

This concept can now be extended to any number of separate gain settings, with K-factors for each and forms the basis for "configurable" signal conditioners which can be programmed to handle a wide range of sensor inputs.

Analog Linearization

Thermocouples and RTD sensors require linearization if the desired output is scaled into engineering units. Although there are a small number of applications where the desired operating span of the sensor is narrow enough to be assumed linear, many applications include some form of linearization.

Analog signal conditioners accomplish linearization using hardware techniques. There are many ways to perform this task, each with varying degrees of complexity and conformance to the standard equations governing the sensor.

RTD sensors are easier than thermocouples to linearize. The nonlinearity of an RTD is a relatively gentle parabolic effect which can be canceled with fair accuracy by a circuit shown in Figure 7.47.

ANALOG RTD LINEARIZATION

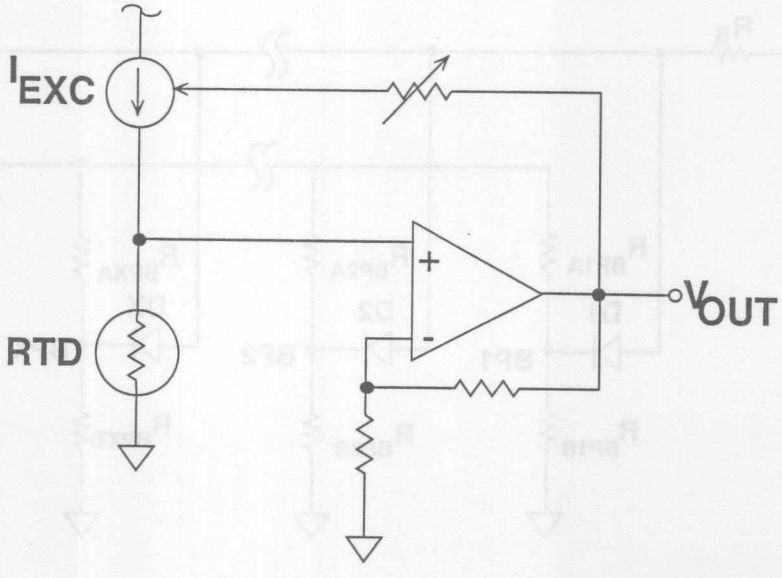


Figure 7.47

In this circuit, a portion of the amplified transducer output is fed back to the excitation circuit. This feedback, if properly scaled, warps the signal with a "bow" that is opposite in shape to that of the sensor output, yielding a linear result.

Thermocouples are more difficult to linearize since their nonlinearity is not a simple second-order function. The most common analog method of thermocouple linearization is the segment approximation method. This technique approximates the thermocouple transfer function as a connected series of straight line segments. With careful placement of the "breakpoints" (the junctions of the segments), a reasonably good fit to the thermocouple characteristic can be obtained.

The circuit in Figure 7.48 is a very simplified example of a passive breakpoint linearizer. At input voltages near zero, the circuit has unity gain and presents an impedance equal to R_S to the load. As the input voltage rises to V_{BP1}, diode D1 begins to conduct, and the circuit gain is reduced due to the shunting effect of the impedance at V_{BP1}. As the input voltage continues to rise to V_{BP2}, the second breakpoint activates (via diode D2) which further reduces the gain of the circuit. Each of the shunt elements in the circuit represents an additional breakpoint, whose turn-on point, as well as its effect on gain, can be arbitrarily chosen. The main drawback to this particular circuit is that the breakpoints are unidirectional; i.e., they can only reduce the gain, they cannot increase it. In practical applications, a more complex circuit with op amps is used so that the gain of the system can increase or decrease at each breakpoint.

ANALOG THERMOCOUPLE LINEARIZATION

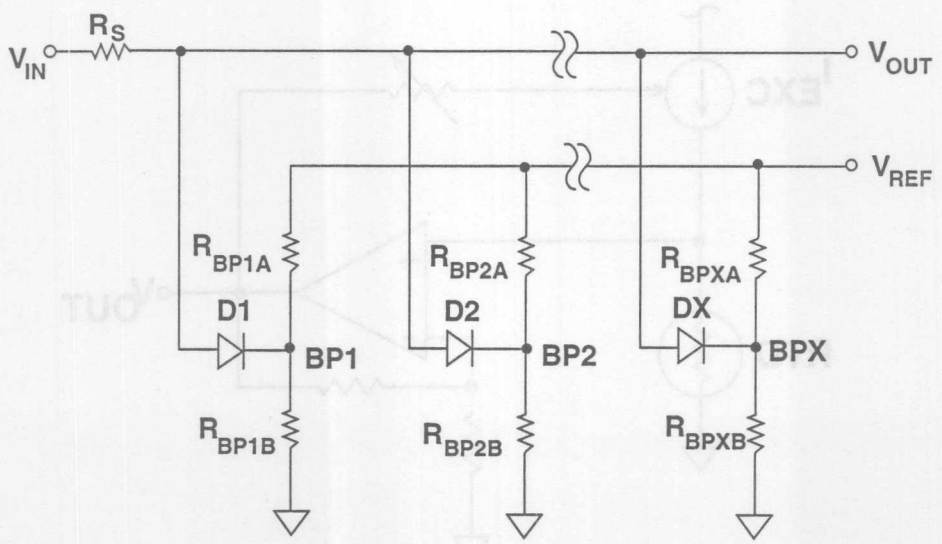


Figure 7.48

The drawback to hardware linearizers is their inflexibility — they must be designed for a specific sensor and operating range; they consume a great deal of circuit board area; and they usually require precision components because they are extremely difficult to trim.

Digital Linearization

In signal conditioners that incorporate both A/D conversion and "intelligence" (i.e., a microcontroller), linearization by digital means is the best approach. Apart from providing almost unlimited accuracy, digital implementations of linearization algorithms are flexible — accommodating a different sensor type involves no more than changing the coefficients of the linearization algorithm. Thus, the conditioner can be programmed for a variety of sensor transfer functions without altering its circuitry; hence, the term "configurable conditioner" is used.

There are tradeoffs when choosing an algorithm for implementing digital linearization. Microcontrollers can be exceedingly slow when asked to perform complex mathematical operations; thus, one such tradeoff is the complexity and precision of the required computation. Another tradeoff is memory which can be in short supply. Fast algorithms that depend upon lookup-tables can use a large amount of memory.

In general, implementing mathematical functions requires some margin of resolution to allow for truncation error. For example, sixteen-bit integer calculations could be employed in systems to produce a 14-bit result. However, the dynamic range of the mathematics must also be taken into account. For example, if polynomial approximation techniques are used, then the dynamic range of the coefficients may demand 24- or 32-bit computation to prevent saturation. Therefore, the selection of the mathematical approach will depend upon the nature of the linearization algorithm. In most cases, if dynamic range requirements call for 32-bit mathematics, IEEE single-precision floating-point routines are more efficient than integer routines. The memory requirements for each variable and/or constant are identical, but the dynamic range of IEEE floating-point routines is far less limited, and execution times are roughly comparable for most microcontrollers. Linearization techniques can take many forms, but the most common techniques are shown in Figure 7.49.

The simplest form of digital piece-wise linear approximation method is illustrated in Figure 7.50. The sensor output span is broken into a number of equal length segments, and a lookup table containing a set of offset and span correction values for each segment is stored in memory.

DIGITAL LINEARIZATION

- Single Polynomial
- Piecewise Linear Approximation
  - Equal Length Segment
  - Optimized Segments
- Segmented Polynomial Splines

Figure 7.49

BREAKPOINT LINEARIZATION WITH EQUAL LENGTH SEGMENTS

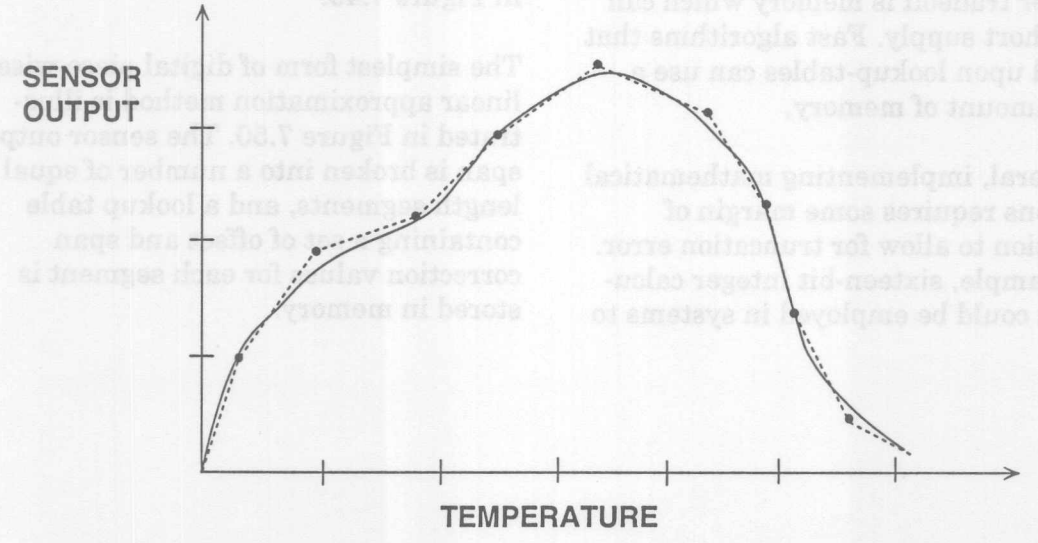


Figure 7.50

The algorithm determines the position of the sensor output relative to the table, retrieves the appropriate coefficients, and performs an "mx + b" operation on the sensor output to produce a linearized result. This approach has the advantage of high speed because only a single multiplication and addition are required to produce the result. However, it requires a large amount of memory to store coefficient table.

The disadvantage of the "equal length segment" method is that the error of approximation is different in each segment. One technique which can be used to minimize the error in each segment is the "optimized segment length" method. This is an advantageous approach because some portions of the thermocouple's curve are more nonlinear than others. Hence, the algorithm can choose the exact length of the segment to minimize the error, as shown in Figure 7.51. For example, shorter segments can be used to minimize the approximation error on portions of the curve where the sensor's output characteristic is curving sharply. Conversely in regions where the transfer function is linear, the segments can be longer. With this "optimized segment length" method, the coefficient table can have fewer entries for an equivalent worst-case error.

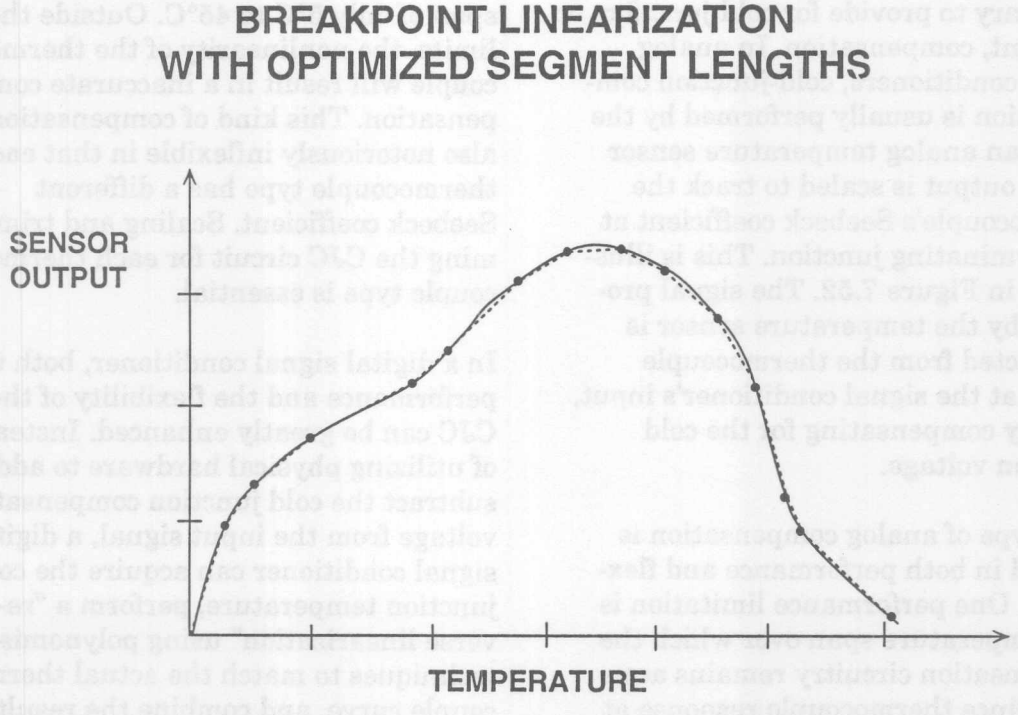


Figure 7.51

This particular method does have one drawback: the separations of the breakpoints vary. The coefficient table must contain the positions of the breakpoints, and the algorithm must search to locate the segment by comparing the sensor output to the breakpoint entries in the table. This segment search can be time consuming, and may negate the speed advantage.

In cases where memory conservation is more important that execution speed, polynomial linearization is a better choice. Only a modest number of coefficients must be stored, and the code for evaluating a polynomial is a simple recursive routine. In some cases, a polynomial approach may actually be faster than the optimized segment length method because no search for breakpoints is necessary.

The accuracy of the polynomial approximation is limited by the degree of the polynomial used which, in turn, is limited by the resolution and dynamic range of the mathematical capabilities of the microcontroller. If single-precision IEEE mathematics is used, the polynomial is constrained to 9th order or less. Fortunately, reasonable performance can usually be achieved with polynomials ranging from 5th to 7th order. The exception is the more nonlinear thermocouples when they are used over a wide temperature range.

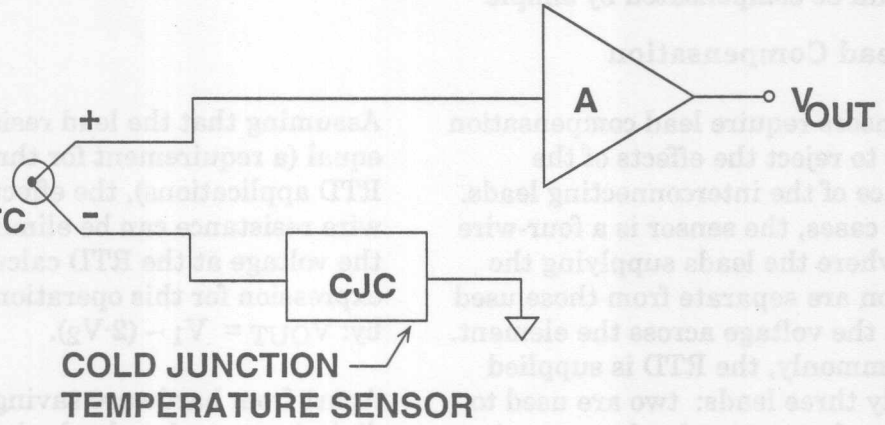
Cold-Junction Compensation

For a signal conditioner to perform linearization on thermocouples, it is necessary to provide for cold-junction, or ice-point, compensation. In analog signal conditioners, cold-junction compensation is usually performed by the use of an analog temperature sensor whose output is scaled to track the thermocouple's Seebeck coefficient at the terminating junction. This is illustrated in Figure 7.52. The signal produced by the temperature sensor is subtracted from the thermocouple signal at the signal conditioner's input, thereby compensating for the cold junction voltage.

This type of analog compensation is limited in both performance and flexibility. One performance limitation is the temperature span over which the compensation circuitry remains accurate. Since thermocouple response at the cold junction is nonlinear, most circuits of this type use a straight-line approximation to the thermocouple curve. Depending upon the particular thermocouple chosen, this approximation will have a useful temperature span of only 5°C to 45°C. Outside these limits, the nonlinearity of the thermocouple will result in a inaccurate compensation. This kind of compensation is also notoriously inflexible in that each thermocouple type has a different Seebeck coefficient. Scaling and trimming the CJC circuit for each thermocouple type is essential.

In a digital signal conditioner, both the performance and the flexibility of the CJC can be greatly enhanced. Instead of utilizing physical hardware to add or subtract the cold junction compensation voltage from the input signal, a digital signal conditioner can acquire the cold-junction temperature, perform a "reverse linearization" using polynomial techniques to match the actual thermocouple curve, and combine the result digitally with the input signal *after* the conversion process. A block diagram for such an operation is shown in Figure 7.53.

ANALOG COLD JUNCTION COMPENSATION



$$V_{OUT} = A(V_{TC} - V_{CJ})$$

Figure 7.52

DIGITAL COLD JUNCTION COMPENSATION

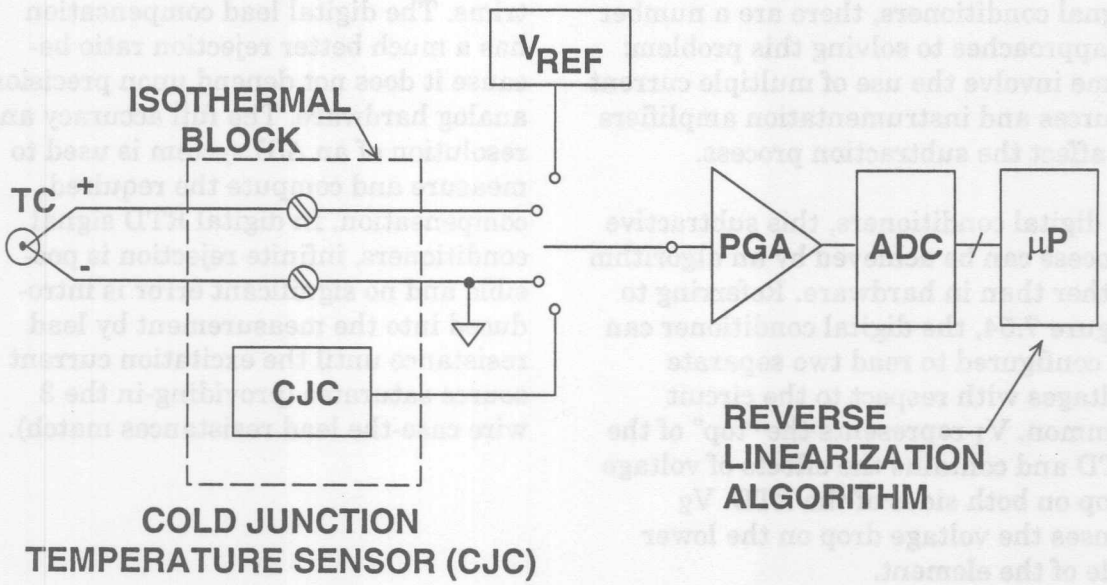


Figure 7.53

The functional advantages of this scheme are flexibility and simplicity, since no analog circuitry is required to combine the compensation voltage with the input signal. Thus, any thermocouple can be compensated by simple substitution of coefficients in the lookup table. This scheme can maintain compensation accuracy over the entire operating range of the signal conditioner.

RTD Lead Compensation

RTD sensors require lead compensation in order to reject the effects of the resistance of the interconnecting leads. In some cases, the sensor is a four-wire device where the leads supplying the excitation are separate from those used to sense the voltage across the element. More commonly, the RTD is supplied with only three leads: two are used to sense the element, and only one excitation lead is attached. One of the sensing leads is used as a return for the excitation current.

Circuits designed to interface to three-wire RTD sensors must contain some provision for reading the excitation drop across one side of the device, and subtracting this voltage drop from the sensor output to compensate for the other, unsensed, side. In analog RTD signal conditioners, there are a number of approaches to solving this problem: some involve the use of multiple current sources and instrumentation amplifiers to affect the subtraction process.

In digital conditioners, this subtractive process can be achieved by an algorithm rather than in hardware. Referring to Figure 7.54, the digital conditioner can be configured to read two separate voltages with respect to the circuit common. V_1 represents the "top" of the RTD and contains the effects of voltage drop on both sides of the RTD. V_2 senses the voltage drop on the lower side of the element.

Assuming that the lead resistances are equal (a requirement for three-wire RTD applications), the effect of lead-wire resistance can be eliminated, and the voltage at the RTD calculated. The expression for this operation is given by: $V_{OUT} = V_1 - (2 \cdot V_2)$.

Apart from hardware savings, the digital approach to lead-wire compensation also yields a significant performance advantage. The lead-wire resistance rejection capability of an RTD signal conditioner is often quoted as a ratio. In analog RTD conditioners, a typical specification might be 0.01Ω/Ω which means that a 1Ω difference in the lead resistance is perceived as 0.01Ω in the RTD. The rejection ratio depends upon the matching and tracking of current sources and/or precision analog trims. The digital lead compensation has a much better rejection ratio because it does not depend upon precision analog hardware. The full accuracy and resolution of an A/D system is used to measure and compute the required compensation. In digital RTD signal conditioners, infinite rejection is possible and no significant error is introduced into the measurement by lead resistance until the excitation current source saturates (providing-in the 3 wire case-the lead resistances match).

DIGITAL LEAD RESISTANCE COMPENSATION

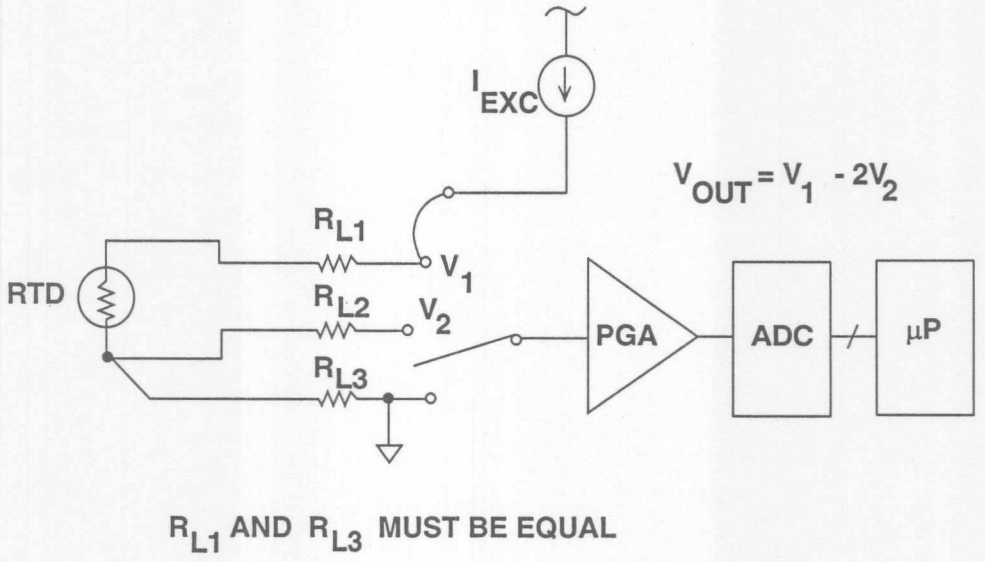


Figure 7.54

Conclusion

Although additional enhancements and corrections are theoretically possible, they have not been implemented due to memory and execution speed constraints. As microcontroller functions become faster and denser, it will be possible to extract significantly better performance from even simpler analog circuits.

Acknowledgments

In preparing this chapter, the author appreciated the support and helpful comments from Joe DiPilato, Ian Ramsden, and AD1B60 designers Howard Samuels and Dan Sheehan, all of Analog Devices' T & IP Division. The author also wishes to acknowledge the efforts of Norm Bernstein whose unpublished paper on digital signal conditioners formed the basis of this work.

SECTION 8

AUDIO APPLICATIONS

- AUDIO PREAMPLIFIERS:
  MIC PREAMPLIFIERS, RIAA PHONO PREAMPLIFIERS, TAPE PREAMPLIFIERS
- AUDIO LINE LEVEL STAGES:
  AUDIO LINE RECEIVERS, AUDIO LINE DRIVERS AND BUFFERS
- DC SERVO CONTROLLED AUDIO STAGES
- SPEAKER CROSSOVERS
- DIGITAL AUDIO APPLICATIONS:
  THE AD1879 18 BIT SIGMA-DELTA AUDIO ADC, APPLICATIONS FOR AUDIO DACS IN COMPACT DISC (CD) PLAYER ELECTRONICS
- DAC ARCHITECTURES
- STEREO CODECS FOR MULTIMEDIA AND BUSINESS AUDIO APPLICATIONS
- SIGNAL COMPUTING AUDIO CHIPSETS AND ALGORITHMS
- PERSONAL SOUND SYSTEMS USING THE AD20MSP614 AUDIO CHIPSET

SECTION 8

AUDIO APPLICATIONS

Walt Jung, Hank Zumbahlen, Walt Kester, David Fair

AUDIO PREAMPLIFIERS, LINE DRIVERS, AND LINE RECEIVERS

Walt Jung

AUDIO PREAMPLIFIERS

Audio signal preamplifiers (preamps) represent the low-level end of the dynamic range of practical audio circuits using modern IC devices. In general, amplifying stages with input signal levels of 10 mV or less fall into the preamp category. This section discusses some basic types of audio preamps, which are:

■ *Microphone* - including preamps for dynamic, electret and phantom powered microphones, using both transformer and transformerless circuits operating from dual and single supplies.

■ *Phonograph* - including preamps for moving magnet and moving coil phono cartridges using a variety of topologies, with detailed frequency response analysis and discussion.

■ *Tape* - including preamp designs useful for a wide range of playback standards including NAB and IEC, covering various time constants/tape speeds.

In general, when working signals drop to a level of 1 mV, the input noise generated by the first system amplifying stage becomes important for wide dynamic range and good signal-to-noise ratio. For example, if the internally generated noise voltage of an input stage is 1μV and the input signal voltage 1mV, the very best signal-to-noise ratio possible is just 60 dB.

In a given application, both the input voltage level and impedance of a source are usually fixed. Thus, for best signal-to-noise ratio, the input noise generated by the first amplifying stage must be minimized when operated from the intended source. This factor has definite implications to the preamp designer, as a "low noise" circuit for low impedances is quite different from one with low noise operating from a high impedance.

Successfully minimizing the input noise of an amplifier requires a full understanding of all the various factors which contribute to total noise. This includes the amplifier itself as well as the external circuit in which it is used, in fact *the total circuit environment must be considered*, both to minimize noise and to maximize dynamic range and general signal fidelity.

A further design complication is the fact that not only is a basic gain or signal scaling function to be accomplished, but *signal frequency response* may also need to be altered in a predictable manner. Microphone preamps are an example of wideband, flat frequency response, low noise amplifiers. In contrast, preamps for phonograph and tape circuits not only scale the signal, they also impart a specific frequency response characteristic to it.

MICROPHONE PREAMPLIFIERS

The microphone preamplifier (mic preamp) is a basic low level audio amplification requirement. Mic preamps can assume a variety of forms, considering the wide range of possible signal levels, the microphone types, and their impedances. These factors influence the optimum circuit for a specific application. In this section mic preamps are discussed which work with both high and low impedance microphones, both with and without phantom power, and with transformer as well as transformerless input stages.

Single-Ended, Single-Supply High-Impedance Mic Preamp

A very simple form of mic preamp is shown in Figure 8.1. This is a non-inverting stage with a single-ended input, most useful with high-impedance microphones such as dynamic and piezoelectric types. As shown it has an adjustable gain of 20-40 dB via variable resistance R_{GAIN}, and is useful with microphones (or other sources) with impedances of 600Ω or more.

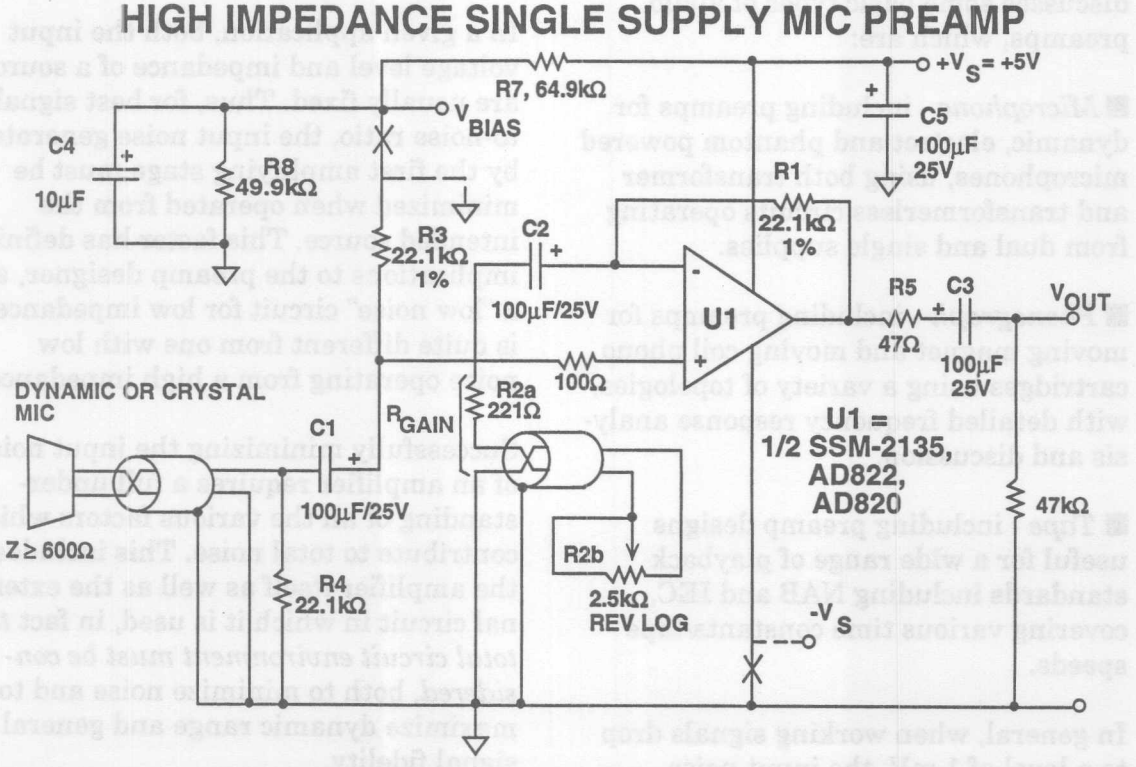


Figure 8.1

The op amp used for U1 greatly affects the overall performance, both in general amplification terms but also in suitability for single supply operation, as shown here. In terms of noise performance, U1 should have a low input noise with ≥500Ω sources, with the external circuit values adjusted so that the source impedance (microphone) dominates the overall source resistance. For very low noise on a single 5V power supply, very few devices are suitable. Among these the dual SSM-2135 and AD822 as well as the single AD820 stand out, and are recommended as first choices. Many other low noise devices can work well in this circuit when the total supply voltage is 10V or more, for example the OP-275, and OP-270/470 types. The circuit can also be easily adapted for dual supply use, as noted below.

In this circuit, gain-determining resistors R_1 || R_2 (where $R_{2a} + R_{2b} = R_{GAIN}$) are scaled such that their total resistance is less than the expected source impedance, that is 1kΩ or less. This minimizes the contribution of the gain resistors to input noise at high gain. As noted, gain of the circuit is adjusted in the feedback path via resistor R_{GAIN}. Control of a microphone or other low level channel signal level is preferably done after it has been amplified, as here.

Because of single supply operation, input and output coupling is of necessity via capacitors, three in the circuit itself and 2 more for bypassing. These should preferably be low ESR types (which is a byproduct of the higher voltage rating).

For lowest noise in the surrounding circuit, the amplifier biasing must also be *noiseless*, that is free from noise added directly or indirectly by the biasing.[1] Resistors with DC across them should have low excess noise, or be AC-bypassed. Thus R_1, R_2, R_3, R_7, and R_8 are preferably metal films, and R_7-R_8 are bypassed. A 2.2V bias source is provided from R_7- R_8, which biases the output of U1 about mid-supply. If higher supply voltages are used, R_7-R_8 can be adjusted for maximum output swing for a particular amplifier.

While the SSM-2135 is optimum for U1 when operating from low impedance sources, the FET input AD820 (or AD822) is preferable when using high impedance sources, such as crystal or ceramic mics. To adapt the circuit for such sources, R_3 and R_4 should be 1MΩ or more, and C_1 can be a 0.1μF film capacitor.

Bandwidth is about 30kHz at maximum gain using the SSM-2135 , or about 20kHz for similar conditions with the AD822 (or AD820). Distortion and noise performance will reflect the device chosen for U1 and the source impedance. With a shorted input, the SSM-2135 has an output noise of about 110μVrms at a gain of 100, with a 1kHz THD+N of 0.022% at 1Vrms into a 2kΩ load. The AD820 measures about 200μVrms with 0.05% THD+N under similar conditions. For either device, these figures will improve at lower gains.

The circuit of Figure 8.1 is good if modest performance and simplicity are required, but will require attention to details for best results. The input cable to the microphone must be shielded, and should be no longer than required. Similar comments apply to any cable used for R_{GAIN}. To adapt the circuit for dual supply use, R_3 is returned to ground, and U1 is operated on symmetric supplies (±Vs = ±5V, ±15V, etc.)

Although microphones with impedances of less than 600Ω can be used with this circuit, noise performance will not be optimum, and many such microphones also require a balanced input interface.

Electret Mic Interface

A popular microphone for speech recording and other non- critical applications is the electret. This is a polarized condenser microphone, typically with a built in FET amplifier. The amplified output signal is taken from the same lead which supplies the microphone with DC power, typically from a 5-10V DC source.

Figure 8.2 illustrates an interface circuit which is useful in powering and scaling the output signal of an electret mic for further use. In this case the Circuits which show methods of optimizing noise performance with low impedance, balanced output microphones are illustrated below.

scaled output signal from this interface is fed into the LEFT and RIGHT inputs of an AD1848 or AD1849 16 bit CODEC for digitization and processing. DC phantom power is fed to the two mic capsules by the R_A-C_A- R_B decoupling network from the +5V supply, and the AC output signal is tapped off by C_{IN}-R_2, and fed into a scaling amplifier, U1. The R_B resistors may of course vary with different electret mics and DC supply voltages, and the values shown are typical.

ELECTRET MIC INTERFACE FOR AD1848 OR AD1849 CODEC

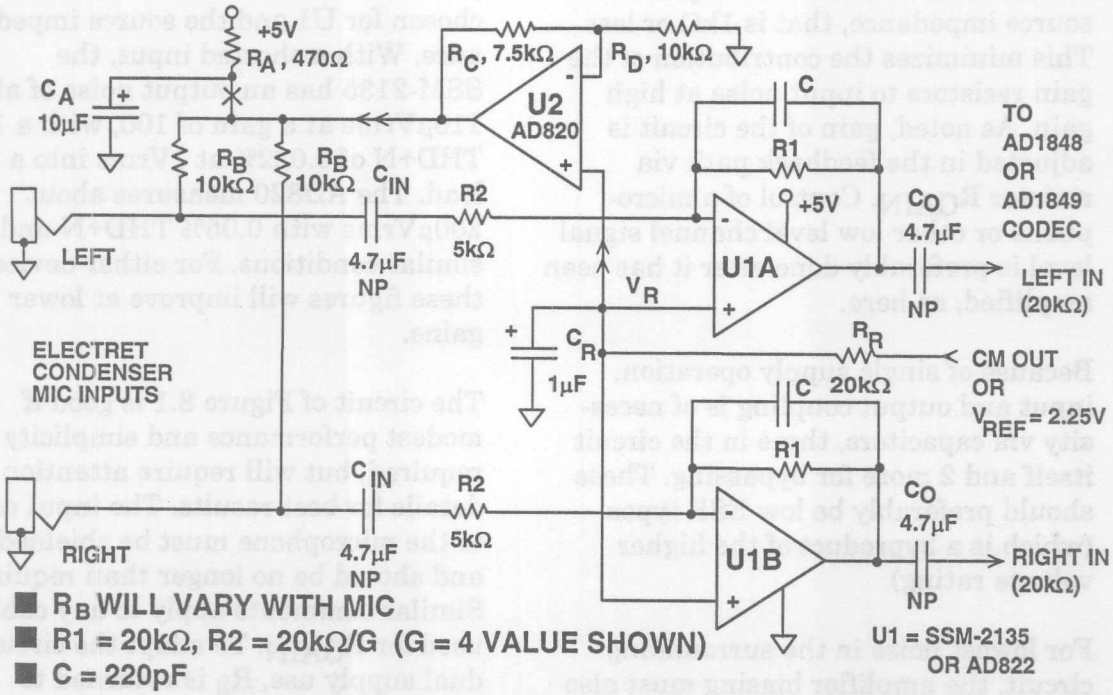


Figure 8.2

The U1 scaling amplifier is a dual SSM-2135 or AD822, and is used here to normalize the mic signal to either a 1Vrms line level or 100mVrms mic level required by the CODEC inputs, and also to low pass filter it prior to digitization. With a wide variety of electret mics and operating parameters, some scaling or normalization of signal level is often required.

Here the scaling gain is simply R_1/R_2, and resistor R_2 is selected as noted, to provide the gain "G" so as to yield 1Vrms at the line inputs (or .1Vrms at the mic inputs) of the CODEC, with the rated output from the mic. Note that since the U1 stages are inverting, G can be greater or less than unity. For example, it can be 4, as is shown here, or as required to normalize any practical input signal to an optimum level for the CODEC. The amplifier's low pass corner frequency is set by the time constant R_1-C, resulting in a -3dB point of 36kHz. DC bias for the two U1 stages is provided from the CODEC, via the V_{REF} or CMOUT pins, which provides a filtered 2.25V reference voltage.

The low frequency time constants C_{IN} - R_B/R_2 and C_O - 20kΩ are wideband, to minimize LF phase shift. For speech or other narrowband uses, these (non-polar) capacitors can be reduced to 1μF or less.

If a more stable and quiet supply voltage for mics than the system 5V supply is desired, a filtered and scaled version of V_R can be generated by the optional U2 connnected as shown. The output from U2 , rather than the output voltage from R_A-C_A, feeds the two R_Bs directly. When an AD820 is used for U2, resistors R_C-R_D scale V_R up to 4V for the values shown. Note that if output voltages within 1V of the 5V supply are required, the U2 op amp must be a rail-rail device, such as an AD820 or AD822.

8

Transformer-Coupled Low-Impedance Mic Preamps

For any op amp, the best noise performance is attained when the characteristic *noise resistance* of the amplifier, R_n, is equal to the source resistance, R_s. Examples of microphone preamps that make use of this factor are discussed in this section. They utilize an input matching transformer to optimize an amplifier to a source impedance which is not equal to the amplifier R_n.

A basic circuit operating on this principle is shown in Figure 8.3. In order to select an optimum transformer turns ratio to match a given source resistance (R_s) to the characteristic R_n of the op amp in use, R_n must first be calculated from data for e_n and i_n as follows:

$$R_n = \frac{e_n}{i_n} \qquad \text{Eq. 8.1}$$

where e_n is in V/√Hz and i_n is in A/√Hz.

TRANSFORMER INPUT MIC PREAMP WITH 28 TO 50dB GAIN

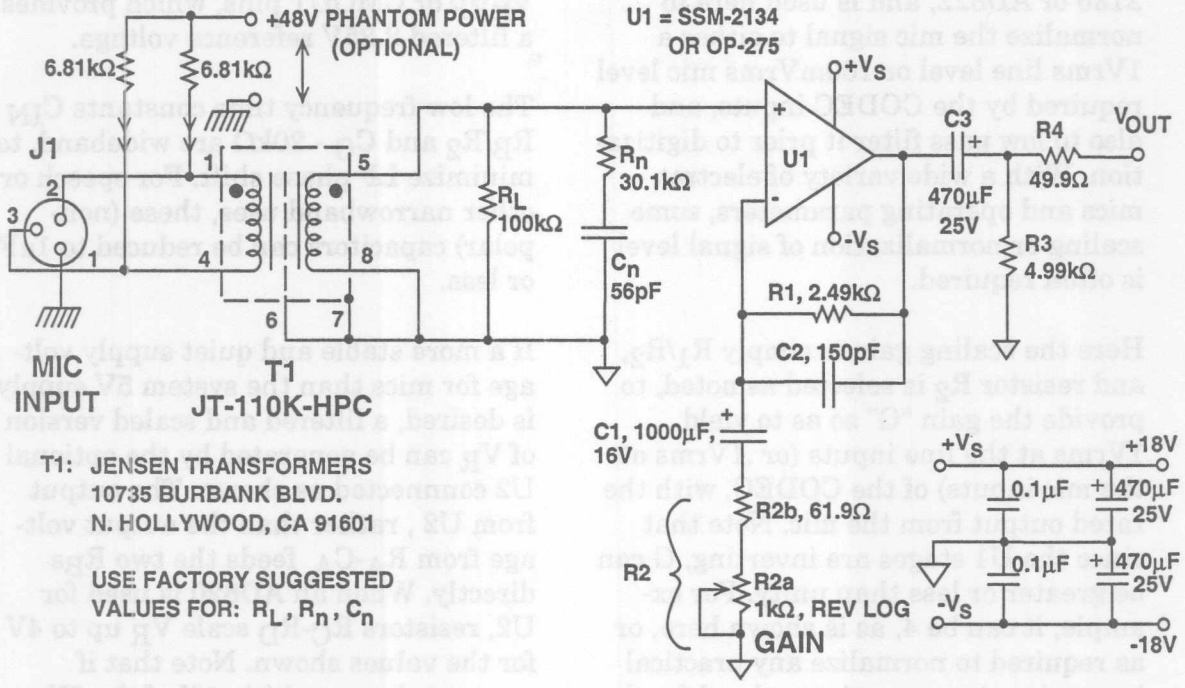


Figure 8.3

Then, a turns ratio for T1 may be calculated as:

$$\frac{N_s}{N_p} = \sqrt{\frac{R_n}{R_s}} \qquad \text{Eq. 8.2}$$

where N_s/N_p is the transformer secondary/primary turns ratio. For the SSM-2134 amp, the values of e_n and i_n are 3.5nV/√Hz and 0.6 pA/√Hz, respectively; thus,

$$R_n = \frac{e_n}{i_n}$$

$$= \frac{3.5 \times 10^{-9}}{0.6 \times 10^{-12}}$$

$$= 5.8k\Omega$$

Since both e_n and i_n vary with frequency, R_n will also vary with frequency. Therefore, a value calculated for R_n from the data sheet (such as above) is most accurate at the specified frequency. If the amplifier is to be optimized for a specific frequency, then the e_n and i_n values should be for that frequency. However audio amplifiers are wideband circuits, so some compromise is likely. When available, a minimum- noise-figure plot for the amplifier will allow graphical determination of the optimum source resistance for least noise.

For this case, an optimum transformer turns ratio can be calculated to provide the optimum R_n to the op amp, working from a given R_s. For example, if R_s is 150Ω, then an optimum turns ratio for an SSM-2134 (or other amplifier) with an R_n of 5.8kΩ will be:

$$\frac{N_s}{N_p} = \sqrt{\frac{R_n}{R_s}}$$

$$= \sqrt{\frac{5.8 \times 10^3}{1.5 \times 10^2}}$$

$$\approx 6.2$$

Other devices with similar e_n/i_n (and thus R_n) can also be so applied, for example the OP-275, the OP-27 or OP-37, and the OP-270/470 types, etc.

Since transformers are catalogued and stocked in fairly narrow and specific impedance ranges, a unit with a rated secondary impedance in the range of 5kΩ to 10kΩ will be useful (since the amplifier minimum noise impedance is reasonably broad). Suitable units for this purpose are the Jensen JT- 13K7-A, JT-110K-HPC, and the JT-115K-E. Of course, T1 must be adequately shielded and otherwise suitable for operation in low-level environments.

The use of a matching transformer allows the circuit to achieve an equivalent input noise (referred to the transformer input) that is only a few decibels above the theoretical limit, or very close to the thermal noise of the source resistance. For example, the thermal noise of a 150Ω resistor in a 20kHz noise bandwidth at room temperature is 219nV. An actual circuit will have a total input referred noise higher than this ideal, due to the noise-degradation of the transformer plus the op amp.

An additional advantage of the transformer lies in the *effective voltage gain* that it provides, due to the step up turns ratio. For a given circuit total numeric gain, G_{total}, this reduces the gain required from the op amp U1, $G_{(U1)}$, to:

$$G_{(U1)} = \frac{G_{total}}{N_s / N_p} \quad \text{Eq. 8.3}$$

Thus, in the composite circuit of Figure 8.3 gain G_{total} is the product of the transformer step up, Ns/Np, and $(R_1 + R_2)/R_1$, which is $G_{(U1)}$. This has advantages of allowing more amplifier loop gain, thus greater bandwidth and accuracy, lower distortion, etc.

The transformer input mic preamp stage of Figure 8.3 uses the JT-110K-HPC transformer for T1 with a primary/secondary ratio of about 1/8 (150Ω/10kΩ). The op amp section has a variable gain of about 3.3-41 times, which, in combination with the 17.8dB transformer gain, yields a composite gain of 28 to 50 dB (26 to 300 times). Transient response of the composite amplifier (transformer plus U1) is excellent.

The amplifier used as U1 is either a unity gain compensated SSM-2134, or an OP-275 section. U1 operates here on supplies of ±18V (up to ±22V maximum), and can drive 600Ω. The power supplies used should be well regulated and decoupled close to U1, particularly when low impedance loads are driven.

For best results, passive components should be high-quality, such as 1% metal film resistors, a reverse log taper film pot for R_{2a}, and low ESR capacitors for C_1 & C_3. Microphone phantom powering[2,3] can be used, simply by adding the ±0.1% matched 6.81kΩ resistors and a 48V DC source, as shown. Close matching of the DC feed resistors is recommended by the transformer manufacturer whenever phantom power is used, to optimize CMR and to minimize the transformer's primary DC current flow.[4] Note that use of phantom powering has little or no effect on the preamp, since the

transformer decouples the CM DC variations at the primary. CMR in an input transformer such as the JT-110K-HPC is typically 85dB or more at 1kHz, and substantially better at lower frequencies. Lower impedance ratio types such as the JT-16A (below) have even higher typical 1kHz CMR, i.e. 100dB.

Performance of this mic preamp for THD+N is shown in the family of curves in Figures 8.4 and 8.5, reflecting use of the OP-275 and SSM-2134 devices, respectively. The test conditions are 35dB gain, and successive input sweeps resulting in outputs of 0.5, 1, 2, and 5Vrms into 600Ω. For these distortion tests as well as most of those following throughout these sections, THD+N frequency sweeps at various levels are used for sensitivity to slewing related distortions[5-7], while output loaded tests are used for sensitivity to load related non-linearities.

TRANSFORMER INPUT MIC PREAMP WITH OP-275
THD + N (%) VERSUS FREQUENCY (Hz)
FOR V_{out} = 0.5, 1, 2, AND 5V rms, GAIN = 35dB, R_L = 600Ω

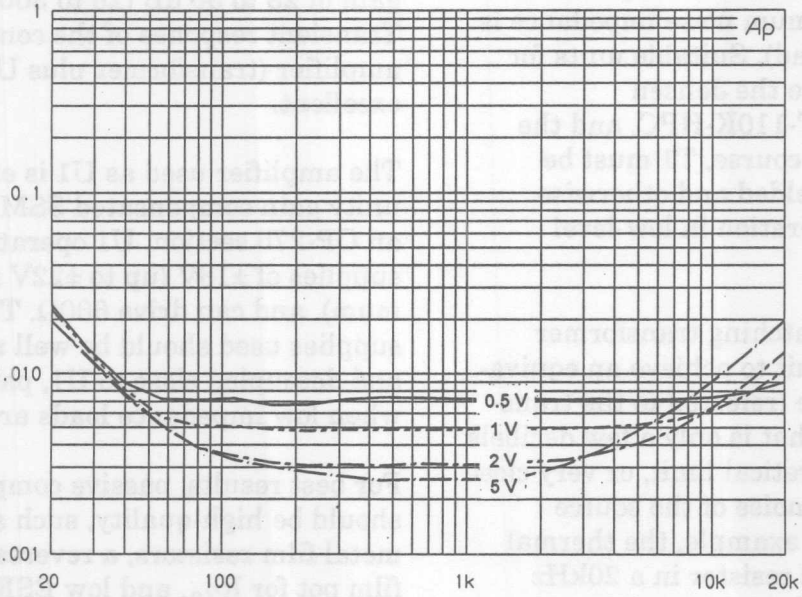


Figure 8.4

TRANSFORMER INPUT MIC PREAMP WITH SSM-2134 THD + N (%) VERSUS FREQUENCY (Hz) FOR V_{out} = 0.5, 1, 2, AND 5V rms, GAIN = 35dB, R_L = 600Ω

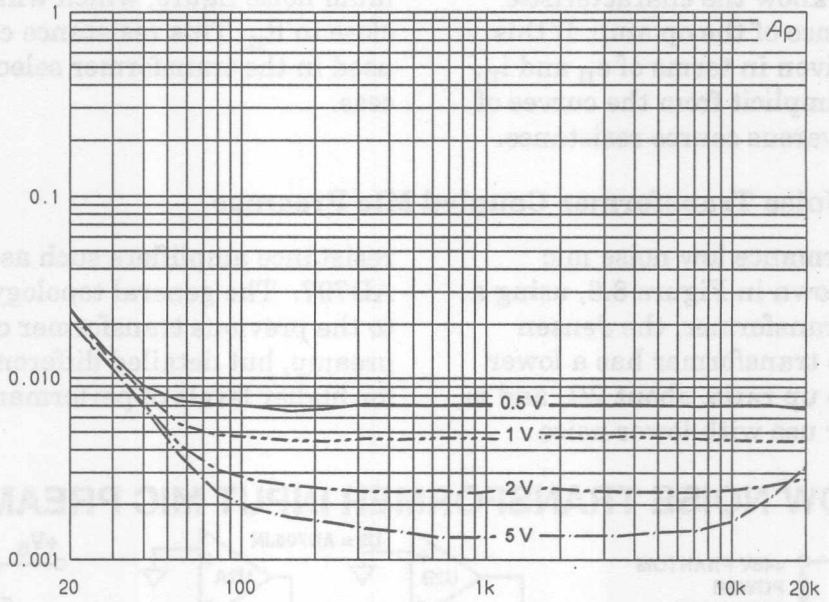


Figure 8.5

For the OP-275, as shown in Figure 8.4, there exist three regions of interest, a low frequency region below 100Hz where distortion is largely due to the transformer, a mid-band region from 100Hz-3kHz where distortion is lowest, and the region above 3kHz where the distortion rises. Over most of the frequency spectrum THD+N is 0.01% or less for medium output levels, becoming slightly higher at high frequencies. For the SSM-2134 performance shown in Figure 8.5 there is the same rise at low frequencies due to the transformer, but THD+N is below 0.01% at all frequencies above 50Hz, and at all levels.

The -3dB bandwidth of this circuit is about 100kHz, and is dominated by the JT-110K-HPC transformer and its termination network, assuming a 150Ω source impedance. Conversely, for higher or lower source impedances, the bandwidth will lower or rise in proportion, so applications of this circuit should take this into account. Some provision should be made to control the source impedance with a build-out pad prior to the transformer, if it is to be used with source impedances lower than 150Ω.[4] One such example is capacitor microphone capsules with emitter follower outputs, which appear as a ≈15Ω source.

A circuit functioning similarly to Figure 8.3 but with servo control of offset could also be an option, by using a second op amp as a servo amp. Alternately, the mic preamp in Figure 8.6 shows an optimized servo stage used for this purpose, which allows elimination of capacitors C_1/C_3 and direct coupling to the load.

Finally, although this transformer input preamp has been discussed in terms of a low impedance source

(microphone), the transformer-matching technique is applicable to other transducers of any impedance. It is only necessary to know the characteristic noise resistance of the op amp. If this data is not given in terms of e_n and i_n, it is usually implicit from the curves of noise figure versus source resistance.

The noise figure is at a minimum when $R_n = R_S$; therefore, it is only necessary to verify the source resistance for minimum noise figure, which will be very close to R_n. This resistance can then be used in the transformer selection process.

Very Low Noise Transformer Coupled Mic Preamps

A high performance low noise mic preamp is shown in Figure 8.6, using a lower ratio transformer, the Jensen JT-16A. This transformer has a lower nominal step up ratio, about 2/1, and is optimized for use with lower noise resistance amplifiers such as the AD797. The general topology is similar to the previous transformer coupled preamp, but detailed differences allow for higher levels of performance.

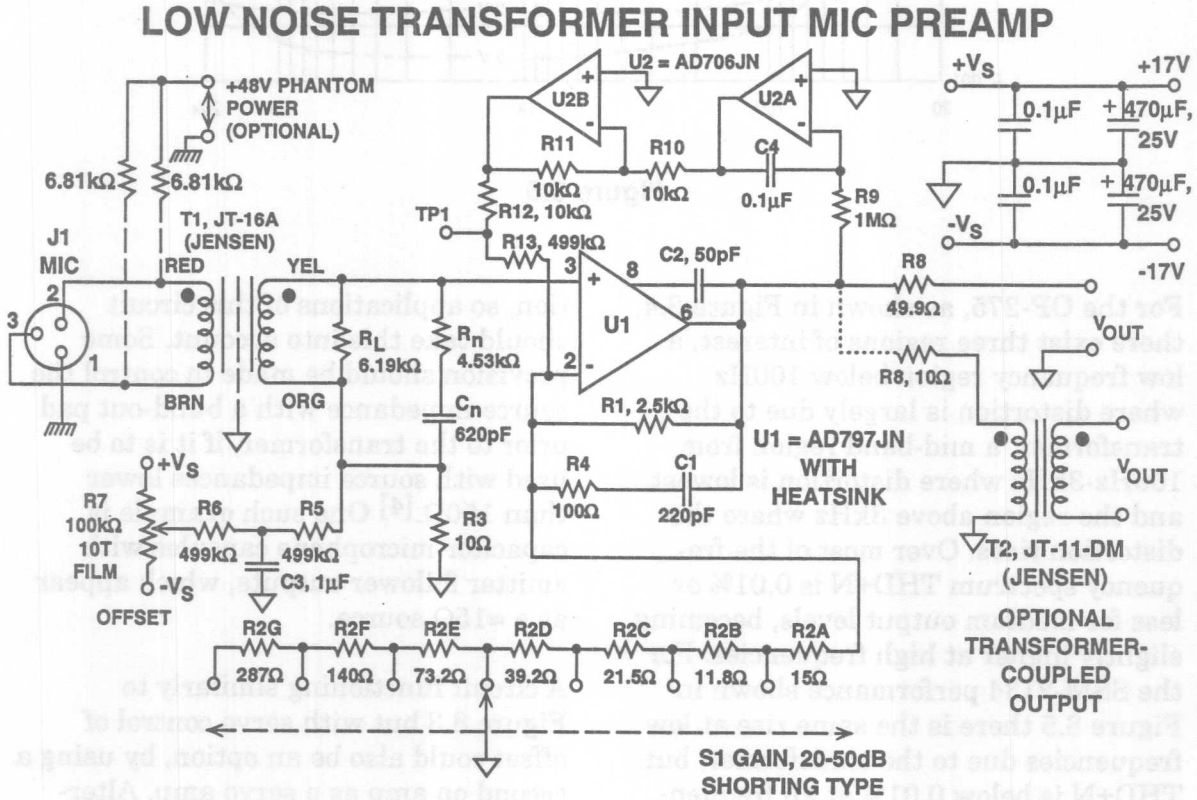


Figure 8.6

This preamp has switch selected variable gain, using switch S1 to alter R_2 of the feedback network to vary U1's gain (and thus overall gain) according to Figure 8.7. The range chosen is 20-50dB, suitable for a wide range of uses, and gain is selected in 5dB increments.

R2 VALUES FOR 20 TO 50 dB GAINS

TOTAL GAIN, dB	U1 GAIN, dB	R2 (TOTAL), Ω	"R2N", Ω
50	44.4	15.15	15.0
45	39.4	27.07	11.8
40	34.4	48.56	21.5
35	29.4	87.68	39.2
30	24.4	160.3	73.2
25	19.4	300	140
20	14.4	588.5	287

- T1 Provides a Fixed 5.6dB Gain
- R2N is individual R2A, R2B, etc.
- Closest Standard Values are Shown

Figure 8.7

Inasmuch as the AD797 has high DC precision as well as low distortion audio characteristics, this circuit can be DC coupled quite effectively. Initial device offset of the AD797 is 80μV(max), allowing a simple trim by R_7 to null output offset. Offset is trimmed out with the servo temporarily defeated by grounding test point TP1, and trimming the output DC to less than 1mV, while at a mid-range gain setting of 35dB. Offset shift with gain is only a few mV, and is of little concern, as the servo circuit composed of U2A and U2B holds longer term DC offset to 100μV or less, with very little gain interaction.

Performance of this mic preamp for THD+N is shown in Figure 8.8, for conditions of 35dB gain, and successive input sweeps resulting in outputs of 0.5, 1, 2, and 5Vrms into 600Ω. From these data it is clear that essentially the only distortion in the circuit is due to the transformer, and this is quite small and only present at the lowest frequencies. Above 100Hz, the apparent distortion is noise limited, continuing through to the highest frequencies.

LOW NOISE TRANSFORMER INPUT MIC PREAMP THD + N (%) VERSUS FREQUENCY (Hz) FOR V_{out} = 0.5, 1, 2, AND 5V rms, GAIN = 35dB, R_L = 600Ω

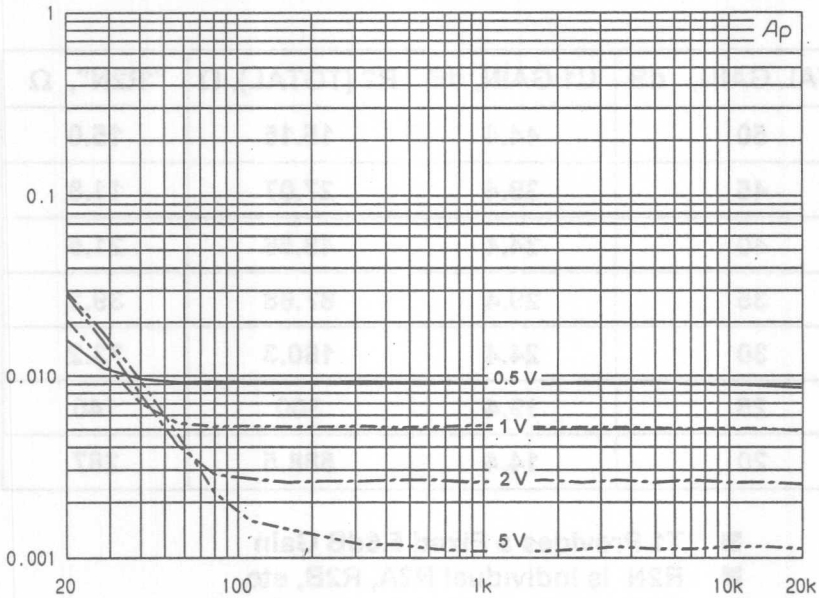


Figure 8.8

The -3dB bandwidth of this circuit is just under 150kHz, and while essentially dominated by the JT-16A transformer and termination, reduces slightly at the highest gain (50dB). Like the previous transformer coupled circuit, this circuit also assumes a 150Ω source impedance, and similar caveats in application are true. Reference [4] includes information on both build out and fixed loss input pads, and other practical interfacing considerations for transformers.

The basic circuit as shown is single-ended with V_{OUT} taken from R_8, but a transformer can be added to drive balanced lines. If used, T2 is a JT-11-DM (or similar) nickel core type for lowest distortion, and is coupled to U1 as shown.

If very high levels of output drive are necessary or long lines are to be driven, a dedicated high current output driver should be used with U1, as described in the "Line Drivers" section. This can be most easily implemented by making U1 a composite amplifier employing an AD797 input section plus a unity-gain follower output stage, using the AD811.

Transformerless Input Low-Impedance Mic Preamp

Another method of amplifying low level balanced mic signals is the use of a *transformerless* differential input stage, using an instrumentation amplifier (in-amp) as the preamp. The in-amp (in IC or other form) is configured for gain with just one resistor. It provides transformerless gain with good rejection of CM noises such as hum, and has low operating noise with commonly used mics.

Figure 8.9 is an example of a low noise transformerless mic preamp, using the SSM-2017P (U1) and an OP- 275GP op amp (U2). This circuit is a mic preamp with gain variable over a range of 6-66dB with an optional phantom power feature.[8]

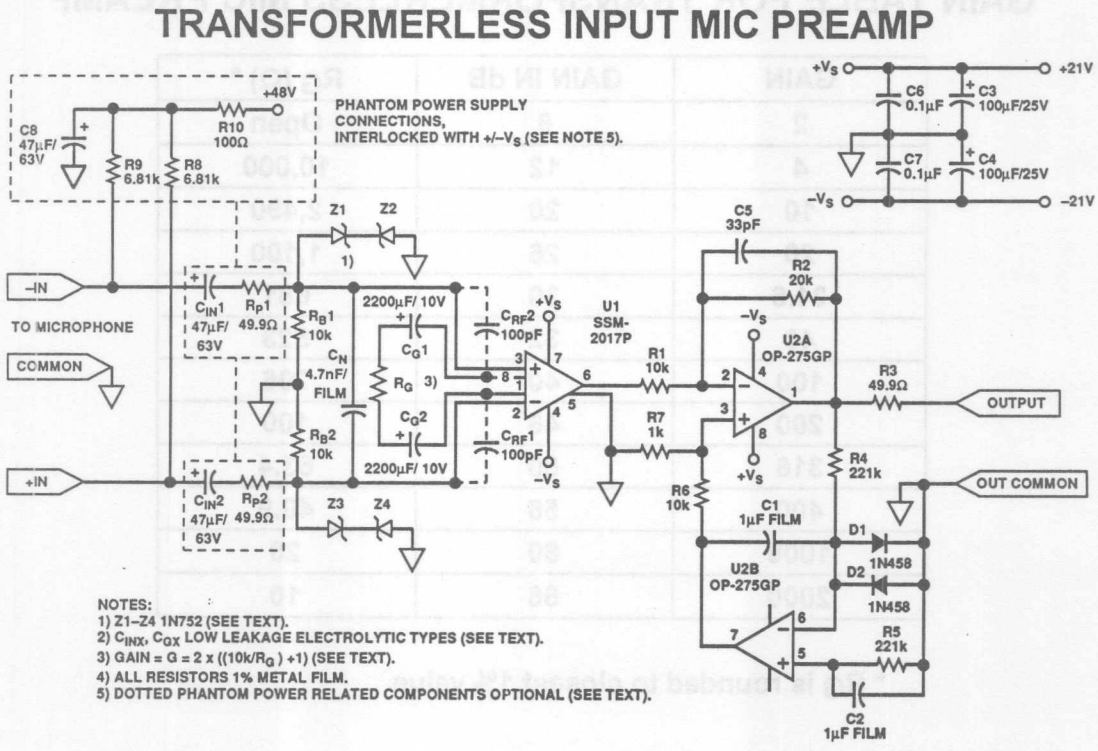


Figure 8.9

The SSM-2017 IC preamp is suitable for use in transformerless mic preamps, with an input noise of less than 1nV√Hz, high CM rejection and low distortion. Gain of this 8 pin IC is set by one external resistor, "R_g", and is adjustable over a range of 1-1000 (0 to 60dB). Differential inputs at pins 2-3 allow balanced input signals, with a single- ended output signal developed between the output (6) and reference (5) pins.

The SSM-2017 is used here in a gain-programmable input stage, which then drives a fixed gain of 2 OP- 275 high current output buffer and DC servo. The buffer provides low distortion drive

into 600Ω loads, with the second half of U2 used as a servo, for low output DC offset (≤ 2mV).

In the U1 stage, gain is set by resistance R_g. Combined with the gain of two in the U2 stage, the overall preamp numeric gain "G" is:

$$G = 2\left[\frac{10{,}000\Omega}{R_g} + 1\right] \qquad \text{Eq. 8.4}$$

R_g can be either a reverse log pot, or a switch controlled resistance used as a gain control for the entire circuit. The R_g value for a given gain G is:

$$R_g = \frac{20{,}000\Omega}{G-2} \qquad \text{Eq. 8.5}$$

Figure 8.10 gives R_g values for various gains, using the closest standard 1% resistor values.

GAIN TABLE FOR TRANSFORMERLESS MIC PREAMP

GAIN	GAIN IN dB	RG (Ω) *
2	6	Open
4	12	10,000
10	20	2,490
20	26	1,100
31.6	30	681
40	32	523
100	40	205
200	46	100
316	50	63.4
400	56	49.9
1000	60	20
2000	66	10

* RG is rounded to closest 1% value

Figure 8.10

Another important requirement for transformerless preamps is that they must be immune to transient damage related to phantom power supplies. With the use of microphone phantom powering, 48V DC power is fed CM to a remote mic capsule, while the balanced audio signal received back from the mic must be amplified cleanly with no side effects from the DC. For steady state conditions this is simple, but switching transients from the DC power can kill an amplifier input stage if it is not protected. Transformerless mic preamps must be protected against power surges, yet must also operate with best performance.

Normally coupling capacitors C_{in1} and C_{in2} decouple the phantom power DC level, passing the balanced audio signal to U1. But, when the phantom power is switched on/off, or the mic cable is plugged in/out, potentially destructive transients of up to ±48V are coupled through C_{in1} and C_{in2}, and appear across R_{b1} and/or R_{b2}. If these transients are not safely dissipated, they can cause destruction of U1. This applies to *virtually any amplifier input stage, not just the SSM-2017*, since energy stored in the coupling capacitors can develop peak discharge currents of several amperes.

Here CM voltage limiting is used on each of the differential input lines, with pairs of back-to-back low voltage zeners, Z1-Z2 and Z3-Z4, standard 400mW, Vz=5.1V units from the 1N750 series. Peak current limiting for transient discharge is provided by the protection resistors R_{p1} and R_{p2}.

This preamp can be operated with or without phantom power, so it is logical to optimize input connections so that those portions of the circuit not essential for phantom power are not in the signal path and the 48V DC power being switched off when phantom power is not in use. When phantom power is used, the 48V supply should be interlocked with the bipolar power supply of the amplifier to prevent switching on phantom power with the amplifier circuitry off.

Another source of problems with high gain preamps is radio frequency interference (RFI). Input capacitor C_n filters frequencies above 135kHz before they reach the preamp input. In addition, further filtering is provided in the second stage by R_2-C_5, at 241kHz.

Additional RFI filtering can use several methods. Separate low resistance inline RF chokes or a single common mode choke can be used in series with the two inputs. RF bypassing of the SSM-2017 input transistors can also be used, from pins 1-2 and 3-8 (shown on the schematic as $C_{rf}1/C_{rf}2$).

This amplifier's performance is quite good over gain ranges of 6-66dB (2/1 to 2000/1). For a typical audio load of 600Ω, THD+N at various gains and an output level of 10Vrms is consistent and well below 0.01%, for all but the highest gains, where it becomes more limited by noise, as shown in Figure 8.11. Noise performance is quite good, at an operating gain of 1000 it is equivalent to 1nV/√Hz referred to the preamp input. Maximum output is a function of the power supplies, and can be as high as 10Vrms. Note that output resistor R_3 limits available swing driving 600Ω, but should be retained for short circuit protection. Supply voltages on the order of ±20V are appropriate for highest output into 600Ω, but the circuit can also be operated on lower supply voltages with lower maximum output.

THD + N PERFORMANCE OF TRANSFORMERLESS MIC PREAMP VERSUS GAIN FOR V_{out} = 10V rms, R_L = 600Ω

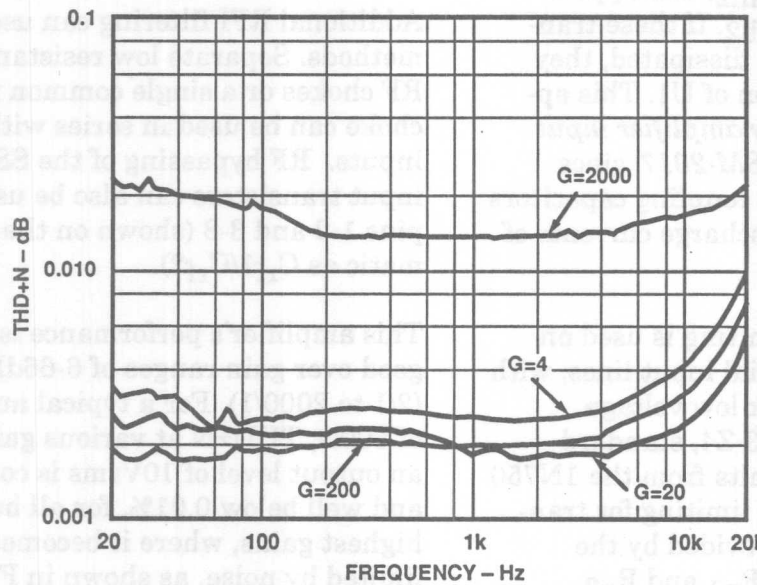


Figure 8.11

The SSM-2017 device architecture is basically similar to family predecessors SSM-2015 and SSM-2016, but without access to the internal gain resistors (because of the 8 pin package). Both the SSM-2015 and SSM-2016 can be applied in circuits similar to Figure 8.9 with phantom powering, and have virtues in their own right. For example, the SSM-2016 can use supplies of up to ±36V, and has a high current output stage (±40mA minimum). This enables it to drive low impedance audio loads to high levels.

REFERENCES: MICROPHONE PREAMPLIFIERS

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3. "ANSI Standard 268-15 (Revision 1987, amendments 1989, 1990, 1991)". American National Standards Institute, 11 W. 42nd St., New York, NY, 10036.

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5. W. Jung, M. Stephens, C. Todd, "Slewing Induced Distortion & Its Effect on Audio Amplifier Performance— With Correlated Measurement/Listening Results", presented at 57th AES convention, May 1977, AES preprint # 1252.

6. W. Jung, M. Stephens, C. Todd, "An Overview of SID and TIM", Parts 1-3, **Audio**, June, July, August, 1979.

7. Walt Jung, **Audio IC Op Amp Applications, 3d Ed.**, Howard W. Sams, 1987.

8. W. Jung, A. Garcia, "A Low Noise Microphone Preamp with a Phantom Power Option", Analog Devices AN-242, November 1992.

9. W. Hoge, "Build a Microphone Preamp", **Audio**, February 1979.

RIAA PHONO PREAMPLIFIERS

An example of an audio range preamplifier application requiring equalized frequency response is the RIAA phono preamp. While present day LP record sales are quickly fading with the establishment of new digital media, for completeness equipment will still be designed to include phono playback stages for some time. RIAA preamp stages, as amplifiers with predictable non-flat frequency response, have more general application connotations. The design techniques within this section are specific to RIAA as an example, but are applicable to other frequency dependent amplitude designs in general.

The techniques are also useful as a study tool, considering the various approaches which have been advanced to optimize the function of high performance gain with predictable equalization (EQ). These last two points make these discussions useful in a much broader sense.

RIAA Basics

The RIAA equalization curve[1] is shown in Figure 8.12, expressed relative to DC. This curve indicates maximum gain below 50 Hz (f1), with two high-frequency inflection points. Above f1, the gain rolls off at 6 dB/octave until a first high-frequency breakpoint is reached at 500 Hz (f2). Gain then remains relatively constant until a second high-frequency breakpoint is reached at 2.1 kHz (f3), where it again rolls off at 6 dB/octave through the remainder of the audio region and above.

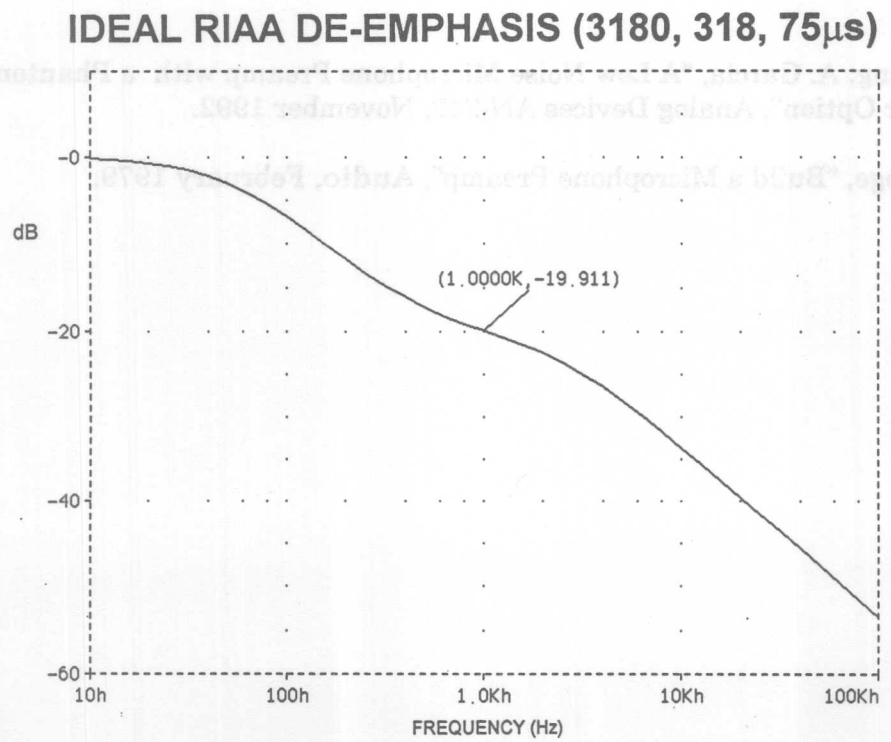


Figure 8.12

Use of a low frequency rolloff (f0, not shown) is at the option of the designer. It can be extended towards DC, or, alternately, rolled off at a low frequency below 50 Hz. When applied, this roll off is popularly called a "rumble" filter, since it reduces turntable/record related low-frequency disturbances and lessens the possibility of system and low-frequency driver overload. This rolloff may or may not coincide with a fourth time constant.

However, gain at the frequencies f1, f2, and f3 describes the basic RIAA curve. This curve is also described in terms of three corresponding time constants, T1, T2, and T3, defined as 3180μs, 318μs, and 75μs, respectively.[1] (Note: T1-T3 are here described as they correspond to ascending frequency, or the reverse of the terminology in [1]. The time constants themselves are identical, however). An IEC amendment to the basic RIAA response adds a fourth time constant of 7950μs, corresponding to an f0 of 20Hz when used.[2] Use of this rolloff has never been standardized in the US, and is not treated in great detail here.

The characteristic gain in dB for an RIAA preamp is generally specified relative to a 1kHz reference frequency. From Figure 8.13, a complete 10-100kHz relative decibel table for the three basic RIAA time constants, the 1kHz gain is 19.91dB below the DC gain (column 3). Expressed in terms of a gain ratio, this means the ideal 1kHz RIAA preamp gain is 0.101 times the DC gain. This constant 0.101 is unique to all RIAA preamp designs following the above curve, therefore it can be designated as "K_{RIAA}", or:

$$K_{RIAA} = 0.101 \qquad \text{Eq. 8.6}$$

This constant logically shows up in various gain expressions of the RIAA preamp designs which follow. Since the shape of the standard RIAA curve is fixed, specifying gain for a given frequency (1kHz) defines the gain for all other frequencies. For convenience, Figure 8.13 shows gains relative to 1kHz (column 2), and to DC (column 3).

IDEALIZED RIAA FREQUENCY RESPONSE

FREQ	VDB(6)(1)	VDB(5)(2)
1.000E+01	1.974E+01	-1.684E-01
1.259E+01	1.965E+01	-2.639E-01
1.585E+01	1.950E+01	-4.109E-01
1.995E+01	1.928E+01	-6.341E-01
2.512E+01	1.895E+01	-9.654E-01
3.162E+01	1.847E+01	-1.443E+00
3.981E+01	1.781E+01	-2.103E+00
5.012E+01	1.694E+01	-2.975E+00
6.310E+01	1.584E+01	-4.067E+00
7.943E+01	1.455E+01	-5.362E+00
1.000E+02	1.309E+01	-6.823E+00
1.259E+02	1.151E+01	-8.398E+00
1.585E+02	9.877E+00	-1.003E+01
1.995E+02	8.236E+00	-1.167E+01
2.512E+02	6.645E+00	-1.327E+01
3.162E+02	5.155E+00	-1.476E+01
3.981E+02	3.810E+00	-1.610E+01
5.012E+02	2.636E+00	-1.727E+01
6.310E+02	1.636E+00	-1.828E+01
7.943E+02	7.763E-01	-1.913E+01
1.000E+03	**8.338E-07**	**-1.991E+01**
1.259E+03	-7.682E-01	-2.068E+01
1.585E+03	-1.606E+00	-2.152E+01
1.995E+03	-2.578E+00	-2.249E+01
2.512E+03	-3.726E+00	-2.364E+01
3.162E+03	-5.062E+00	-2.497E+01
3.981E+03	-6.572E+00	-2.648E+01
5.012E+03	-8.227E+00	-2.814E+01
6.310E+03	-9.992E+00	-2.990E+01
7.943E+03	-1.184E+01	-3.175E+01
1.000E+04	-1.373E+01	-3.365E+01
1.259E+04	-1.567E+01	-3.558E+01
1.585E+04	-1.763E+01	-3.754E+01
1.995E+04	-1.960E+01	-3.951E+01
2.512E+04	-2.158E+01	-4.149E+01
3.162E+04	-2.357E+01	-4.348E+01
3.981E+04	-2.557E+01	-4.548E+01
5.012E+04	-2.756E+01	-4.747E+01
6.310E+04	-2.956E+01	-4.947E+01
7.943E+04	-3.156E+01	-5.147E+01
1.000E+05	-3.356E+01	-5.347E+01

Notes:

(1) denotes 1kHz 0dB reference

(2) denotes DC 0dB reference

Figure 8.13

It can also be seen from the RIAA curve of Figure 8.12 that the gain characteristic continues to fall at high frequencies. This implies that an amplifier with unity-gain stability for 100% feedback is required, which can indeed be true, if a standard feedback configuration is used. There are many circuit approaches which can be used to accomplish RIAA phono-playback equalization, but all must satisfy the general frequency response characteristic of Figure 8.12.

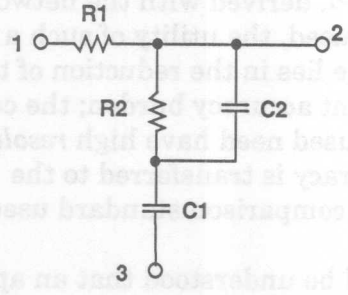
Equalization Networks for RIAA Equalizers

Two EQ networks well suited in practice to RIAA phono reproduction are illustrated in Figure 8.14a and 8.14b, networks N1 and N2. Both networks with values as listed can yield with high accuracy the three standard RIAA time constants of 3180, 318, and 75μs as outlined by network theory.[3,4,5,6]

For convenience, both theoretical values for the ideal individual time constants are shown (left), as well as closest fit standard "no trim" values (right). Designers can of course, parallel and/or series such R and C values as may be deemed appropriate or practical, adhering to network theory.

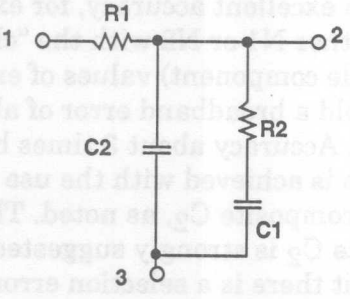
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RIAA NETWORKS (T1 = 3180μs, T2 = 318μs, T3 = 75μs)



A: "N1" NETWORK

THEORETICAL	CLOSEST FIT
R1 = 9.79kΩ	R1 = 9.76kΩ
R2 = 789.3Ω	R2 = 787Ω
C1 = 0.3μF	C1 = 0.3μF (BASE)
C2 = 0.1029μF	C2 = 0.1μF +3nF



B: "N2" NETWORK

THEORETICAL	CLOSEST FIT
R1 = 7.290kΩ	R1 = 7.32kΩ
R2 =1.06kΩ	R2 =1.05kΩ
C1 = 0.3μF	C1 = 0.3μF (BASE)
C2 = 0.1029μF	C2 = 0.1μF +3nF

Figure 8.14

Of course there are an infinite set of possible RC combinations from which to choose network values, but practicality should rule any final selection. A theoretical starting point for a network value selection can begin with *any* component, but in practice the much smaller range of available capacitors suggests their selection first, then resistors, from their much broader span of (stock) values. Note that precision film resistors can in fact be obtained (on special order) in virtually *any* value, up to several megohms. The values listed here are those taken as standard from the E96 series.

Very high standards of EQ accuracy are possible, to tolerances of noticeably better than ±0.1dB (see for example data from[8] also quoted in [6]). In the design process however, there are several distinct general aspects of EQ component selection which can affect the ultimate accuracy. These are worth reviewing before embarking on a design.

■ The *selection tolerance* of the component defines how far an ideal (zero manufacturing tolerance) component deviates from the theoretical value. A good design will seek to minimize this error by using either carefully selected standard values, or series and/or shunt combinations, so as to achieve selection tolerance of less than 1%, preferably zero.

■ The *manufacturing tolerance* of the component defines how far an otherwise ideal component deviates from its stated catalog value, such as ±1, ±2%, etc. This can obviously be controlled by tighter specifications, but usually at some premium, particularly with capacitors of ±1% or less. Note that a "hidden" premium here can be long delivery times for certain values. Care should be taken to use standard stock values with capacitors— even to the extent that multiple standard values may be preferable (3 times 0.1μF for 0.3μF, for example).

■ *Topology-related parasitics* must also be given attention, as they can also potentially wreck accuracy. Amplifier gain-bandwidth is one possible source of parasitic EQ error. However, a more likely error source is the parasitic zero associated with active feedback equalizers. If left uncompensated below 100kHz, this alone can be a serious error.

In any event, for high equalization accuracy to be "real", once a basic solid design is selected the designer must provide for the qualification of components used, by precise measurement and screening, or tight purchase tolerances. An alternative is iterative trimming against a reference standard such as [9], but this is not likely to be attractive for production. An example is the data of [8], derived with the network of.[9] If used, the utility of such a trim technique lies in the reduction of the equipment accuracy burden; the comparator used need have high *resolution*, but accuracy is transferred to the network comparison standard used.

It should be understood that an appropriately selected high quality network will yield excellent accuracy, for example either N1 or N2 with the "closest fit" (single component) values of exact value yield a broadband error of about ±0.15dB. Accuracy about 3 times better than this is achieved with the use of N1 and the composite C_2, as noted. The composite C_2 is strongly suggested, as without it there is a selection error of about 3%.

It is strongly recommended that only the highest quality components be employed in these networks.

Regardless of the quality of the remainder of the circuit, it is evident that the equalization accuracy and fidelity can be no better than the quality of these components used to define the transfer function. Thus only the best available components should be used in the N1 (or N2) RC network, selected as follows:

■ *Capacitors*— should have close initial tolerance (1-2%), a low dissipation factor and low dielectric absorption, be non-inductive in construction, and have stably terminated low-loss leads. These criteria in general are best met by capacitors of the Teflon, polypropylene and polystyrene film families, with 1-2% polypropylene types being preferred as the most practical.[10,11,12] Types which should be avoided are the "high K" ceramic families, while in contrast, "low K" ceramic types, such as "NP0" or "COG" dielectrics, have excellent dissipation factors. While not recommended as readily as the best film types (their DA is not as well controlled as the best films), they may be worth consideration for small values and/or where space is at a premium.

■ *Resistors*— should also be close tolerance (≤1%), have low non-linearity (low voltage coefficient), be temperature stable, with solid stable terminations and low-loss non-inductive leads. Types which meet these criteria best are the bulk metal foil types and selected thick films, or selected military grade RN55 or RN60 style metal film resistor types.[13]

The specific component values suggested may not be optimum from a low impedance and low noise standpoint, but the practical realities for general use will most likely deter the use of appreciably lower ones. For example, one could reduce the input resistance of either network to 1kΩ, and thus lower the input referred noise contribution of the network. But this in turn would necessitate greater drive capability from the amplifier stage, and raise the C values to 1-3μF, where they are large, expensive, and very difficult to obtain. This may be justified for some uses, where performance is the guiding criterion rather than cost effectiveness, or the amplifiers used sufficiently low in noise to justify such a step. Regardless of the absolute level of impedance used, the components should be adequately shielded against noise pickup, with the outside foils of C_1 or C_2 connected to common.

These same N1/N2 networks can suffice for both active and passive type equalization. Active (feedback) equalizers use the network simply by returning the input resistor (R_1) to common, that is jumpering points 1-3, and employing the network as a two-terminal impedance between points 1+3, and 2. Passive equalizers use the same network in a three terminal mode, interstaged between two wideband gain blocks.

8

RIAA Equalizer Topologies

There are of course many different circuit topologies which can be used to realize an RIAA equalizer, and three possible ones are illustrated in fundamental form in Figures 8.15 through 8.17 of this section. Dependent upon the type of phono cartridge to be used, the 1kHz gain of the preamp can range from 30-70dB.

Magnetic phono cartridges in popular use consist of two basic types: moving

magnet and moving coil. The moving magnet types, which are the most familiar, are suitable for the first circuits to be described. The moving coil cartridge types are higher performance devices; they are less commonplace but still highly popular.

Functionally, both types of magnetic cartridges perform similarly, and both must be equalized for flat response in accordance with the RIAA characteristic. A big difference in application, however, is the fact that moving magnet types have typical sensitivities of about 1 mV of output for each cm/s of recorded velocity. In moving coil types, a sensitivity on the order of 0.1 mV is more common (for a similar velocity). In application then, a moving coil RIAA preamp must have more gain than a moving magnet preamp. Typical overall (1 kHz) gains are 60-70 dB for moving coils and 30-40 dB for moving magnets. Noise performance of a moving coil preamp becomes critical, however, because of low-output voltage and low impedance involved—typically 3-40 ohms. The following circuits illustrate techniques that are useful in meeting these requirements.

Actively Equalized RIAA Preamp Topology

The most familiar topology is shown in Figure 8.15, and is called an active feedback equalizer, because the network N used to accomplish the EQ is part of an active feedback path.[10,14] In these and the following discussions it is assumed that the input from the pickup is appropriately terminated by R_t-C_t, which are selected for flat response. The following discussions deal with the frequency response of the amplifier, given this ideal input signal.

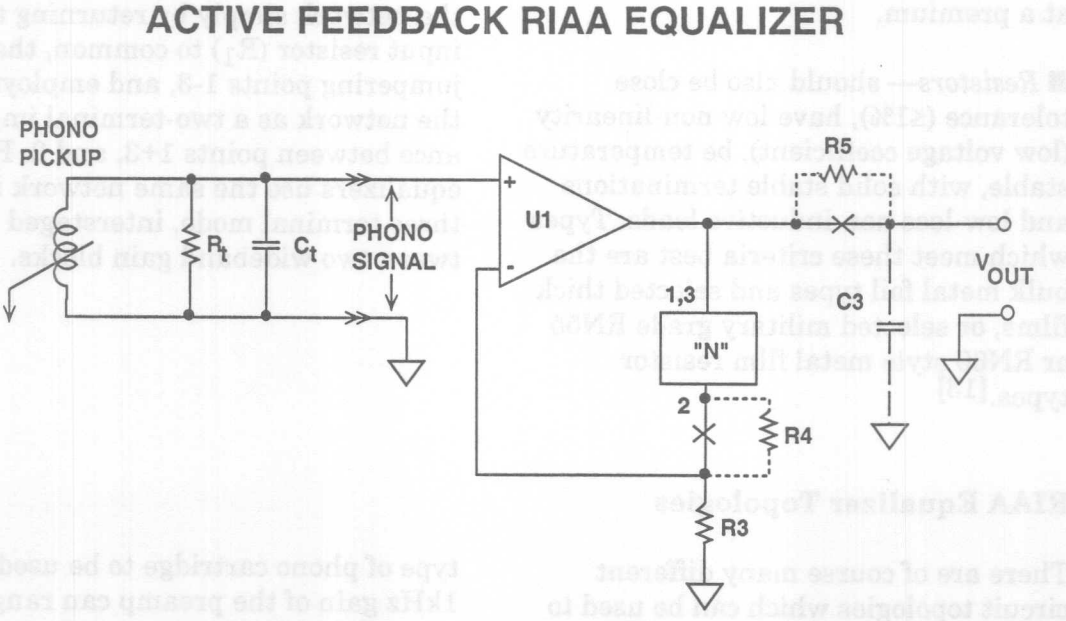


Figure 8.15

Assuming a sufficiently high gain amplifier for U1, the gain/frequency characteristics of this circuit are determined by the network. Gain of the stage is set by R_3, and the output is available at a low impedance, V_{OUT}. The gain of this stage at 1kHz is defined by the RIAA curve and resistors R_1 and R_3 (where R_1 is part of network N1), and is:

$$G_{(1kHz)} = 0.101\left(1 + \frac{R_1}{R_3}\right) \qquad \text{Eq. 8.7}$$

where 0.101 is the RIAA constant, K_{RIAA}.

An ideal RIAA response falls with increasing frequency, and will be less than unity at some high frequency. The basic topology of Figure 8.15 cannot achieve this, as the minimum gain approaches unity at some (high) parasitic zero frequency, where the network equivalent series capacitive impedance becomes equal to R_3.

However, the practical consequence of this may or may not be of significance, depending upon where the zero frequency falls. If this is well above audibility (≥ 100kHz), it will introduce some equalization error at the upper end of the audio range, but this may be small. If this frequency is as low as 100kHz, the (uncorrected) error at 20kHz is about 0.3dB.

Fortunately, this error can be exactly compensated by a passive low-pass filter after the amplifier, R_5-C_3. The time constant of this filter is set to match the time constant of the zero, T4, which is:

$$T4 = R_3 \times C_{EQUIV} \qquad \text{Eq. 8.8}$$

where R_3 is a value required for gain in the specific design, and C_{EQUIV} is the series equivalent capacitance of network capacitors C_1/C_2, or:

$$C_{EQUIV} = \frac{C_1 C_2}{C_1 + C_2} \qquad \text{Eq. 8.9}$$

For example, if C_{EQUIV} of network N1 is 7.6nF and $R_3 = 200\Omega$, the required R_5-C_3 time constant is T = 1.5µs, which can be compensated with $R_5 = 499\Omega$ and C_3 = 3nF. Note that this design step increases the output impedance of the circuit, making it more susceptible to load variations. Therefore this measure should be weighed against the added parts complexity and the loading tradeoffs.

In some designs, a resistor R_4 (dotted) may be used in series with N (for example, for purposes of amplifier stability at a gain higher than unity). With R_4 present, time constant T4 is calculated as:

$$T4 = (R_3 + R_4) \times C_{EQUIV} \qquad \text{Eq. 8.10}$$

and the R_5-C_3 product is then chosen to be equal to this T4.

Passively Equalized RIAA Preamp Topology

Another design approach is a so-called passively equalized preamp.[10] A basic circuit which can be used for such RIAA phono applications is shown in Figure 8.16. This consists of two high quality wideband gain blocks, U1 and U2, separated by a three terminal network, "N" (either network N1 or N2).

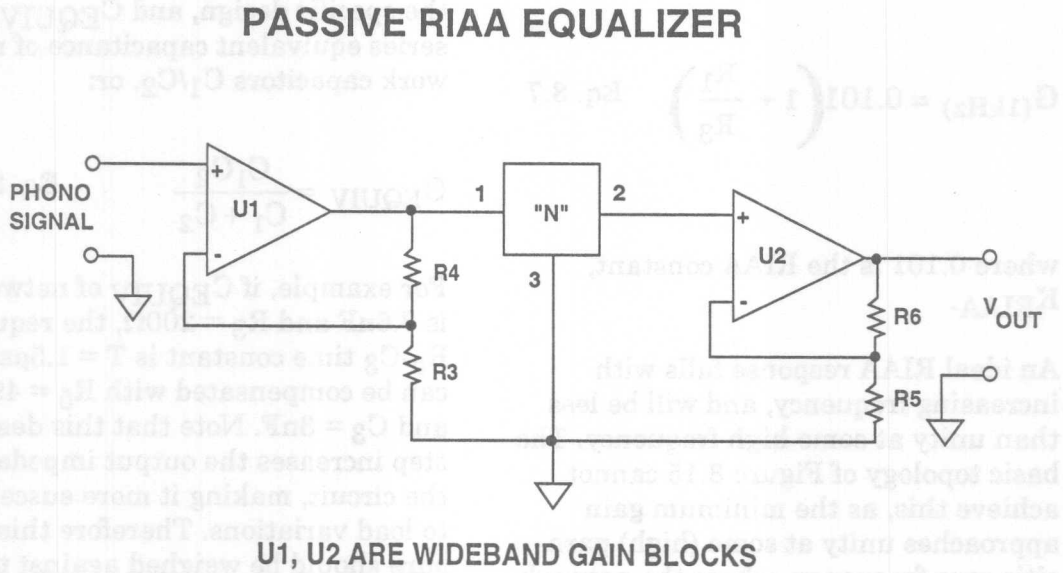


Figure 8.16

The gain stages are set up for the required total gain, with R_4-R_3 and R_6-R_5. In general, the 1kHz gain of this circuit is:

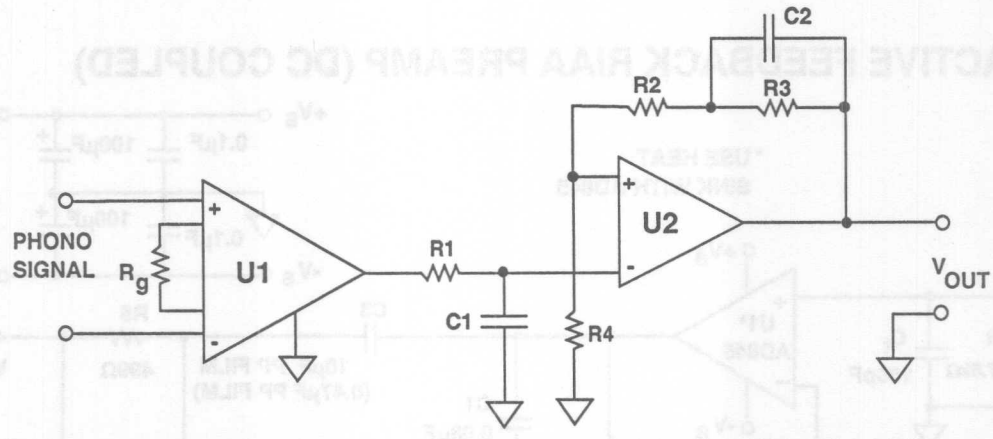
$$G_{(1kHz)} = 0.101\left(1 + \frac{R_4}{R_3}\right)\left(1 + \frac{R_6}{R_5}\right) \qquad \text{Eq. 8.11}$$

The op-amp gain blocks could be made identical for purposes of simplicity but are not necessarily. A preamplifier topology such as this must be optimized for signal-handling capability, both from an overload standpoint and for low noise. Stage U1 is chosen for a gain sufficiently high that the input-referred noise will mostly be due to this stage and the cartridge, but yet not so high that it will clip at high-level high-frequency inputs. Amplifiers with a 10V rms output capability (±18V supplies) allow U1 to accept ≈400 mVrms with a gain of 25 at high frequencies.

Hybrid Equalized RIAA Preamp Topology

By using a combination of passive/active or "hybrid" equalization, the noise/overload constraints of the totally passive equalization is lessened.[15] In addition, "hybrid" equalization can use either an instrumentation or an op amp input stage for best noise performance (Figure 8.17).

HYBRID (PASSIVE AND ACTIVE FEEDBACK) RIAA EQUALIZER



- U1, U2 ARE WIDEBAND GAIN BLOCKS
- U1 CAN BE AN INSTRUMENTATION AMP OR AN OP AMP

$T_1 = R3 \cdot C2 = 3180\mu s$

$T_2 = \frac{R3 \cdot C2\ (R2+R4)}{R2+R3+R4} = 318\mu s$

$T_3 = R1 \cdot C1 = 75\mu s$

Figure 8.17

Here U1 is shown as a differential input amplifier, which accepts a balanced signal from the phono cartridge, and amplifies it by a wideband gain of $G_{(U1)}$ (which is the gain of the device used for U1). Overall, the gain of this entire circuit is the product of the U1-U2 stage gains, as modified by the RIAA frequency response. At 1kHz, the gain is:

$$G_{(1kHz)} = 0.101\left[G_{(U1)}\right]\left(1 + \frac{R_2 + R_3 + R_4}{R_4}\right) \quad \text{Eq. 8.12}$$

Unlike the previous equalizers, the three time constants in this circuit are not set by a single network, but by the relationships shown in the Figure 8.17. This has the advantage of less interaction, and noise performance can be optimized by using less gain in stage U2. The gain of stage U1 in this circuit ($G_{(U1)}$) is used to adjust overall gain, whether U1 is an in- amp, or a conventional op amp stage.

Active Feedback RIAA Phono Preamp

Figures 8.18 and 8.20 illustrate two variants of the most popular approach to achieving a simple RIAA phono preamp using active feedback. Figure 8.18 is a high-performance DC coupled version using the recommended precision components. Amplifier U1 provides the gain, and equalization components R_1-R_2-C_1-C_2 form the RIAA network, providing a very accurate realization with standard component values. (The network used here is N1 of Figure 8.14a, with terminals 1 and 3 common and values scaled 10x).

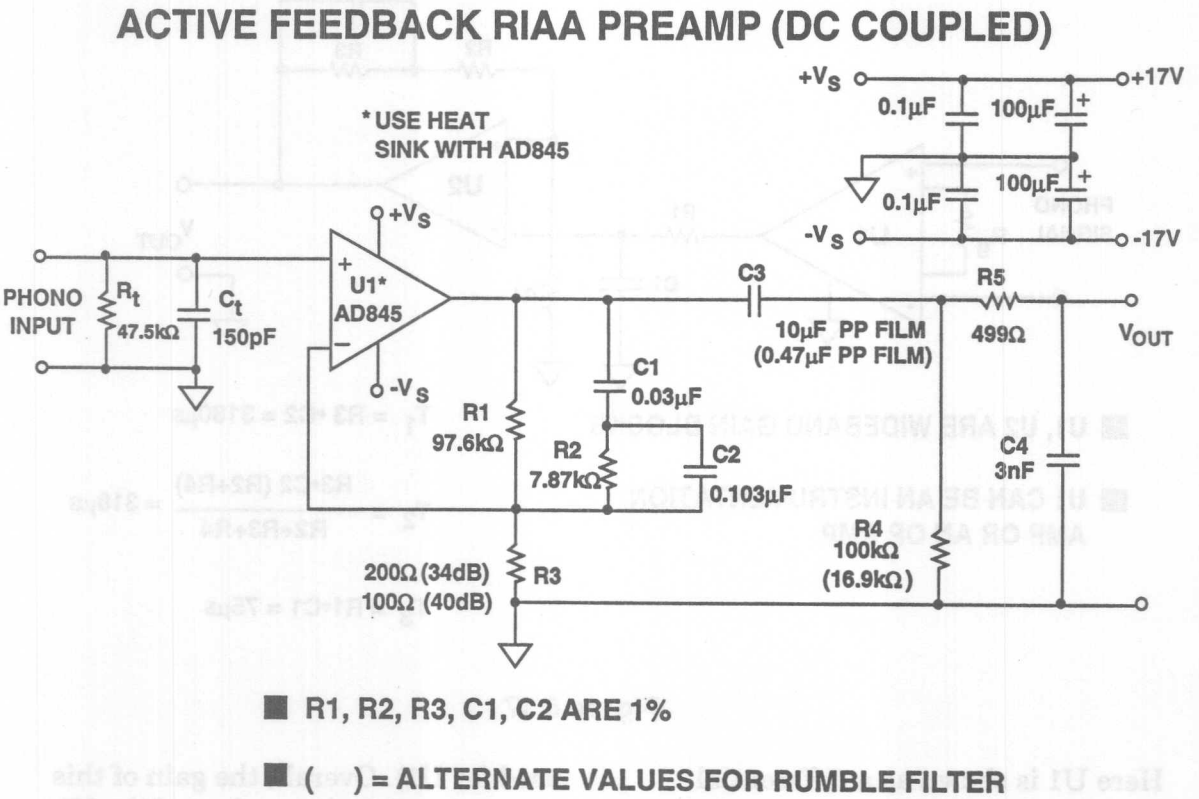


Figure 8.18

The actual network components should be 1% precision high-quality types, both for initial equalization accuracy and also for minimal errors from parasitic properties. High-quality metal-film resistors and film capacitors of polystyrene or polypropylene are recommended.

The input RC components, R_t-C_t, terminate the moving magnet cartridge with values recommended by the manufacturer. The values shown are typical, with C_t variable for flattest response. Note that these comments apply generally to all the RIAA circuits that follow.

The amplifier parameters required for optimum performance of this circuit are demanding. For lowest noise from the cartridge's inductive source, the amplifier should have a voltage noise density of 5 nV/√Hz or less, and a current noise density of 1 pA/√Hz or less. The former requirement is best met by using low-noise bipolar-input amplifiers, such as the OP-27, OP-270, OP-275, and SSM-2134 or 5532/5534 types. The latter need is best met by the use of FET-input amplifiers in general.

For bipolar-input amplifiers, DC input-bias current can be a potential problem when direct coupling to the cartridge, so in this directly coupled circuit an op amp with a low input bias current amplifier is suggested. If a bipolar input amplifier is used for U1, it should have an input current of ≤100nA for minimum problems with DC offset (assuming a typical phono cartridge of about 1kΩ resistance). Examples here are the OP- 27, OP-270 and related devices.

FET-input amplifiers generally have negligible bias currents but they also tend to have a higher voltage noise. FET-input types useful for U1 are the AD845 and SSM-2131, even though their voltage noise is not as low as the best of the bipolar devices mentioned. On the positive side, they both have a high output current and slew rate for low distortion when driving the load of the feedback network (which approaches R_3 at high frequencies). Of the two, the SSM-2131 has the lower voltage noise, while the AD845 has higher output current and slew rate.

For high-gain accuracy, particularly at high stage gains, the amplifier should have a high gain-bandwidth product; preferably 5 MHz or more. Because of the 100% feedback through the network at high frequencies, the amplifier used for U1 must be a unity-gain-stable type. To minimize noise from sources other than the amplifier, gain resistor R_3 is set to a relatively low value, and generates a voltage noise that is low in relation to that of the amplifier used.

The 1kHz gain of this circuit can be calculated from Eq. 8.7 above. For the values shown, the gain is just under 50 times (≈34dB). Higher gains are easily accommodated by decreasing R_3, but gains higher than 40dB may show increasing equalization errors, depending upon the gain bandwidth of the amplifier used. For example, R_3 can be 100Ω for a gain of about 100 times (≈40dB) (note that if R_3 is changed for a higher gain, C_4 should also be changed to satisfy Eq. 8.8).

With a suitable amplifier, this circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7V rms (assuming ±15V supplies) and higher with the ±17V supplies suggested. RIAA accuracy is quite good using the stock equalization values, and a simulation run is shown in Figure 8.19 for the suggested gain of 34dB. In this expanded scale plot over the 20-20kHz range, the error relative to the 1kHz gain is less than ±0.1dB.

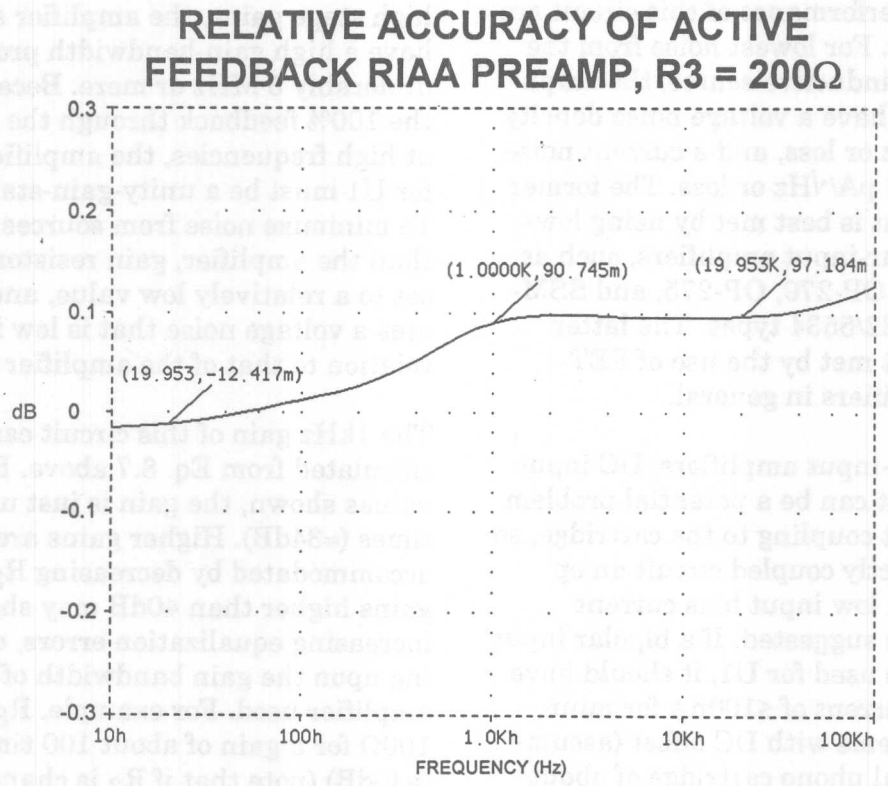


Figure 8.19

For extended low-frequency response, C_3 and R_4 are the larger values shown, with C_3 preferably a polypropylene film type. Alternately, the smaller values for C_3 and R_4 (when applied) form a simple 6dB per octave rumble filter, with a corner at 20Hz. Placing a rumble filter's high-pass action after the preamp stage has the desirable property of discriminating against the RIAA amplified 1/f noise components, in addition to the pickup produced disturbances. C_3 is the only DC blocking capacitor in the circuit. Because the DC gain of the circuit is on the order of 54dB, the amplifier used must be a low offset-voltage device, with an offset voltage that is insensitive to the source. This implies an offset voltage on the order of a few mV, and a low bias current.

Since this is a high-gain low-input-level circuit, the supply voltages should be well regulated and free of noise, and reasonable care should be taken with the shielding and conductor routing.

An alternative AC coupled form of this circuit can be built with higher bias current, low-noise bipolar devices, such as the OP-275 with I_B = 350nA(max), which would otherwise make direct coupling to a cartridge difficult. This form of the circuit is shown in Figure 8.20, and can be used with any unity gain stable bipolar op amp.

ACTIVE FEEDBACK RIAA PREAMP (AC COUPLED)

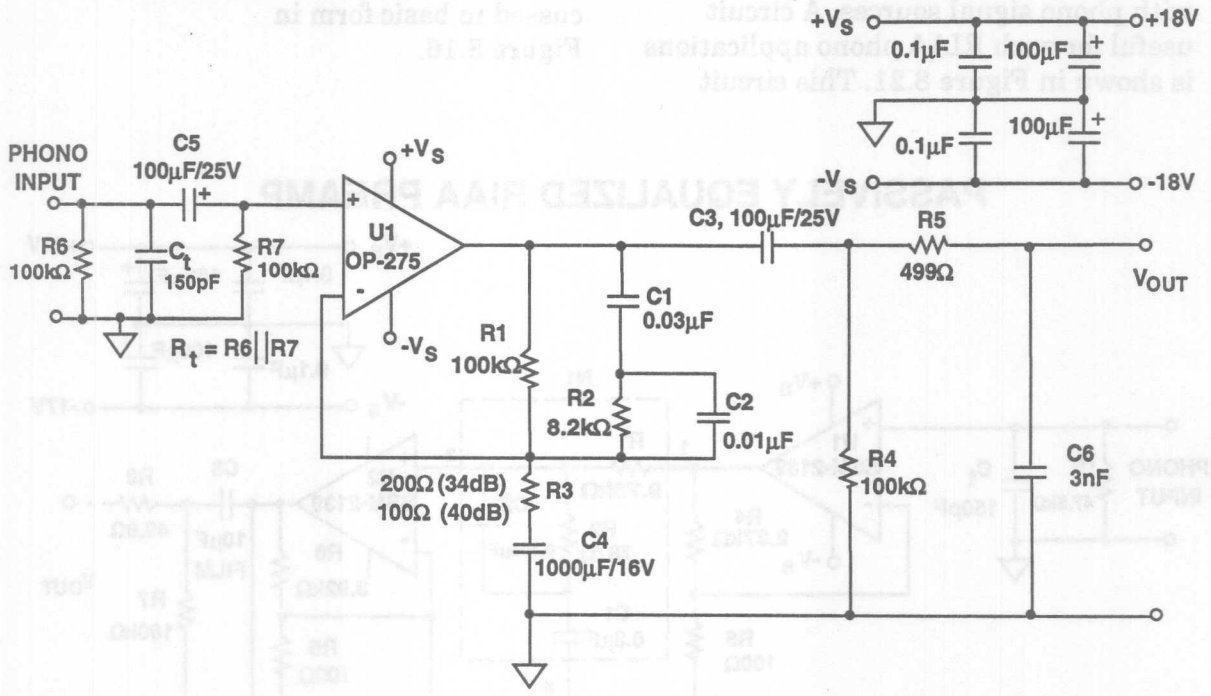


Figure 8.20

Here input AC coupling to U1 is added with C_5, and the cartridge termination resistance R_t is therefore made up of the parallel equivalent of R_6-R_7. R_3 of the feedback network is AC-grounded via C_4, a large value electrolytic. These measures reduce the DC offset at the output of U1 to a few mV. Nearest 5% value units are also used for the network components, making the design both easily reproducible and inexpensive. The output coupling network C_3-R_4 is shown with values suitable for wideband response, but if desired, can be altered to a 7950µs time constant for use as a 20Hz rumble filter. The R_3-C_4 time constant shown provides a corner frequency of ≤1Hz.

The frequency response of this version is not quite as good as that of the circuit in Figure 8.18, but is still within ±0.2dB over 20Hz-20kHz (neglecting the effects of the low frequency rolloff). If tighter response is desired, the N1 values can be used. For the OP-275, supplies can be increased to ±21V if desired, for outputs up to 10Vrms.

Passively Equalized RIAA Phono Preamp

Another area of interest is passively equalized preamplifier circuits used with phono signal sources. A circuit useful for such RIAA phono applications is shown in Figure 8.21. This circuit consists of two high-quality wide bandwidth gain blocks, U1 and U2, as discussed in basic form in Figure 8.16.

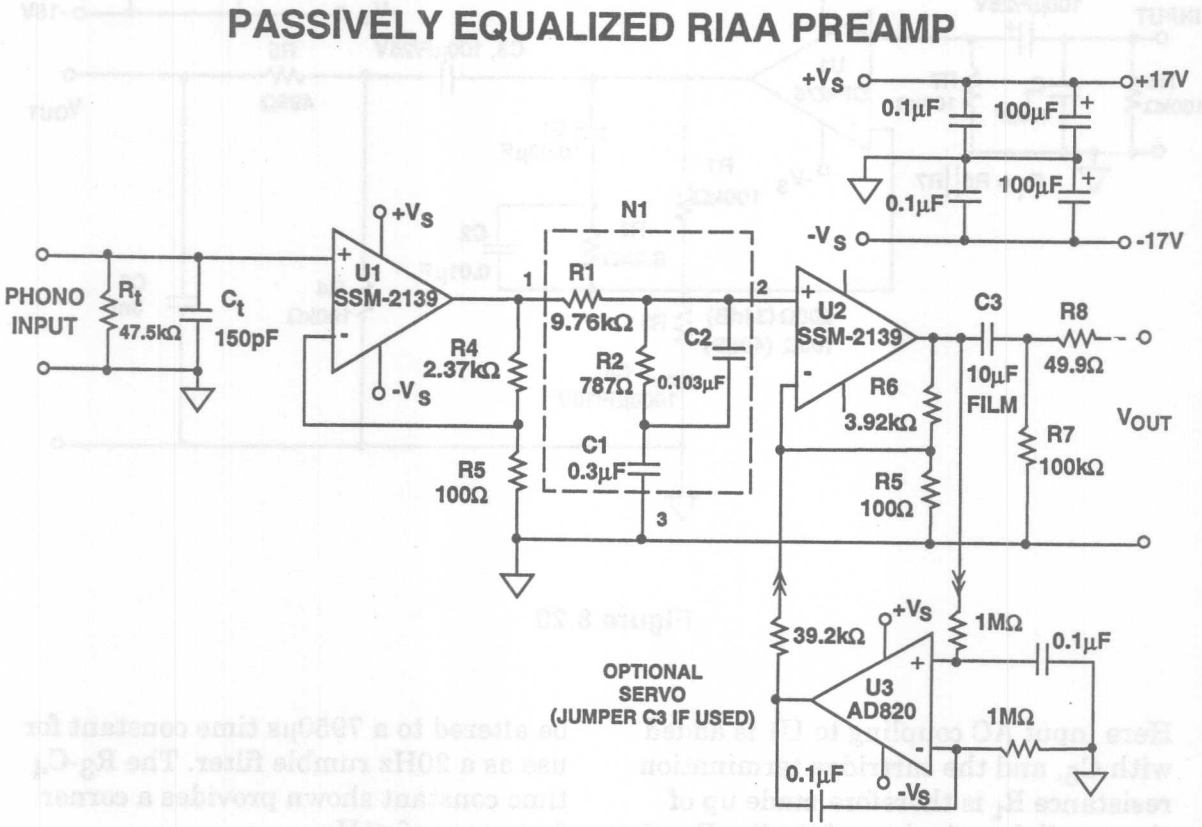


Figure 8.21

The gain of the two blocks are set up by R_4-R_3 and R_6-R_5, as defined in Eq. 8.11. The values shown yield a 1kHz gain that is the product of the U1-U2 stage gains (24.7 times 40.2), times that of the interstage network N. With the 1kHz RIAA gain factor of 0.101, this yields an overall 1kHz gain of 40dB. Other gains can be realized by changes to R_4.

A passively equalized preamplifier such as this one must be carefully optimized for signal handling, both from an overload standpoint and for low noise. Stage U1 is chosen for a gain sufficiently high that the input-referred noise will mostly be due to this stage (and the cartridge, when connected), but yet not so high that it will clip high-level high-frequency inputs. To aid this objective, maximum supply voltage and a high output capability amplifier should be used.

Since U1 operates at a relatively high gain, it need not necessarily be unity gain stable. Decompensated low noise op amps such as the OP-37, SSM-2139, and the FET input AD745 may provide better signal/noise ratio in this application. Other FET-input types, the AD845, the SSM-2131, and OP17 or PM357 types will yield good performance, but with higher noise levels. However, perhaps the best choice is the SSM-2139 dual, which performs both U1 & U2 functions, and has excellent DC specifications.

Gain distribution between U1 and U2 should be LOW/HIGH from an overload standpoint, but HIGH/LOW from a noise standpoint. Practically, these conflicting requirements can be eased by choosing a low noise device for U1, and using the highest possible power supply voltages. There is nearly 40dB loss in the network N at 20 kHz, so output overload of the circuit will be noticed at high frequencies first. With the gain distribution chosen, the circuit allows a 3V rms undistorted output to 20kHz with ±15V supplies, and more with higher supply voltages.

The equalization network N following U1 should use the lowest impedance values practical from the standpoint of low noise, as the noise output at pin 2 of the network is equivalent to the input referred noise of A2. A practical example for this network are the "N1" RC values of R_1-R_2-C_1-C_2 in Figure 8.14a. As noted, scaling can be applied to either network of Figure 8.14 for component selection, as long as the same ratios are maintained. If extremely low noise performance is sought, such as is required for a moving coil preamp, then the N1 values can be reduced further.

Noise in amplifier U2 is less critical than in U1 at low frequencies, but is still not negligible. A low voltage noise device is very valuable for U1 and U2, as is a relatively low input current noise.

U1 should have a low bias current. With 100nA or less bias current, direct coupling to a moving magnet phono cartridge is practical. For example, the maximum 80nA bias current of the SSM-2139 will induce only an 80-160μV input voltage offset at U1 for a typical 1-2kΩ cartridge resistance. Similarly, the bias current induced offset voltage of U2, from the 10kΩ DC resistance of R_1 will be low relative to the amplified offset of U1. As a result, the worst-case overall output DC offset using the SSM-2139 can be held to under 1V for a 40dB gain, allowing the use of a single coupling capacitor, C_3, for DC blocking purposes.

Frequency response of this passively equalized preamp is better than the active version, because there is less interaction with the amplifier(s) compared to the active topology. The frequency response can approach the inherent accuracy of the network components in the audio range, with greater errors at higher frequencies. Figure 8.22 illustrates this point in a simulation of the Figure 8.21 circuit using OP-37 models. Midband error is on the order of ±0.02dB with the N1 network composite values.

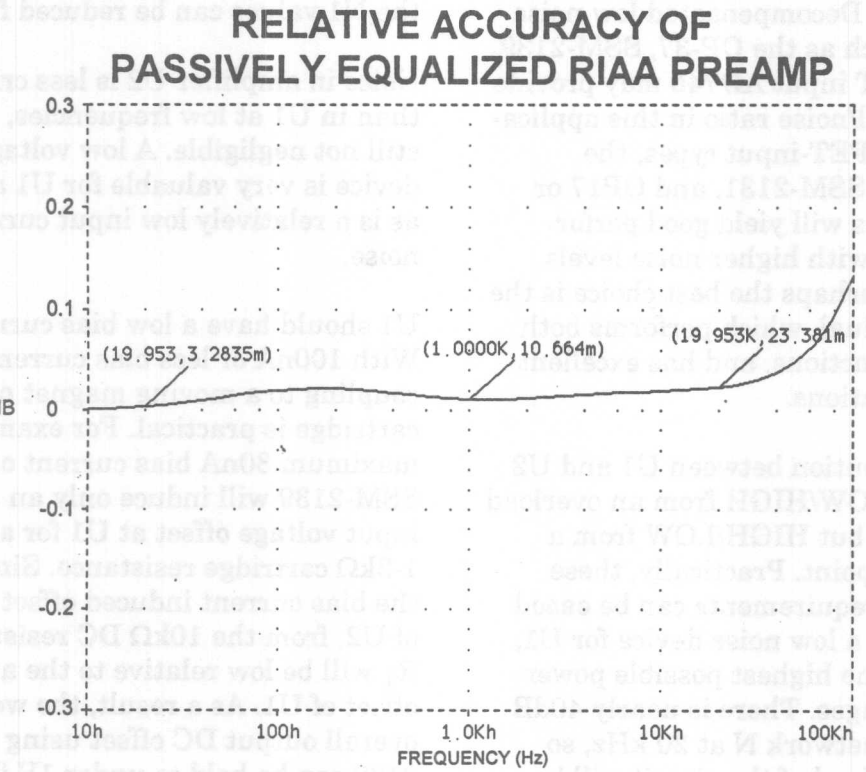


Figure 8.22

This circuit also can be adapted to servo control of the output offset, by replacing C_3 with the optional noninverting servo integrator around stage U2, shown as an option in Figure 8.21.

A general-purpose noninverting servo described in the appendix can be used, along with a low-offset op amp such as the AD820, AD711, OP-97 or AD705.

Hybrid-Equalized Differential-Input, Servo-Controlled, RIAA Phono Preamp

By using a combination of passive and active equalization, some of the noise/overload constraints of totally passive equalization are reduced. In addition, this "hybrid" equalization can be combined with a low-noise differential-input instrumentation amplifier, the AD625, for excellent noise performance and flexibility.

Figure 8.23 shows a hybrid-equalized phono preamp circuit, which has servo control for precise offset and the elimination of coupling capacitors. U1 is the AD625, an in-amp with low voltage noise (4nV/√Hz). It is used as an adjustable differential input amplifier, which accepts a balanced signal from a moving magnet cartridge. Both the DC and AC terminations of the cartridge are split and balanced, with an optional AC trim for best HF CM rejection (C_{tb2}).

HYBRID EQUALIZED RIAA PREAMP

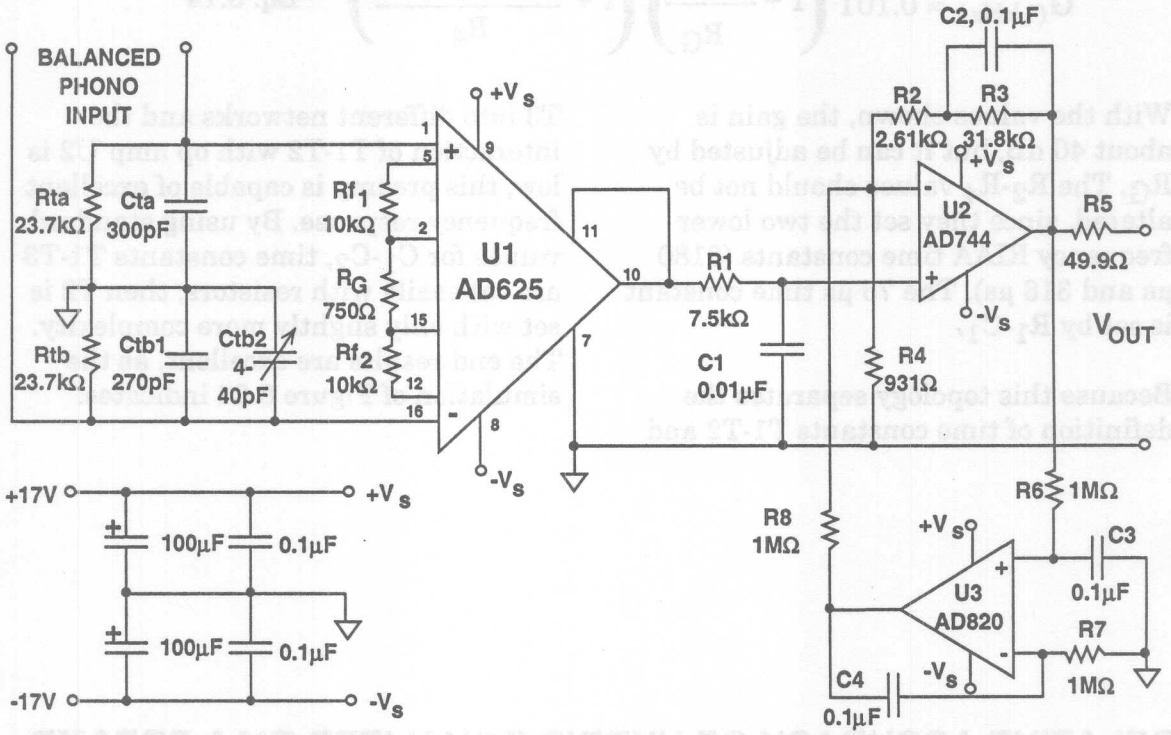


Figure 8.23

The common-mode rejection of U1 below 100 Hz is on the order of 100 dB, a great aid to noise rejection. To minimize noise pickup, a shielded twisted-pair signal cable should be used from the cartridge, with the shield grounded to the common point of R_{ta}-R_{tb} as shown.

The gain of stage U1 in this circuit is:

$$G_{(U1)} = 1 + \frac{2R_F}{R_G} \qquad \text{Eq. 8.13}$$

where $R_{F1} = R_{F2}$, and these resistors and R_G are located at pins 5-2, 2-15, and 15-12 of the AD625. R_{F1} and R_{F2} are matched 10kΩ 1% metal film types. R_G is also a 1% metal-film resistor that is used to adjust overall gain as necessary.

The gain of this entire circuit is the product of the U1 and U2 stage gains, as modified by the RIAA frequency response. At 1kHz, the gain is:

$$G_{(1kHz)} = 0.101\left(1 + \frac{2R_F}{R_G}\right)\left(1 + \frac{R_2 + R_3 + R_4}{R_4}\right) \quad \text{Eq. 8.14}$$

With the values shown, the gain is about 40 dB, but it can be adjusted by R_G. The R_2-R_4 values should not be altered, since they set the two lower frequency RIAA time constants (3180 µs and 318 µs). The 75 µs time constant is set by R_1-C_1.

Because this topology separates the definition of time constants T1-T2 and T3 into different networks and the interaction of T1-T2 with op amp U2 is low, this preamp is capable of excellent frequency response. By using standard values for C_1-C_2, time constants T1-T3 are set easily with resistors; then T2 is set with only slightly more complexity. The end results are excellent, as the simulation of Figure 8.24 indicates.

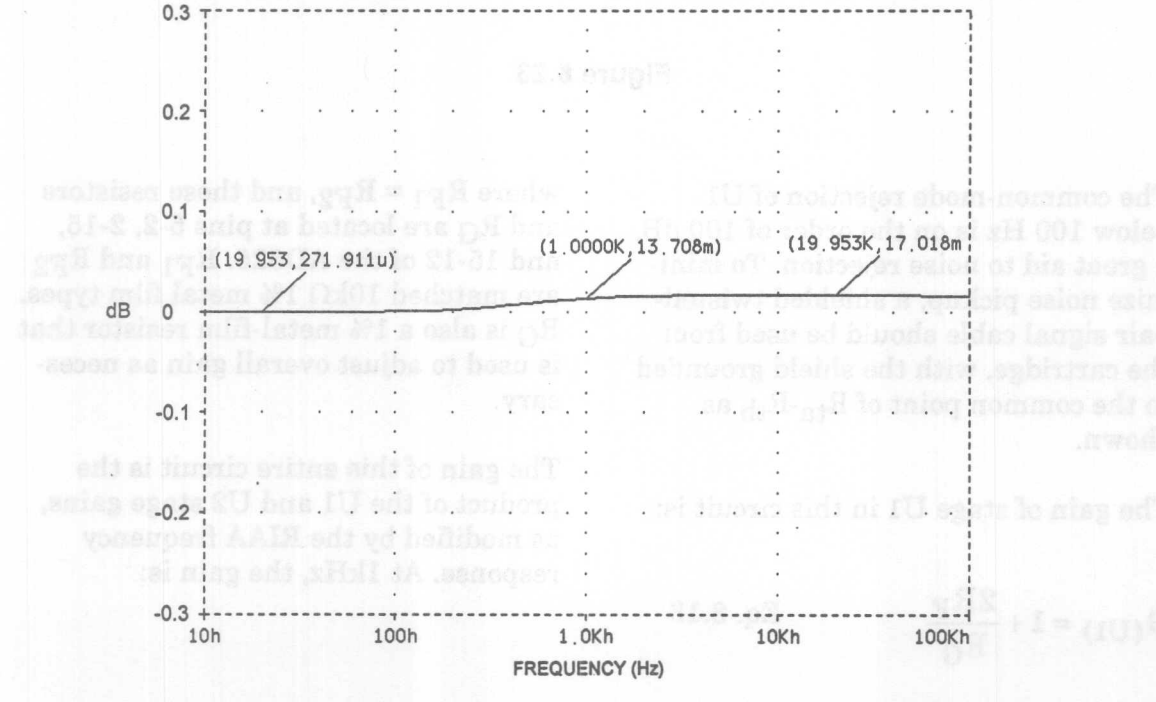


Figure 8.24

Amplifier U3 is a DC servo stage, using an AD820 in a noninverting configuration with an effective 0.3 second time constant. DC feedback for the servo is through the feedback input of stage A2. Note that if any op amp other than the AD820 is used for U3, it is prudent to check if low leakage diodes will be needed as servo anti-latchup clamps across C_3 (discussed in the appendix). The output offset of the circuit will be essentially that of U3, typically less than 1 mV.

Single devices are shown for U2-U3, each optimized for the function. Use of the AD744 for U2 allows very low distortion from this stage, and the AD820 is an effective servo amplifier. Duals will be more cost effective in some applications, however, and an AD712 or OP-249 can used be for U2-U3 (clamping diodes may be necessary at U3).

This circuit is capable of very high performance with excellent SNR. Very careful circuit layout is necessary around the input of stage U1, the feedback components at U2, the high-impedance inputs of U3, and components R_6-R_7 and C_3- C_4 should be close to U3.

Moving Coil RIAA Preamplifiers

There are two general approaches which may be taken to satisfy the amplification requirement of a moving coil cartridge. These consist of two different methods by which the additional voltage gain required by the moving coil pickup may be achieved.

One technique is to use another low noise, flat, wideband preamp, ahead of an existing RIAA-equalized preamp. Such an amplifier stage is called a "pre-preamp" (also sometimes called a "head amp," for its place at the head of the signal path). A second technique is to incorporate the very high gain required directly into an RIAA equalized stage.

A pre-preamp circuit useful with any standard RIAA preamp is shown in Figure 8.25. Because of the extremely low source resistance from which this type of circuit must operate (≈10-100Ω), amplifier feedback resistances must be kept very low. Obviously, the input voltage noise of the amplifier used must also be low, in general ≤1nV/√Hz. Two devices which have noise voltages this low are the AD797 op amp, and the SSM-2017 in-amp.

SINGLE-ENDED RIAA "PRE-PREAMP" WITH 30/40dB GAIN

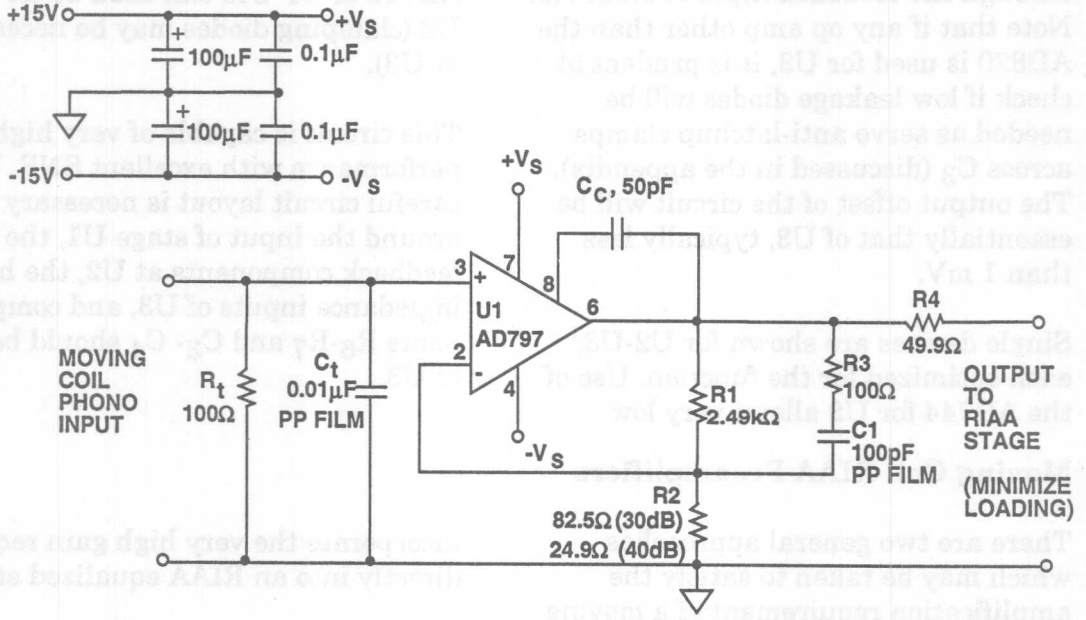


Figure 8.25

The circuit of Figure 8.25 is a pre-preamp suitable for low level input single ended applications. It uses an AD797 op amp in a low noise configuration, with either 30 or 40dB gain, adjustable by R_2. At the higher (40dB) gain the output noise of this circuit will be dominated by the source or the op amp, dependent upon the actual DC resistance of the cartridge in use. With a low resistance cartridge, it will be on the order of 2nV/√Hz.

Input terminating resistor R_t should be adjusted to suit the cartridge. C_t is relatively non-critical, but should be a low inductance film type to minimize RFI effects. Capacitor C_c acts as part of a distortion cancellation loop, in conjunction with the AD797's internal stages.

In a system, this circuit can be used two ways. One is as a stand-alone pre-preamp, used with another RIAA preamp, in which case a short low capacitance cable connects the output to that stage, and R_2 is set for the desired overall gain. Another way to use this circuit is as the first stage in either a passive or hybrid RIAA equalizer circuit, for example as a U1 stage replacement in either Figure 8.21 or Figure 8.23.

This entire stage replaces the entire U1 stage in one of those circuits, and R_1-R_2 are adjusted for the desired 1kHz gain. Typically this will be of the order of 50-60 dB, or about 20 dB higher than with the moving magnet transducer.

Taking the passive equalizer of Figure 8.21 as an example: the gain of stage U1 becomes 5-20 times higher, making it in the range of 100-400 times. For an overall gain of 54dB, R_2 of Figure 8.25 should be 20Ω for a U1 stage gain of about 125 times, or 42dB. Combined with the N1 network and stage U2 of Figure 8.21, the overall gain is then ≈510 times, or close to 54dB. The gain expression generally follows Eq. 8.11, but with the values of R_1 and R_2 from Figure 8.25 used in place of R_4 and R_3. The resistor shown in Figure 8.25 as R_4 then becomes the input resistance of the network N1, with the remainder of the circuit similar to Figure 8.21.

The AD797 is a stable DC amplifier, but with an input offset of ±80μV and cascaded DC gains above 1000, some form of overall DC stabilization will be needed. If it is used in the circuit of Figure 8.21, a DC servo should be used with the loop adjusted to null out the input referred offset which is ±150μV. The output amplifier can be a buffered composite amp using the AD744 and the AD811, as described in the "Line Drivers" discussion. Details of this configuration are left as an"exercise for the reader".

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TAPE PREAMPLIFIERS

A third audio preamplifier application is a magnetic tape or film playback system. These preamp circuits often operate at signal levels of 1 mV or less, placing stringent SNR requirements on the amplifier. In addition to high 1kHz gain, equalized frequency response is also necessary, which can raise the low-frequency gain as high as 80 dB. Few op amps can provide adequate loop gain with low input noise and high linearity under these conditions.

Tape Playback Basics

A generalized post-emphasis response curve required for tape playback is shown in Figure 8.26, similar in some senses to the generalized RIAA response of the previous section. These curves correspond to a subset of various tape playback response characteristics which meet the requirements of the IEC standard.[1] They are expressed here in dB relative to response at DC, over a range of 10Hz-100kHz.

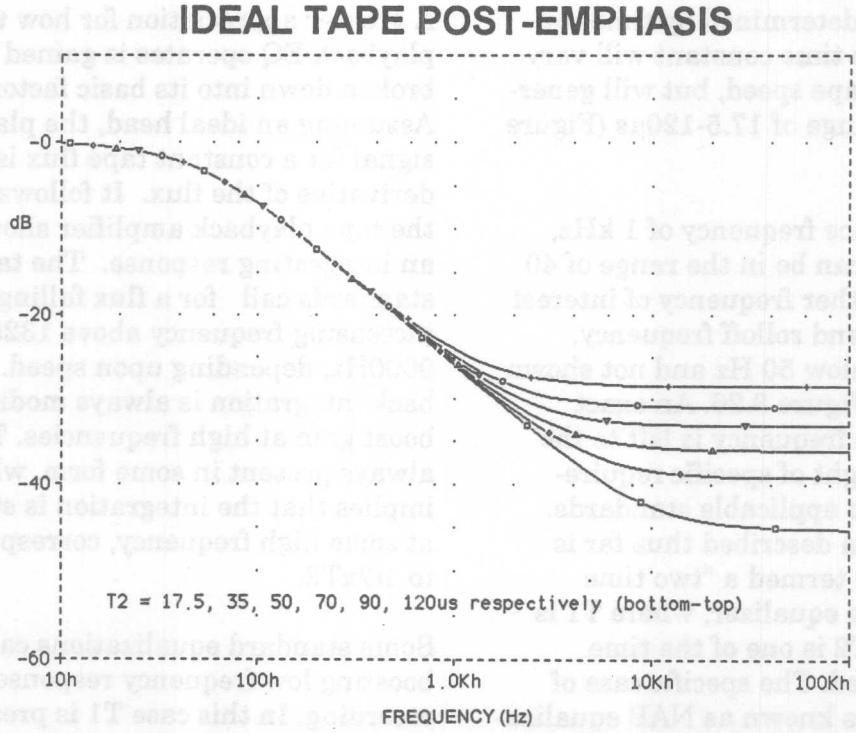


Figure 8.26

From Figure 8.26 gain is maximum below 50 Hz (f1), which is the lower corner frequency beginning the equalized portion of this curve, corresponding in this case to a 3180μs time constant, T1. (Note: as was true for the RIAA time constants of T1-T3, tape time constants T1-T2 are described here as they correspond to ascending frequency, the reverse of the terminology in [1]. The time constants themselves are identical). One major difference between RIAA and tape playback equalization is that there are many standard tape time constants, two for low frequencies and 5 for high frequencies, which can be combined differently. The discussions which follow place the similarities between RIAA and tape in context, then address the many differences necessary for tape equalization.

Above 50Hz, the response rolls off at 6 dB/octave until it reaches a corner frequency f2, determined by time constant T2. This time constant will vary according to tape speed, but will generally be in a range of 17.5-120μs (Figure 8.26).

At the reference frequency of 1 kHz, preamp gain can be in the range of 40 to 50 dB. Another frequency of interest is f0, the low-end rolloff frequency, somewhere below 50 Hz and not shown explicitly by Figure 8.26. An exact choice for this frequency is left to the designer, in light of specific requirements and the applicable standards. What has been described thus far is what could be termed a "two time constant" tape equalizer, where T1 is 3180μs, and T2 is one of the time constants noted. The specific case of 3180μs/50μs is known as NAB equalization, and used in a design example.

While the tape playback EQ curves of Figure 8.26 may appear similar to the analogous RIAA curves, this similarity is more superficial than fundamental. For the cases so far described, it is true that a tape playback amplifier can be modeled as a low pass amplifier (like the RIAA case, but with a single pole and zero). The design process to follow shows how to use these factors to advantage for a specific pair of time constants and gain.

However, the two time constant case is not the entire picture for tape EQ, as the low frequency time constant T1 can actually be extended towards DC. This makes the present design process less predictable. There are also other potential parasitic effects on the system, including the loading of the tape head, which should be addressed at some point during the design.

A greater appreciation for how the tape playback EQ operates is gained if it is broken down into its basic factors. Assuming an ideal head, the playback signal for a constant tape flux is the derivative of the flux. It follows that the tape playback amplifier should have an integrating response. The tape standards call for a flux falling with increasing frequency above 1325 to 9000Hz, depending upon speed. Playback integration is always modified to boost gain at high frequencies. T2 is always present in some form, which implies that the integration is stopped at some high frequency, corresponding to $1/2\pi T2$.

Some standard equalizations call for boosting low frequency response in recording. In this case T1 is present, and integration is stopped at a low

frequency, $1/2\pi T1$. For cases without low frequency boost, $T1 \Rightarrow \infty$, and the integration continues down until limited by circuit practicalities.

Many non-ideal factors related to the tape pickup head may also require correction. These include non-uniformity of frequency response (eddy-current losses, RC head loading), wavelength response (gap-length loss, head bumps), lot-lot variability, etc. Most tape playback EQ circuits therefore provide trims for one or more head design parameters, to accommodate these limitations and to allow best overall calibration. This process involves playback of a standard test tape through the system, chosen for the standard involved.[1,2] In view of the above factors, a "universal" tape playback EQ circuit is impossible, and a well designed practical circuit should make allowances for external factors.

A "Two Time Constant" Design Example

A flexible tape preamp with a range of possible uses is shown in Figure 8.27. This circuit is most effective with only a few selected op amps, preferably a low noise, decompensated FET input type such as the AD745, or possibly either of the low noise bipolar input OP-37 or SSM-2139.

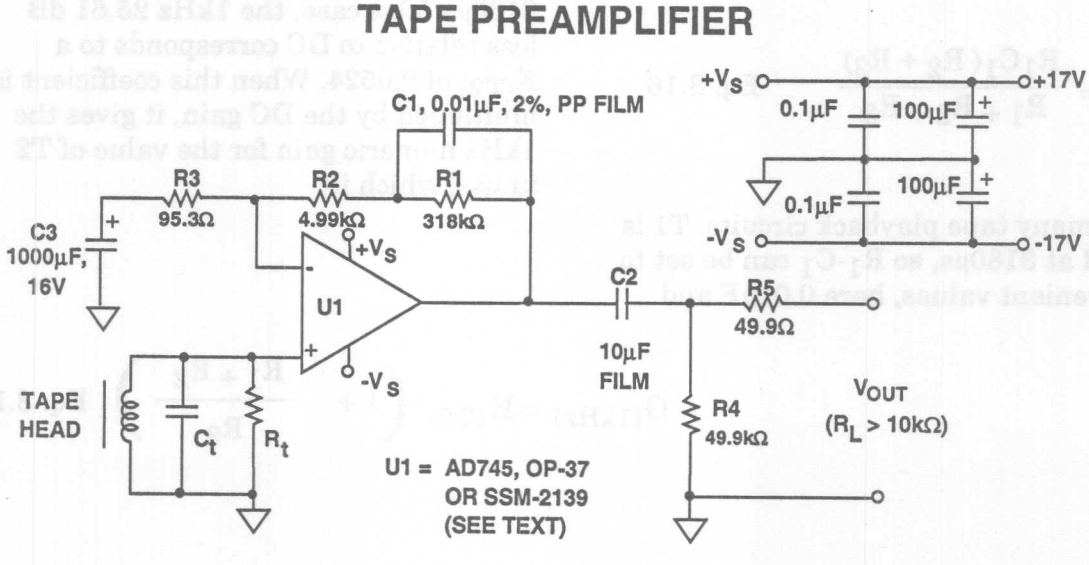


Figure 8.27

This preamp design has a high frequency gain greater than unity, due to the presence of T2 and can therefore take advantage in the extended bandwidth and low SNR in a decompensated amplifier. Possible alternates and further selection criteria are discussed below. This circuit may be used as it stands, or with other component values for specific time constants and/or gains.

The gain and equalization characteristics of this circuit are set by the feedback network, which consists of R_1-R_3 and C_1. The interactions of these components are best appreciated when analyzed as a network, as was done for RIAA preamps. In this case, two time constants are involved, T1 and T2, but the general design approach is similar to that for an RIAA active feedback preamp.

In the circuit of Figure 8.27, time constants T1 and T2 are set as:

$$T1 = R_1C_1 \qquad \text{Eq. 8.15}$$

and,

$$T2 = \frac{R_1C_1(R_2 + R_3)}{R_1 + R_2 + R_3} \qquad \text{Eq. 8.16}$$

For many tape playback circuits, T1 is fixed at 3180µs, so R_1-C_1 can be set to convenient values, here 0.01µF and 318kΩ. Time constant T2 will be unique to a given playback speed, so Eq. 8.16 above is solved for this case. The T2 of 50µs used yields R_2 = 4.99kΩ.

The ratio of ($R_1 + R_2 + R_3$) to R_3 determines the gain at DC (similar to the RIAA case), so the nominal 1kHz gain and T2 are somewhat interactive. In practice however, small variations in R_3 have minimal effect on the frequency response.

For equalization using the 3180µs time constant, the 1kHz gain can be related to an (ideal) DC gain, since the stage is a low pass amplifier with a pre-defined response. For a T2 of 50µs the DC/1kHz difference is 25.61 dB. For other T2 and a given 1kHz gain, the DC gain can be calculated, so that given the desired gain at 1kHz, it is then possible to select the R_1-R_3 ratios.

It is generally convenient in this design process to relate the DC/1kHz relative gains in terms of the equivalent 1kHz scaling coefficient, "K", where K is unique to a given T2, or "$K_{(T2)}$". In the 3180µs/50µs case, the 1kHz 25.61 dB loss relative to DC corresponds to a $K_{(T2)}$ of 0.0524. When this coefficient is multiplied by the DC gain, it gives the 1kHz numeric gain for the value of T2 in use, which is:

$$G_{(1kHz)} = K_{(T2)}\left(1 + \frac{R_1 + R_2}{R_3}\right) \qquad \text{Eq. 8.17}$$

Or for the example of T1/T2 = 3180µs/50µs, the 1kHz gain is:

$$G_{(1kHz)} = 0.0524\left(1 + \frac{R_1 + R_2}{R_3}\right) \qquad \text{Eq. 8.18}$$

Since the time constants should be the first variables to be resolved in the design process, R_3 remains for the overall network gain adjustment, after R_1-R_2 are selected. Given a gain at 1kHz of $G_{(1kHz)}$ and the scaling coefficient $K_{(T2)}$ for the T2 in use, R_3 can be calculated from:

$$R_3 = \frac{R_1 + R_2}{\frac{G_{(1kHz)}}{K_{(T2)}} - 1} \qquad \text{Eq. 8.19}$$

In this 3180µs/50µs example the 1kHz gain is 45dB, so $G_{(1kHz)}$ is 177.83, and $K_{(50)}$ is 0.0524, thus R_3 works out as 95.3Ω (nearest standard value).

Figure 8.28 illustrates the relative accuracy of this NAB tape equalizer using the chosen component values and an AD745 op amp model in a SPICE simulation. The 45 dB gain is accurate within 0.1dB at 1kHz, and the frequency response errors of the circuit relative to the ideal 3180µs/50µs time constants are within ±0.1dB over 20Hz-20kHz (not shown). Similar results should be expected using other T2 options. Figure 8.29 lists time constants from 30-120µs, and their corresponding scaling coefficients.

8

NAB 50µs POST-EMPHASIS CIRCUIT, R1 = VARIOUS VALUES

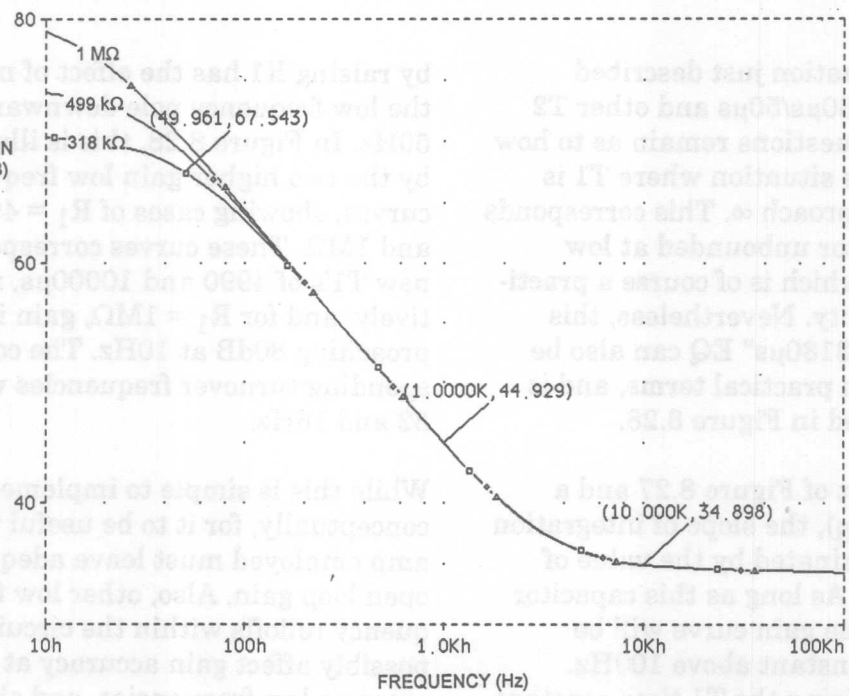


Figure 8.28

1kHZ SCALING COEFFICIENTS FOR TAPE EQUALIZERS FOR T2 = 17.5, 35, 50, 70, 90, AND 120μs

T2, μs	K (T2)
17.5	0.0503
35	0.0512
50	0.0524
70	0.0546
90	0.0574
120	0.0626

Figure 8.29

T1 > 3180μs

While the situation just described covers the 3180μs/50μs and other T2 cases, some questions remain as to how to address the situation where T1 is allowed to approach ∞. This corresponds to an integrator unbounded at low frequencies, which is of course a practical impossibility. Nevertheless, this case of "T1 > 3180μs" EQ can also be approached in practical terms, and is also illustrated in Figure 8.28.

For the circuit of Figure 8.27 and a given gain (R_3), the slope of integration is largely dominated by the value of capacitor C_1. As long as this capacitor is constant, the gain curve will be essentially constant above 100Hz. Therefore, raising the T1 time constant by raising R1 has the effect of moving the low frequency pole downwards from 50Hz. In Figure 8.28, this is illustrated by the two higher gain low frequency curves, showing cases of R_1 = 499kΩ and 1MΩ. These curves correspond to new T1's of 4990 and 10000μs, respectively, and for R_1 = 1MΩ, gain is approaching 80dB at 10Hz. The corresponding turnover frequencies would be 32 and 16Hz.

While this is simple to implement conceptually, for it to be useful the op amp employed must leave adequate open loop gain. Also, other low frequency rolloffs within the circuit may possibly affect gain accuracy at the extreme low frequencies, and should be

checked. Practically speaking, when a T1 $\rightarrow \infty$ EQ case is used, a trim for the R_1 value should be provided, and the circuit time constants for R_3-C_3 and C_2-R_4 should be appreciably greater than the effective T1 value. The op amp used should have an open loop gain of one million or more, which is the case for the AD745.

Optimizing the Remaining Circuit

Other circuit details around U1 are also important in realizing the full potential of this configuration. For lowest noise, the value of resistor R_3 should be low in comparison to the source resistance. Capacitor C_3 and R_3 set the low frequency rolloff frequency, which is ≤2Hz for the values shown in Figure 8.27. Output coupling capacitor C_2 also sets an LF cutoff at 0.16Hz with a 10kΩ load. Note that this is the lowest recommended load for the circuit for best EQ accuracy and overall performance, unless U1 is provided with additional buffering for greater drive.

If R_3 is made variable, it can provide gain trim for the circuit, varying the 1kHz gain by +5 and -4dB, about 45 dB, using a 50Ω resistor and 100Ω pot. *Note that wide range gain adjustment is not generally recommended, due to potential interactions with frequency response.* For greater gain changes, a better solution is a design re-scaled around the higher (or lower) 1kHz gain, which may then be trimmed if necessary. Gain can also be trimmed in a post EQ gain stage which may also serve as a buffer amplifier.

If adjustment of T2 is wanted, resistor R_2 can be made variable, to accommodate the various playback curves. *However, when a decompensated amplifier is used, the minimum allowable value of R_2 is 4 × R_3 for stability reasons.*

Using an op amp with input offset of less than 1mV (which is the case with all those mentioned), the maximum output DC offset from U1 will be on the order of a few mV when C_3 is used, since the amplifier operates with unity DC gain. This provides maximum headroom, and for ±15V supplies output signals of 5Vrms or more are possible, since the film capacitor C_2 decouples the offset at V_{OUT}. Note that if a more loosely controlled offset or high DC bias current device is used for U1 (such as a 5534), the simple biasing may not work as well. An alternate form of DC control is a servo loop for lowest output offset, using the general concepts described both in the microphone and RIAA preamp sections and the appendix. This tape EQ stage is topologically similar to the output stage of Figure 8.23, and could use a servo in a similar fashion.

It is not recommended that other op amps be substituted for the AD745 in this circuit, unless they are selected for low noise and distortion, for high gain, and for DC biasing compatabilities. Some alternatives which might be considered are the OP-37 or SSM-2139, which are bipolar. The most critical performance spec for U1 is low input noise, which in this application means both low voltage noise and low current noise. For high impedance heads, the current noise may well be more important than voltage noise, since the source impedance is inductive. To place this in

some perspective, a 1H head with a 1kHz Z of 10kΩ can have a effective 1kHz noise density component of 10nV/√Hz due to the effect of amplifier noise current, when used with an 1pA/√Hz amplifier. Of course, since noise sources add in root sum of squares fashion, in any given case there may be several noise sources which affect the equivalent input noise at the amplifier input. Reactive sources such as tape heads can require a low current noise amplifier, just as much as they also need one with low voltage noise. The AD745 excels in current noise, with a 1kHz noise density of 6.9fA/√Hz. In contrast, low noise bipolar input amplifiers such as the OP-37 and SSM-2139 have noise current densities of 0.4-0.6pA/√Hz (while their voltage noises are on a par with the AD745, ≈3.5nV/√Hz). For low-Z heads, an ultra-low voltage noise device like the AD797 may be useful.

For highest circuit performance, use 1% metal-film resistors and 1-2% polypropylene film capacitors in the gain and equalization components, for the reasons noted in the RIAA discussions. Power supplies should be well regulated, and in the range of ±15V to ±18V.

While the above method of equalization can yield excellent results insofar as the *amplifier* frequency response is concerned, the tape head must also be properly terminated in the prescribed network for flattest playback response with a standard test tape. R_t and C_t are intended to serve part of this purpose, and final adjustments for frequency response may include trim of the EQ components.

REFERENCES: TAPE PREAMPLIFIERS

1. IEC, "Magnetic Tape Sound Recording & Reproducing Systems", Publication 94-1, Fourth Edition, 1981.

2. "Choosing and Using MRL Calibration Tapes", Magnetic Reference Laboratory, Inc., 229 Polaris Ave, Suite 4, Mountain View, CA, 94043.

3. Scott Wurcer, "Designing Circuits for Low Noise", discussion in AD745 data sheet, **Amplifier Reference Manual**, 1992, Analog Devices.

4. C. Motchenbacher, F. Fitchen, **Low-Noise Electronic Design**, Wiley, New York, 1973.

AUDIO LINE LEVEL STAGES

Audio line level stages represent an intermediate level in dynamic range for practical audio circuits using modern IC devices. Line level amplifying stages generally work with single-ended or balanced input/output signal levels of 1-10V, and at medium levels of power. This section discusses some basic types of audio line stages which are:

- *Line receivers* - including line receiver stages which accept single-ended or balanced line level signals with maximum noise immunity, and provide scaled outputs for further processing.

- *Line amplifiers* - including amplifiers which scale a received signal in single-ended form and feature low distortion designs.

- *Line drivers* - including single-ended and balanced drivers which are capable of driving appreciable output levels in terms of voltage swing, current levels, and/or difficult loads, such as capacitive lines.

Some general concepts of line driving and buffer amplifier design have been covered previously, with emphasis on video applications.[1-3] The material in this section continues the discussion and expands on those themes with audio line-receivers and line-drivers as examples.

Audio transmission systems, unlike their video counterparts, do *not* generally use terminated transmission lines, so long transmission lines usually appear capacitive. Therefore, capacitive load isolation is important in audio drivers. In general, when building audio circuits of any type, "housekeeping" rules of layout and bypassing are strongly recommended, particularly for the buffer and line driver circuits.

The function of sending/receiving audio signals between various parts of a system has traditionally involved tradeoffs of one form or another. Fully differential or balanced transmission systems are best at rejecting low frequency and RF noise, so they are used for high performance, and are discussed in some detail following.

A typical audio system block diagram using differential transmission is shown in Figure 8.30. A balanced transmission system like this might use several input/output coupling schemes. Some major points distinguishing coupling methods are discussed briefly before considering actual circuits.

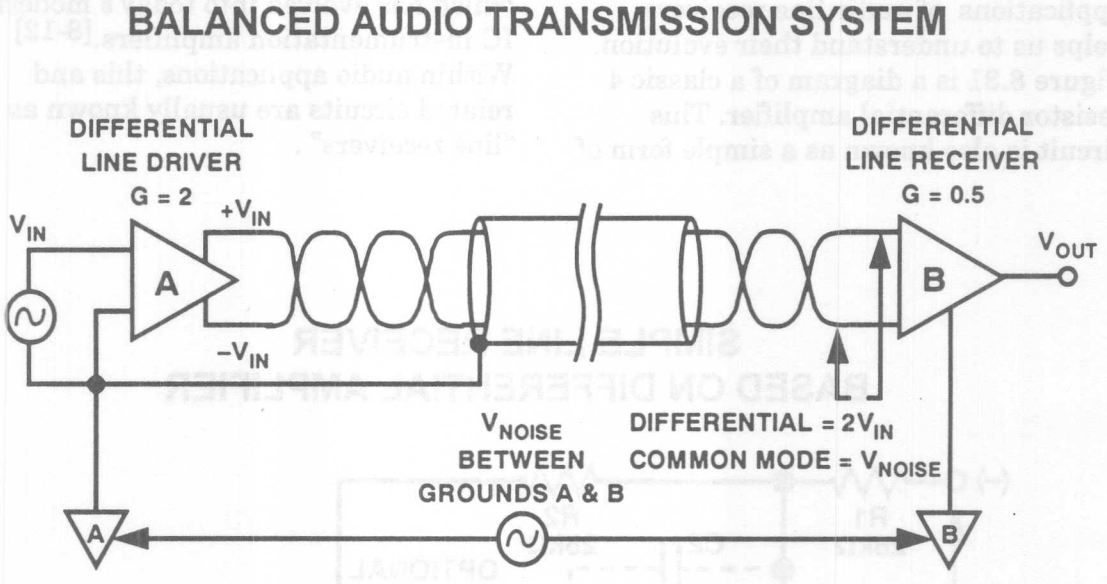


Figure 8.30

Transformers[4-7] have been a traditional audio line coupling element, at both input or output. They have well known problems with noise pickup, frequency response, distortion, and operating level. While these problems are all soluble to some extent, the solutions are usually costly. Nevertheless, transformers are unexcelled in some applications.

The outstanding virtue of transformers is the ability to *isolate*, which shows in two regards. They can galvanically isolate drive/receive stages (up to the breakdown potential of the windings), allowing signals to be transmitted across high ground potential differences (tens or hundreds of volts). This feature is one quite difficult to achieve with solid state circuitry. Also, suitably designed transformers can have very high common mode rejection (CMR) in the audio range, in excess of 100dB. Some transformer-isolated driver stages are described in this section.

The general system of Figure 8.30 can in principle use either transformer or active coupling to the line. The goal for either approach is to reproduce a final signal V_{OUT} equal to V_{IN}, while rejecting noise between grounds A and B by 80- 100dB. A typical unity gain design uses a line drive of $\pm V_{IN}$ and a receiver gain "G" of ½, to maximize receiver CM range.

AUDIO LINE RECEIVERS

Walt Jung, Adolfo Garcia

A brief review of the topologies and applications of audio line receivers helps us to understand their evolution. Figure 8.31 is a diagram of a classic 4 resistor differential amplifier. This circuit is also known as a simple form of *instrumentation amplifier* (in-amp), which has evolved into today's modern IC instrumentation amplifiers.[8-12] Within audio applications, this and related circuits are usually known as "line receivers" .

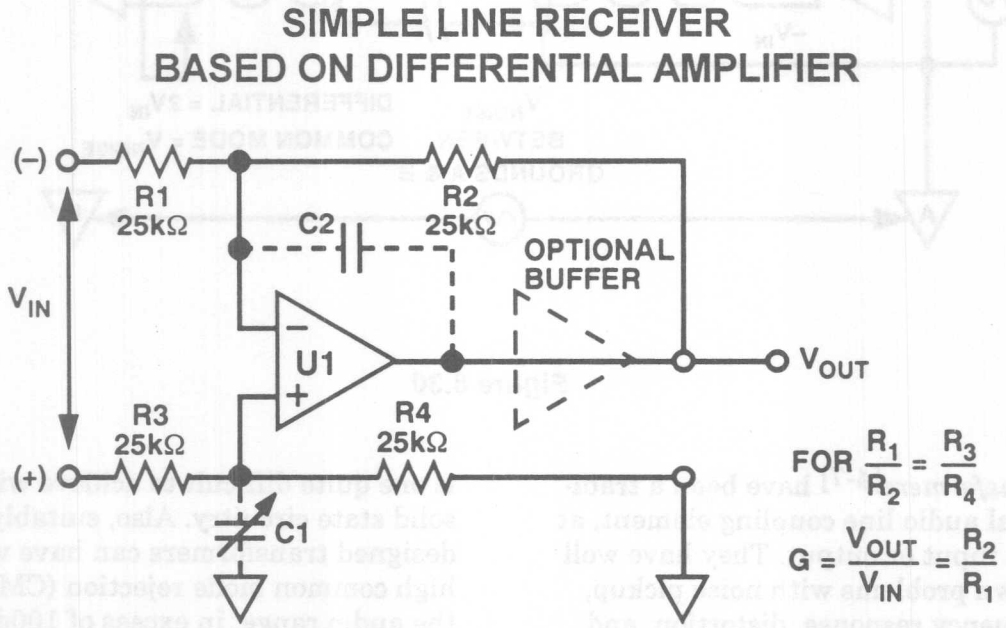


Figure 8.31

The Simple Line Receiver

This simple line receiver circuit uses four resistors and an op amp for gain. Such bridge-based difference amplifiers are *critically* dependent upon the resistor ratio matching for good performance, an enormously important point. The amplifier can also be critical, but many practical limitations of these topologies arise from bridge *un*-balance which may be at AC or DC or both.

The circuit appears somewhat trivial, as the minimum ingredients are four matched film resistors and a good audio op amp. While this works functionally, how well it works in rejecting line noise is uncertain.

The main purpose of all line receivers is to reject common-mode noise, picked up on a twisted pair transmission line.

Even with a high quality op amp for U1, noise rejection is only as good as the resistor matching. More precisely, the *ratios* of resistors R_1/R_2 and R_3/R_4 must match extremely well to reject common mode noise (the absolute values are relatively unimportant).

Picking four 1% resistors from a single batch may yield ratio matching of 0.1%, which will achieve a common mode rejection (CMR) of 66dB. If one resistor differs from the rest by 1%, the CMRR will drop to only 46dB. In general, the worst case CMR of a circuit of this type is[8]

$$CMR(dB) = 20\log\left(\frac{1 + R_2/R_1}{4K_r}\right) \qquad \text{Eq. 8.20}$$

where "K_r" is the *individual* resistor tolerance in fractional form, where 4 discrete resistors are used. A single component network with a net matching tolerance of K_r would probably be used for this circuit, in which case the expression would then be:

$$CMR(dB) = 20\log\left(\frac{1 + R_2/R_1}{K_r}\right) \qquad \text{Eq. 8.21}$$

Either case assumes a significantly higher *amplifier* CMR (≥100dB).

Eq. 8.20 shows that the worst case CMR due to tolerance build-up for 4 unselected 1% resistors to be no better than 34dB. Clearly for high noise rejection, circuits such as these need four single-substrate resistors, with very high absolute and TC matching. Such networks using thick- and thin-film technology are available from companies such as Caddock and Vishay-Ohmtek, in ratio matches of 0.01% or better.

Some simulations may bring this point of critical matching home more clearly. Figure 8.32 shows the effect of various DC mismatches on a differential amplifier like that of Figure 8.31, with a single resistor mismatch in R_1 of 0.1% (top trace), 0.01% (middle trace) and perfect matching (bottom). This display of CM error vs. frequency also shows a reactive imbalance for the perfect DC-balanced (bottom) case, due to an intentional capacitive mismatch.

BASIC LINE RECEIVER COMMON MODE REJECTION VERSUS FREQUENCY FOR VARIOUS DC TRIMS (SIMULATION)

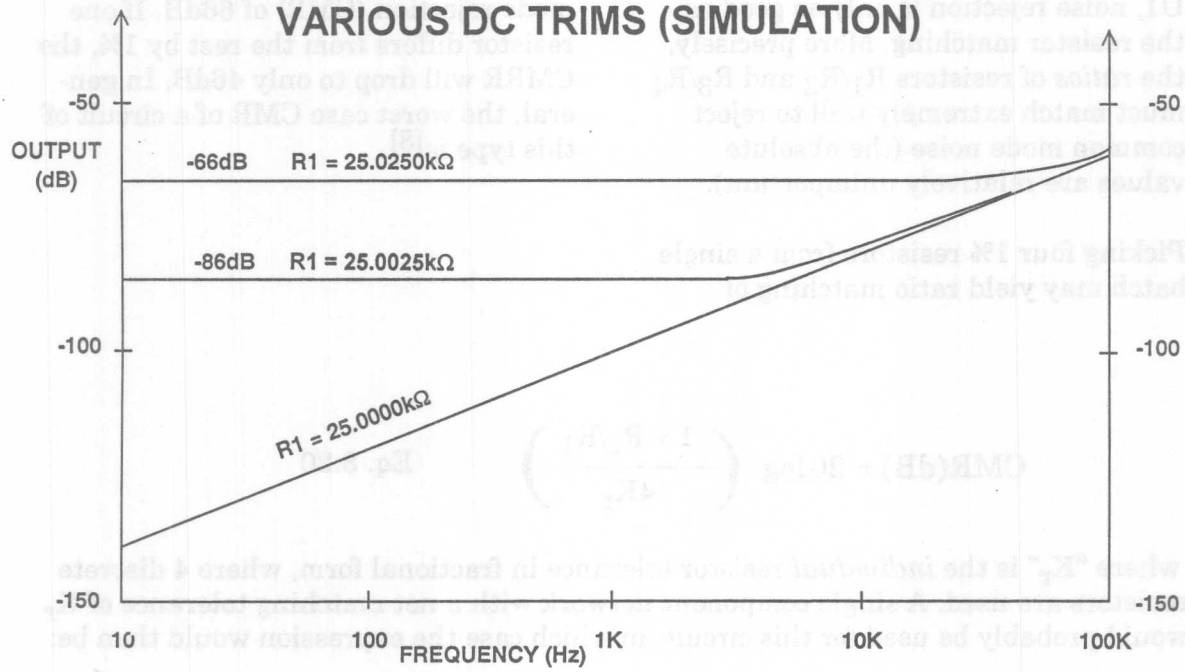


Figure 8.32

BASIC LINE RECEIVER COMMON MODE REJECTION VERSUS FREQUENCY FOR VARIOUS AC TRIMS (SIMULATION)

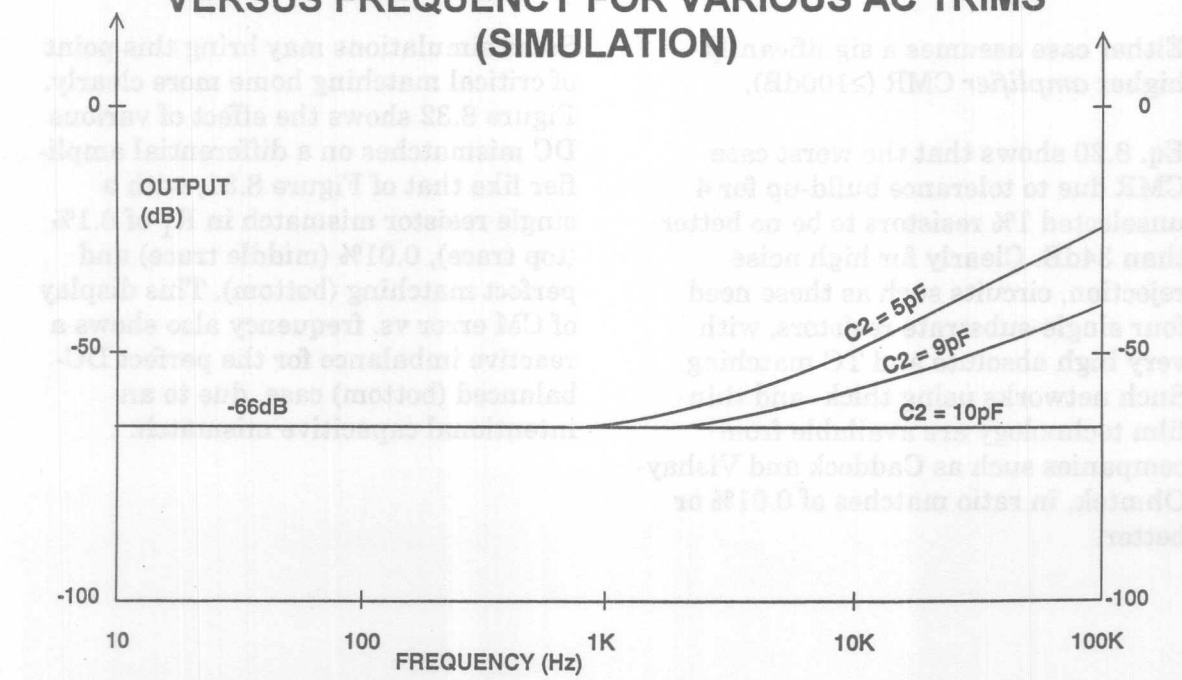


Figure 8.33

Figure 8.33 shows the effect of AC matching on this differential amplifier using 0.1% DC matched resistances, with C_2 varied away from a nominal match to C_1 (10pF). A 10% mismatch here results in a CM degradation as low as 10kHz.

Clearly, for wideband audio use, the bridge ratio needs to be maintained at AC as well as DC, to achieve flat CMR versus frequency. Capacitances from the R_2/R_1 and R_4/R_3 nodes need to be balanced. In practice, this is best achieved with very low and/or balanced parasitic capacitances at C_1-C_2.

It is worthy of note that this circuit also has a highly desirable property; that is, it *attenuates* the input CM voltage. Thus it inherently has some protection against overvoltage. In general, practical line receivers *require* input CM division, for safe use in harsh environments and to allow CM voltages to exceed the supply rails. For simplicity, the receiver gain resistors should also perform this function, as here.

The working CM input range of the circuit in Figure 8.31 is $(1+(R_3/R_4))\times V_{CM(U1)}$, and the differential input resistance is R_1+R_3. Gain of the circuit may not easily be changed, because of the matched resistor ratios.

8

Implementing the Simple Line Receiver Function

To present a reasonably high impedance to the line, receivers of this type typically use input resistances of 20kΩ or more. Given a well matched resistor network and low or balanced parasitic capacitances, suitable amplifiers for U1 are the AD711, AD744 and SSM-2131 (singles), and the AD712, AD746, OP- 249, OP-275 and SSM-2139 (duals). With 10kΩ-25kΩ resistances, extremely low voltage noise in the amplifier is not highly critical, but high slew rate and output drive allows clean high frequency, high amplitude levels, and 600Ω load capability. If low impedance loads need to be driven, output current of a standard op amp can be boosted with an "in-loop" unity gain buffer, connected between U1 and the load/feedback point. Devices such as the BUF-04 unity gain buffer or a follower-connected AD811 can serve for this function.

From the criteria of DC and AC trim/balance, the circuit in Figure 8.31 is most effective when the resistors and amplifier are made in a single monolithic IC. The Analog Devices 8 pin SSM-2141 and SSM-2143 are such ICs, designed and characterized as low distortion, high CMR audio line receivers with net gains of unity (SSM-2141), and 0.5 (SSM-2143). The SSM-2141 has resistors just as shown in Figure 8.31, while the SSM-2143 uses 12kΩ/6kΩ resistors.

Even with these devices the resistor pinouts are such that buffers can be easily added if needed. In both the SSM-2141 and SSM-2143 for example, the amplifier output appears at pin 6, the feedback resistor is at pin 5, and the reference resistor is at pin 1. With $V_{IN(+)}$ and $V_{IN(-)}$ at pins 3 & 2, respectively, a unity- gain buffer can be connected as shown symbolically in Figure 8.31, and the buffered output taken from pin 5.

In applying circuits of the Figure 8.31 type (or other topologies which resistively load the source), a designer must

bear in mind that all *external* resistances added to the circuit can compromise CMR. To place this in perspective, a 2.5Ω or 0.01% mismatch can easily occur with wiring, and if not balanced out, this mismatch will degrade the CMR of otherwise perfectly matched 25kΩ resistors to 86dB. These circuits are therefore best fed from balanced low impedance sources.

Other Issues with the Simple Line Receiver

An application point which becomes relevant for large systems with multiple balanced pair lines is the issue of receiver *load balance*. Ideally, an audio line receiver should exhibit equal AC loading at the two inputs. With the simple line receiver of Figure 8.31, this goal is not met- i.e., the circuit does not present balanced loading to the input lines.

When driven with a balanced voltage $2V_{IN}$, as from complementary sources, the simple line receiver exhibits unbalanced input currents in the R_1 and R_3 legs, due to feedback action. For the values of Figure 8.31, the current in R_1 is 3 times that in R_3.

In large systems with multiple balanced transmission line pairs, the current imbalance in the input lines is potentially serious, as associated fields will not cancel as they do for balanced loading. There is thus potential for crosstalk in systems using simple line receivers.

But, while not optimum from a large system and/or line balance viewpoint, the simple line receiver is nevertheless quite useful in more modest situations. With resistors R_1-R_3 relatively high (20k or more), it is adequate for small-scale or confined systems where I/O lines are relatively short, few in number, or they are not cabled. In such uses, devices like the SSM-2141 and SSM-2143 serve well as efficient single IC receivers.

Balanced Line Receivers

It is important in the highest performance systems that audio line receivers exhibit equal loading to the source at both inputs- i.e., they should be truly balanced. At least two topologies behave in this way and are well suited for professional use in balanced systems.

Balanced Feedback Differential Line Receiver

Birt[7] of the BBC has analyzed the simple line receiver topology and presented a modified and balanced form, shown in Figure 8.34. Here U1 uses an 4 resistor network identical to that of Figure 8.31, while feedback from unity gain inverter U2 drives the previously grounded R_4 reference terminal. This has two overall effects; the input currents in the two input legs become equal, and the gain of the stage is halved.

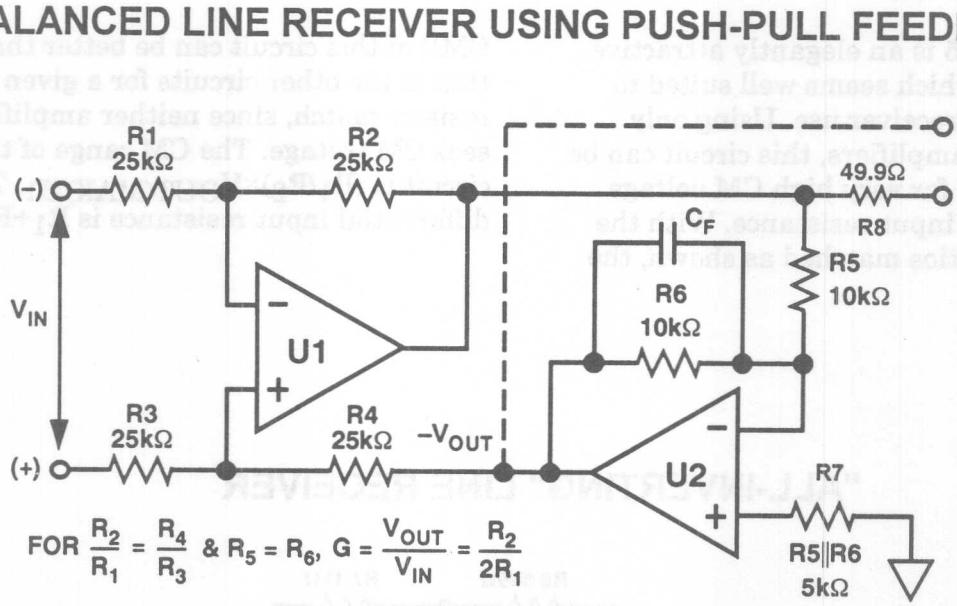


Figure 8.34

Compared to Figure 8.31, and for like resistor ratios, the Figure 8.34 gain from V_{IN} to V_{OUT} is ½, or a gain of -6dB (0.5) as shown. However it also offers an optional complementary output from U2, $-V_{OUT}$. Like the circuit in Figure 8.31, the gain of this circuit is not easily changed.

Because of the two feedback paths, this circuit holds the inputs of U1 at a null for differential input signals. However CM signals are seen by U1, and the CM range of the circuit is $(1+(R_3/R_4))\times V_{CM(U1)}$. Differential input resistance is R_1+R_3.

The circuit can be broken into a simple line receiver and an inverter. Thus line receivers like the one in Figure 8.31 can be converted to balanced form by adding an appropriate inverter, U2. The performance of an example of this circuit is discussed below.

Alternate Balanced Line Receivers

Other types of instrumentation amplifiers can achieve fully balanced input loading, but may be undesirable for other reasons. For example, there are standard in-amp circuits which use either 2 or 3 amplifiers and have high input impedance, due to the use of non-inverting inputs.[8-11] The drawback of these circuits as line receivers lies in their limited gain and CM range, and they also require four additional resistors for overload protection. Since these resistors also influence gain and CMR, they must be precision ratio matched types. As a net result, workable audio line receivers using such in-amps are not really practical as they require 8 or more matched resistors and 2 or 3 op amps.

"All Inverting" Line Receiver

Figure 8.35 is an elegantly attractive topology which seems well suited to audio line receiver use. Using only inverting amplifiers, this circuit can be configured for very high CM voltage range and input resistance. With the resistor ratios matched as shown, the CMR of this circuit can be better than that of the other circuits for a given resistor match, since neither amplifier sees CM voltage. The CM range of this circuit is $(R_1/R_2)\times V_{OUT(MAX)U1}$. The differential input resistance is R_1+R_3.

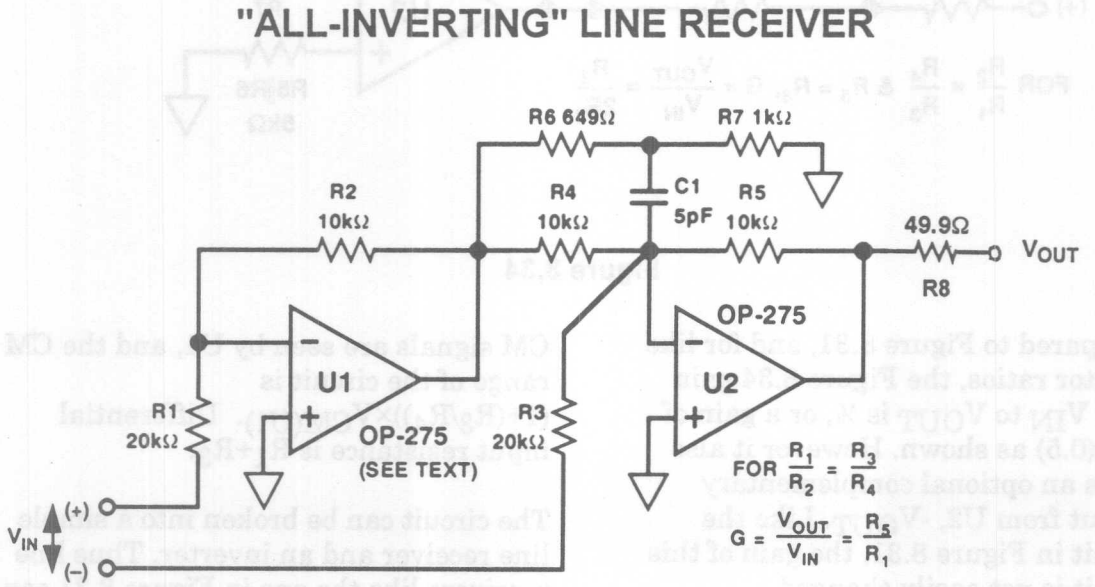


Figure 8.35

The circuit has the unusual and desirable property of single resistor gain adjustment via R_5, but *without* affecting CMR interaction. The gain extends from well below to well above unity. As shown it is driven with a balanced signal, but it can also be driven single-ended at either the (+) or (-) terminal, with no gain interaction from the opposite input port. A number of inputs can be summed, by adding additional ratio matched input resistor pairs (not shown). In this example the gain is set at 0.5, to be consistent with the general line receiver system requirements.

This circuit is also well known in its basic form.[8-11] However, in this example phase lead compensation is used to enhance high frequency CMR. A small capacitor shunting R_4 with a value chosen to compensate for the gain-bandwidth of U1 compensates for the lag through U1, and maximizes phase matching of the ± CM signals at U2. However, for op amps with gain bandwidths above a few MHz and practical resistor values, the capacitors required may be too small to be practical.

The R_6-R_7-C_1 tee network reduces the effective value of C_1, by dividing the applied voltage. A nominal division ratio for compensation capacitance (C_c) can be approximated by:

$$K_c = \frac{1}{2\pi BW_{(U1)} R_4 C_1} \qquad \text{Eq. 8.22}$$

where "K_c" is the division ratio of R_6-R_7. For this example, with BW(U1) about 5MHz (the closed loop bandwidth of U1), K_c is about 0.6, making C_c effectively about 3pF. Circuit parasitics, loading effects and part variations make this inexact; however, once nominal compensation for a given layout and devices is achieved, a 30dB CMR improvement in 10kHz CMR is possible relative to no phase compensation at all. While the phase compensation network is not absolutely necessary to the circuit's basic function, it does make a significant CMR performance difference for audio applications.

8

Performance

The balanced line receiver configurations of Figure 8.34 and Figure 8.35 were tested for CM performance, with common conditions of G=0.5, Vs=±18V, and a 10Vrms input sweep, 20Hz-50kHz, filter bandwidth of 80kHz. The Figure 8.34 circuit was built with U1 as an SSM-2141, and U2 as an OP-275 inverter, with C_F=68pF. The Figure 8.35 topology was implemented with an OP-275 and a resistor network matched to 0.005%, with the phase lead network trimmed to the values shown (for best high frequency CMR). The results are shown in Figure 8.36.
Both circuits show excellent results, with ≤1kHz CM errors of -100dB or less and little sensitivity to source impedances of 50Ω-600Ω (not shown). The circuit in Figure 8.35 offers better results at higher frequencies, perhaps due to the trimming technique used which is not applicable to the Figure 8.34 circuit. In the worst case, the CM errors are no worse than -80dB at 10kHz, very good for an untrimmed circuit. While CM performance data was measured for the Figure 8.35 circuit with several of the other dual devices mentioned with good- to-excellent results, the OP-275 was chosen to be illustrated here because of its generally higher output drive and all-around utility.

BALANCED LINE RECEIVER COMMON MODE ERROR VERSUS FREQUENCY FOR G = 0.5, V_S = ±18V, R_S = 600Ω

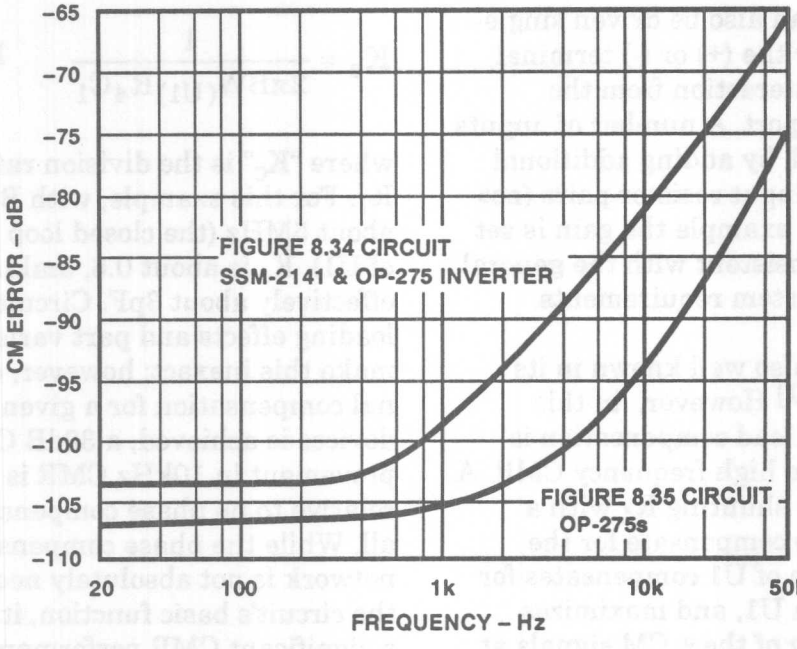


Figure 8.36

BALANCED LINE RECEIVER THD + N (%) VERSUS FREQUENCY (Hz) FOR G = 0.5, V_{in} = 1, 2, 5, 10V rms, V_S = ±18V

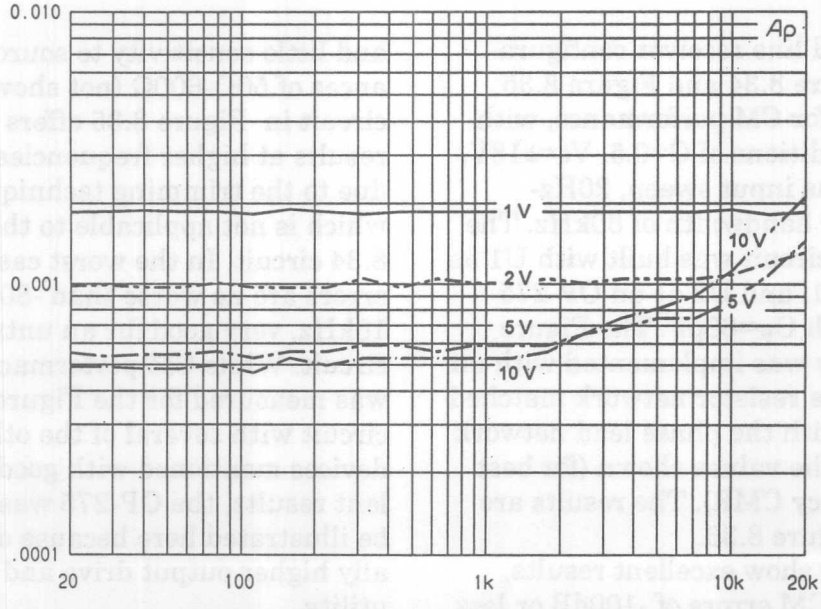


Figure 8.37

THD+N data was taken for both circuits and, while dominated by the noise floor at many levels, there are some differences worth noting between the two. Figure 8.37 shows THD+N performance of the Figure 8.34 SSM-2141/ OP-275 circuit for loading conditions of 100k, and successive input sweeps of 1, 2, 5 and 10Vrms. The lower level sweeps are noise dominated, while the 5 and 10V sweeps show some increase in distortion at high frequencies. Distortion in this circuit also rises with loading of 600Ω (not shown).

The performance of the circuit in Figure 8.35 for similar drive conditions is shown in Figure 8.38, and for conditions of 600Ω loading. These data indicate less loading and frequency dependence, due primarily to the OP-275's higher slewrate and greater output drive into 600Ω loads.

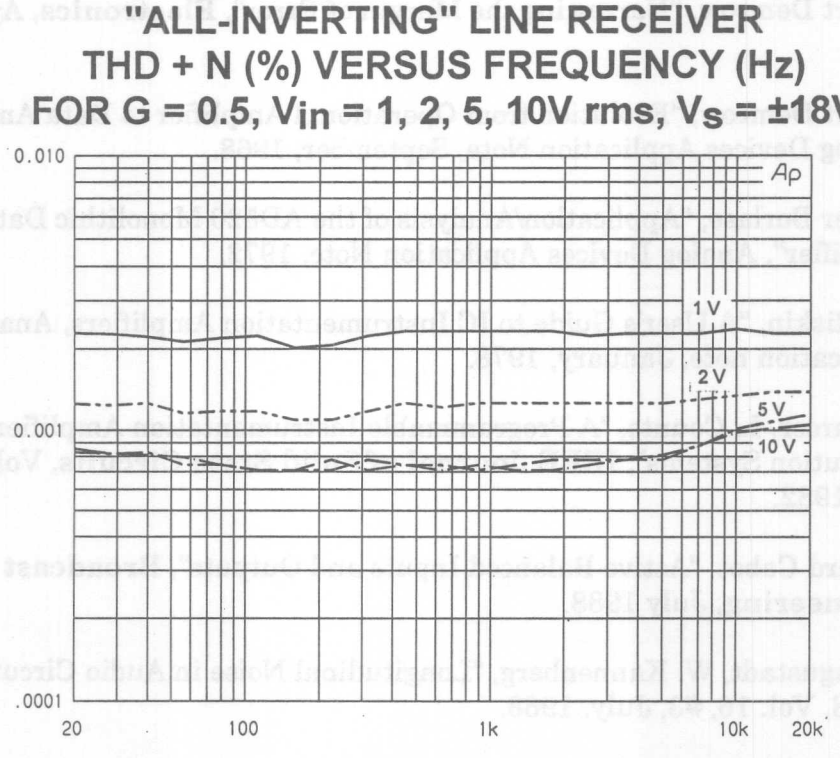


Figure 8.38

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AUDIO LINE DRIVERS AND BUFFERS

Audio line drivers and buffer amplifiers can take a wide variety of forms, which include single-ended and differential output drivers, as well as transformer isolated drivers. Within these general formats there are many different performance options, many of which are covered in this section.

Many op amps useful as video drivers and buffers also do well as audio drivers, because of the high current output stages necessary for good linearity over video bandwidths.[1,2] Some examples of video amplifiers which are useful for audio are the AD810, AD811, AD817, AD818, AD829, AD840 series, AD845, AD846, and AD847. Other types notable for either high or unusually linear output drives or other performance features useful in audio applications are the AD797, OP-275, and SSM-2131.

High Current Buffer Basics

As a preliminary to detailed application discussions, some basic circuit principles germane to high current buffers and drivers should first be considered. With output currents up to 100mA or more, "housekeeping" details of bypassing, grounding and wiring become even more important than usual, and must be considered. These are briefly discussed here in the context of high current buffers, using the unity gain buffer circuit of Figure 8.39 as a point of departure.

UNITY GAIN STAND-ALONE BUFFERS

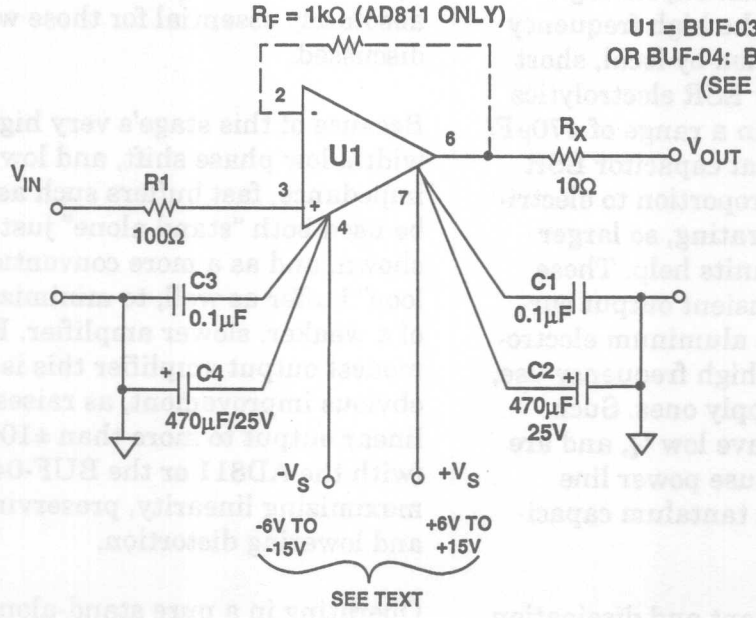


Figure 8.39

First, whichever IC is used for U1, close attention should be given to making buffer stages free from parasitic capacitances and inductances, at input, output, and supplies. Physical construction of buffer-drivers and other high current stages should be in accordance with high speed rules. A continuous copper ground plane is preferred, and circuit layout should be compact, with low capacitance around high-Z nodes. Signal and ground runs should be laid out with signal coupling and load current flow in mind.[3-6]

In addition, the power supplies should be well bypassed close to the high current supply pins. In Figure 8.39 this is indicated by the Kelvin connections of C_1-C_4 to the ±Vs pins of U1. This should be standard practice for all high current stages, and must be used for all the driver applications in this section.

As a minimum, local low inductance/low ESR RF bypass caps should used within 0.25" of the device supply pins, shown as C_1 and C_3. These are preferably 0.1µF ceramic or other low inductance capacitor type. In addition, for high peak current loads, the high frequency bypasses are paralleled by local, short lead/large value, low ESR electrolytics such as C_2 and C_4, in a range of 470µF/25V and up. Note that capacitor ESR reduces in inverse proportion to electrical size and voltage rating, so larger size and/or voltage units help. These capacitors carry transient output currents, and should be aluminum electrolytic types rated for high frequency use, that is switching supply ones. Such capacitors tend to have low Q, and are thus less likely to cause power line resonances than are tantalum capacitors.

DC power management and dissipation are important with buffer ICs. For example, the BUF-03 and the AD811 ICs can dissipate fairly large power levels even with light loading at supplies above ±12V, because the quiescent current of these devices is 15-18mA, relatively independent of operating voltage.

As a conservative rule of reliability, any IC with a power dissipation above 300mW should not be used without a heat sink. For buffer or driver circuits using more than 300mW, use the lowest thermal resistance package possible, and the appropriate heatsink (Thermalloy 2227 for the BUF-03 or other TO-99 ICs, or Aavid #5801 for the BUF-04, AD811 or other high dissipation 8 pin ICs).

Output resistor R_X in this circuit should be 10 ohms or more, to isolate the buffer from capacitive loading (more on this, below). For an extra safety margin against possible de- stabilization due to capacitive loads, make this resistor as high as practical. Input resistor R_1 is a "bullet-proof" parasitic suppression device, and may be required for stability with some amplifiers but it is not absolutely essential for those we have discussed.

Because of this stage's very high bandwidth, low phase shift, and low output impedance, fast buffers such as this can be used both "stand alone" just as shown, and as a more conventional "in loop" buffer as well, to minimize loading of a weaker, slower amplifier. For any modest output amplifier this is an obvious improvement, as raises the linear output to more than ±100mA (with the AD811 or the BUF-04), while maximizing linearity, preserving gain, and lowering distortion.

Operating in a pure stand-alone mode, THD+N tests on several buffers are

shown in Figure 8.40, for conditions of 10Vrms into a 600Ω load. The BUF-03, a design with no closed loop feedback path, shows a distortion for these conditions of about 0.15%. The BUF-04, a closed loop transimpedance design buffer, shows a very low distortion of about 0.004%. The AD811 transimpedance amplifier, externally configured as a unity gain follower with R_F = 1k, shows an intermediate level of distortion, just under 0.01%. As a choice among these types, both the BUF-04 and AD811 are capable of more than ±100mA of output, and have input currents on the order of 1-2μA. The BUF-03 has a lower maximum output current (±70mA), but the advantage of an input current on the order of 200pA.

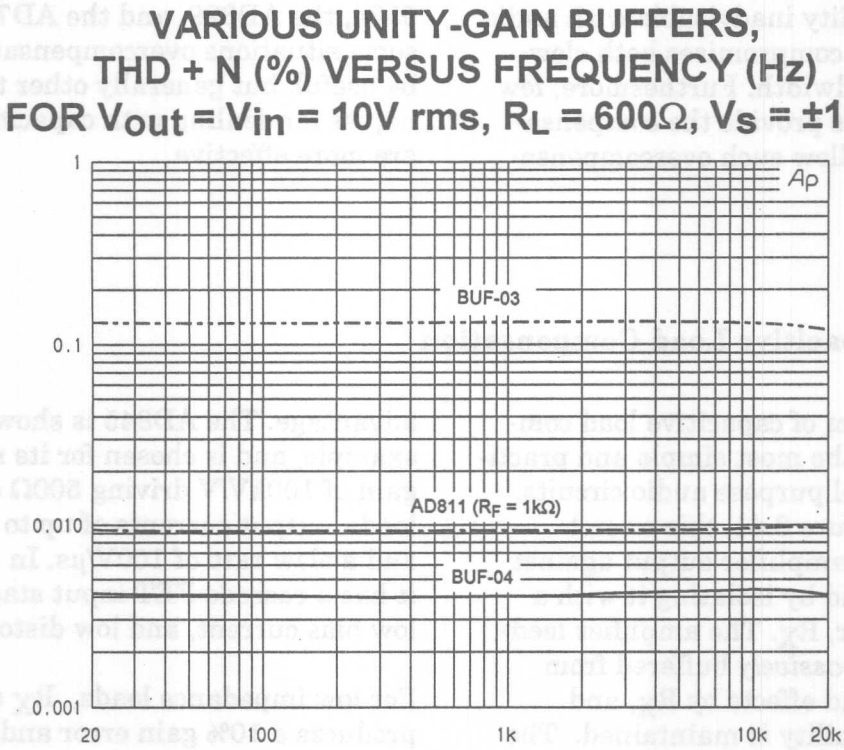


Figure 8.40

Capacitive Loading

Audio output/input stages are typically operated as voltage source drivers feeding high impedance loads. When connected with long transmission lines between stages, the result is that the driver sees an unterminated line, which can appear highly capacitive.

Audio driver stability with capacitive loading is not always easy to achieve. Fortunately, some standard techniques exist for stabilizing op amp drivers with capacitive loads, and these can be implemented in a reasonably direct fashion.

A good rule for any type of audio driver is that capacitive loading should be expected in any application, however benign it may seem. Signal trace ca-

pacitance can build up quickly, even on the same PC board, and particularly for long signal runs. "Off board" circuits at the end of short cable runs should be evaluated for capacitive loading much more carefully, with the capacitive loading characterized as well as possible. "Outside world" drivers where load capacitance is either poorly defined or undefined must be considered a worst case, and bullet-proofed accordingly with appropriate design techniques.

Overcompensation

Overcompensation of an op amp to achieve stability inadvisable with audio circuits, as it compromises both slew rate and bandwidth. Furthermore, few audio op amps provide the compensation pins to allow such overcompensation (some exceptions to this are the 5534, the AD829, and the AD744). In some situations overcompensation may be useful, but generally other techniques for dealing with capacitive loads are more effective.

Passive Capacitive Load Compensation

A passive form of capacitive load compensation is the most simple and practical for general purpose audio circuits. Shown in Figure 8.41, this circuit stabilizes an amplifier output against capacitive load by isolating it with a series resistor, R_X. The amplifier feedback loop is *passively* buffered from capacitive load effects by R_X, and amplifier stability is maintained. The series resistor R_X does cause a voltage drop proportional to load current, so for low impedance loads it must necessarily be low. Typical R_X values will lie in the range of 10-50Ω, which produce small but (usually) manageable power losses for loads of 500Ω or more.

Obviously, the choice of U1 buffer amplifier must be consistent with the load requirements, and generally the ability to drive high currents is an advantage. The AD845 is shown in this example, and is chosen for its minimum gain of 100kV/V driving 500Ω or higher loads, output currents of up to ±50mA, and a slew rate of 100V/µs. In addition, it has a cascode FET input stage with low bias current, and low distortion.

For low impedance loads, R_X at 50Ω produces a 10% gain error and a similar power loss. Gain accuracy also suffers, if the load is remote or its impedance is not known accurately.

If the load R_L is known and stable, then adding gain resistors R_F and R_{IN} can compensate for the gain loss caused by R_X. For this unity gain driver, when these resistors are matched in ratio to R_X/R_L, a nominal overall gain of 1 is restored.

PASSIVE CAPACITIVE LOAD ISOLATION USING ISOLATION RESISTOR, R_X

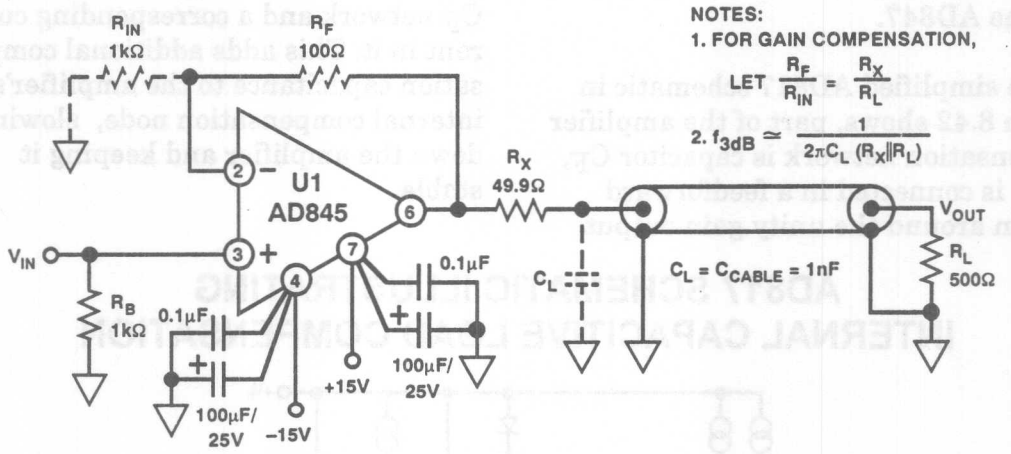


Figure 8.41

This capacitive load compensation technique is quite simple and can be effective, but it does have drawbacks. Already mentioned is loss of gain (or gain accuracy) and loss of output power, there is also loss of bandwidth for high values of load capacitance, and a possible loss of slew rate. For example, while the AD845 has a basic slew rate of 100V/μs, this falls to 50V/μs with C_L=1nF. In general the slew rate in this circuit will be limited to Io(max)/C_L V/s, when this figure is *smaller* than the intrinsic device slew rate (as is the case here).

The technique of Figure 8.41 is a general one, and is useful with any amplifier. High speed, high current devices will of course make best use of it for audio. The applications following show op amps generally suited for line driving use by virtue of their unusually high current output, low output resistance, and/or speed capabilities.

Internal Capacitive Load Compensation

An even simpler method of driving capacitive loads is to use an op amp which has an *internal* load compensation network. This is an amplifier design feature that makes capacitive loading virtually transparent to the user. It is used in a number of ADI op amps, including the AD817, the AD829, and the AD847.

As the simplified AD817 schematic in Figure 8.42 shows, part of the amplifier compensation network is capacitor C_F, which is connected in a feedforward fashion around the unity gain output stage. Under normal circuit operation with low capacitive loads this network is bootstrapped by the output stage, little voltage appears across it, and it has little effect on the output. With capacitive loading and large signals, current is drawn from the output stage, which causes a voltage drop across the C_F network and a corresponding current in it. This adds additional compensation capacitance to the amplifier's internal compensation node, slowing down the amplifier and keeping it stable.

AD817 SCHEMATIC ILLUSTRATING INTERNAL CAPACITIVE LOAD COMPENSATION

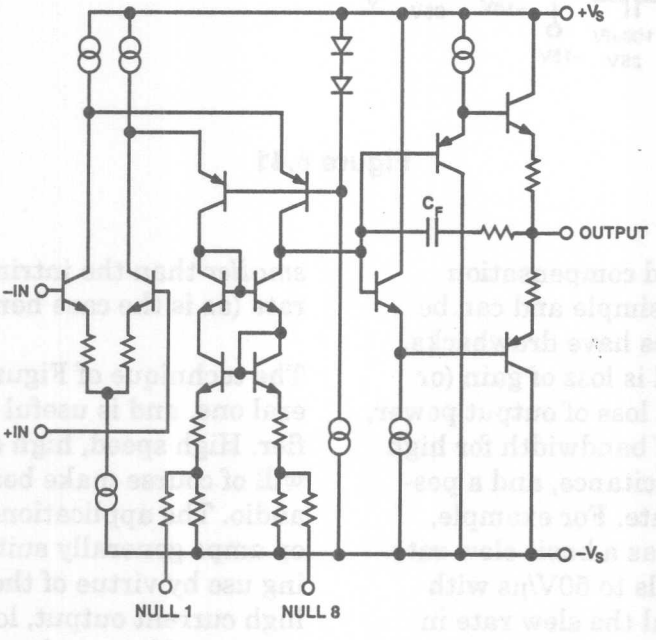


Figure 8.42

Like the passive form of capacitive load compensation, internal compensation causes in loss of bandwidth and slew rate. In addition it is signal dependent, having greater effect with large signals than small ones. It can also cause some distortion, since the amplifier bandwidth varies dynamically.

External "In Loop" Capacitive Load Compensation

External *in loop* compensation is the most flexible and accurate of the compensation techniques available for capacitive load isolation. It is flexible because it can, in principle, be applied to any unity gain stable op amp, whether it is operating in inverting or non-inverting mode. It is accurate because it includes the isolation resistance R_X within a DC feedback loop. This feature makes the low frequency gain accuracy as good as the resistors used (assuming adequate gain in the op amp). Its main problem is that it reduces bandwidth and slew rate, like the other techniques we have discussed.

The basic circuit illustrating operation is shown in Figure 8.43. It is a non-inverting stage with a gain of 2, where resistor R_X isolates the capacitive load C_L. While the circuit is similar to that in Figure 8.41, the resistive feedback is taken from the *load* side of R_X, automatically compensating for gain errors and loading. The basic gain expression is similar to that of a standard non-inverting op amp stage.

CAPACITIVE LOAD ISOLATION USING "IN-LOOP" COMPENSATION

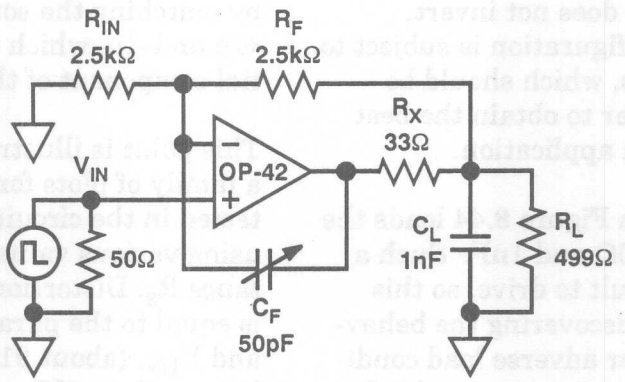


Figure 8.43

The capacitor C_F provides compensation for the additional lag introduced by C_L. C_F can be adjusted to cancel the effect of C_L and provide a well damped step response. This counters the tendency towards overshoot, ringing or oscillation caused by C_L, but it does not allow maximum bandwidth, as the closed loop bandwidth of the stage is still a function of R_X and C_L.

The value chosen for R_X is not critical, and the stage can be tuned with values in the range of 10-100Ω. R_X should not be excessively large, as this will degrade power output as well as bandwidth.

The optimum value for C_F is a function of R_X, C_L and the gain resistors, and with fixed values for R_F, R_{IN} and R_X, will track C_L. While several references suggest procedures for predicting C_F,[7,8] the best practical approach is to select a close nominal value for C_F, then adjust it for optimum pulse response *in the final circuit layout*.[9] This approach takes additional parasitic capacitances into account .

Low values of R_F/R_{IN} minimize sensitivity to stray capacitance. This will force C_F higher than 20pF and into a range of greater predictability and stability. C_F is best a composite of an NPO capacitor in parallel with an NPO trimmer. Alternately, it can be a single fixed value, once the optimum value has been verified in final layout.

Op Amp Device/Topology Related Distortions

Single-ended audio drivers can be built using Figure 8.41 as a starting point, and that circuit, with appropriate choice of op amp and gain can well serve as a basic audio driver. The non- inverting gain stage architecture is preferable for a line driver, since it loads the signal source less, and it does not invert. However, this configuration is subject to certain distortions, which should be understood in order to obtain the best performance in an application.

The test circuit in Figure 8.44 loads the amplifier with 500Ω and 1nF. Such a load is quite difficult to drive, so this test is useful for discovering the behavior of devices under adverse load conditions. By programming a gain of 2 the test ensures the presence of sufficient common-mode voltage to test for common-mode related distortion as well. The tests are conducted with ±18 V supplies and an analyzer bandwidth of 10 Hz-80kHz. We find that amplifiers with linear output stages and high drive capability may still exhibit nonlinearity in this test, due to the nonlinear C/V characteristics of the amplifier inputs. The effect can be minimized by matching the source impedances at +In and -In, which reduces the differential component of this error.

This point is illustrated by Figure 8.45, a family of plots for the OP-275 op amp tested in the circuit of Figure 8.44, using various values of source resistance R_S. Distortion is lowest when R_S is equal to the parallel equivalent of R_F and R_{IN}, (about 910Ω). For higher or lower values of R_S, distortion rises. Appreciably higher source impedance (10kΩ) can cause the distortion to occur at lower frequencies, making performance much worse overall.

TEST CIRCUIT FOR LINE DRIVER AMPLIFIERS

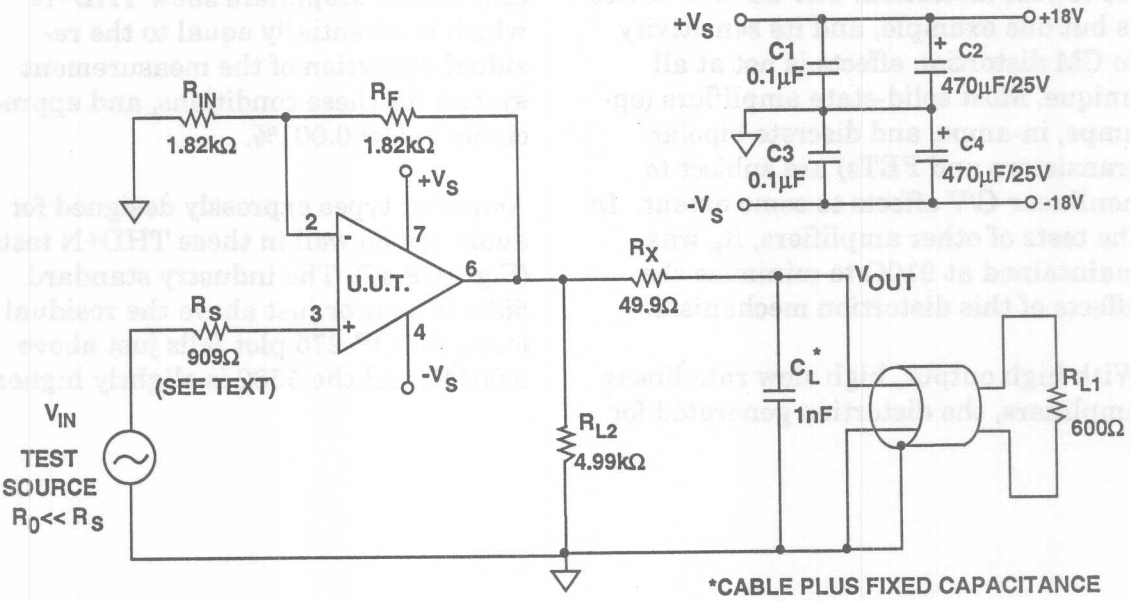


Figure 8.44

FOLLOWER MODE R_S SENSITIVITY: OP-275
THD + N (%) VERSUS FREQUENCY (Hz) FOR
V_{out} = 7V rms, R_S = 910Ω, 100Ω, 10kΩ, R_L = 500Ω, V_S = ±18V

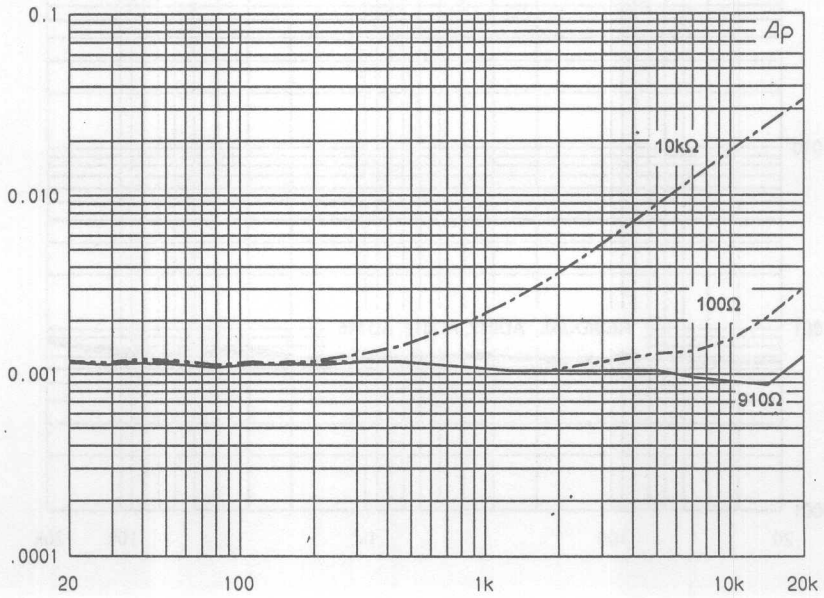


Figure 8.45

Whenever possible, amplifiers which operate as voltage followers should have their source impedances balanced for lowest distortion. The OP-275 device is but one example, and its sensitivity to CM distortion effects is not at all unique. Most solid-state amplifiers (op-amps, in-amps, and discrete bipolar transistors and FETs) are subject to nonlinear C/V effects to some extent. In the tests of other amplifiers, R_S was maintained at 910Ω to minimize the effects of this distortion mechanism.

With high output, high slew rate linear amplifiers, the distortion generated for these test conditions can be comparable to the distortion of the test equipment (Figure 8.46). Here the AD817, AD818 and AD845 amplifiers show THD+N which is essentially equal to the residual distortion of the measurement system for these conditions, and appreciably below 0.001%.

Amplifier types expressly designed for audio use do well in these THD+N tests, (Figure 8.47). The industry standard 5534 is near or just above the residual level, the OP-275 plot falls just above 0.001%, and the 5532 is slightly higher.

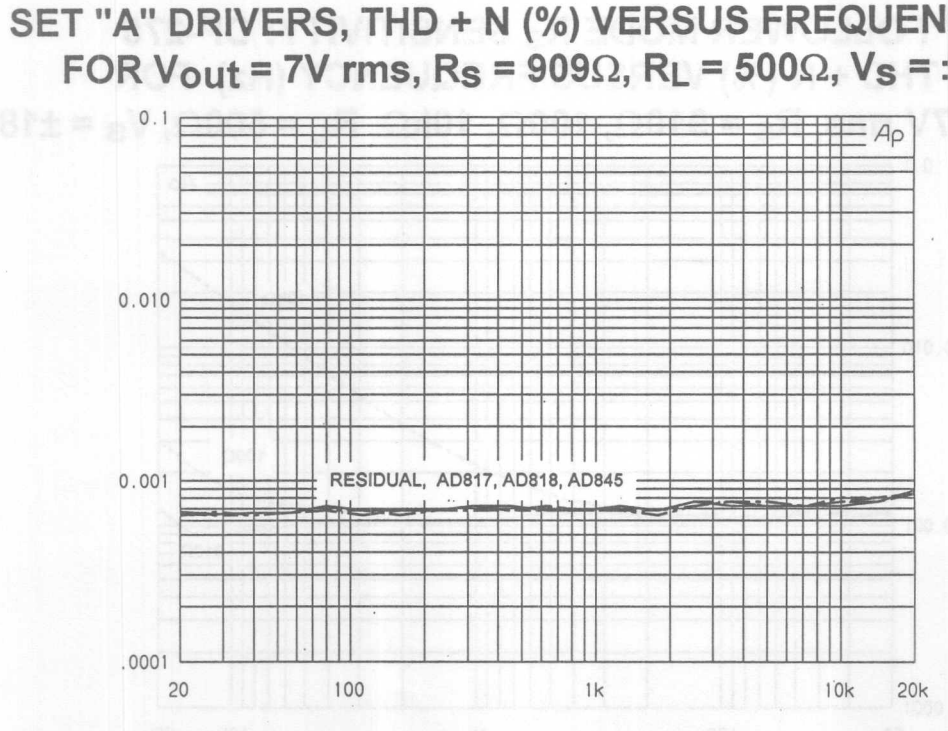


Figure 8.46

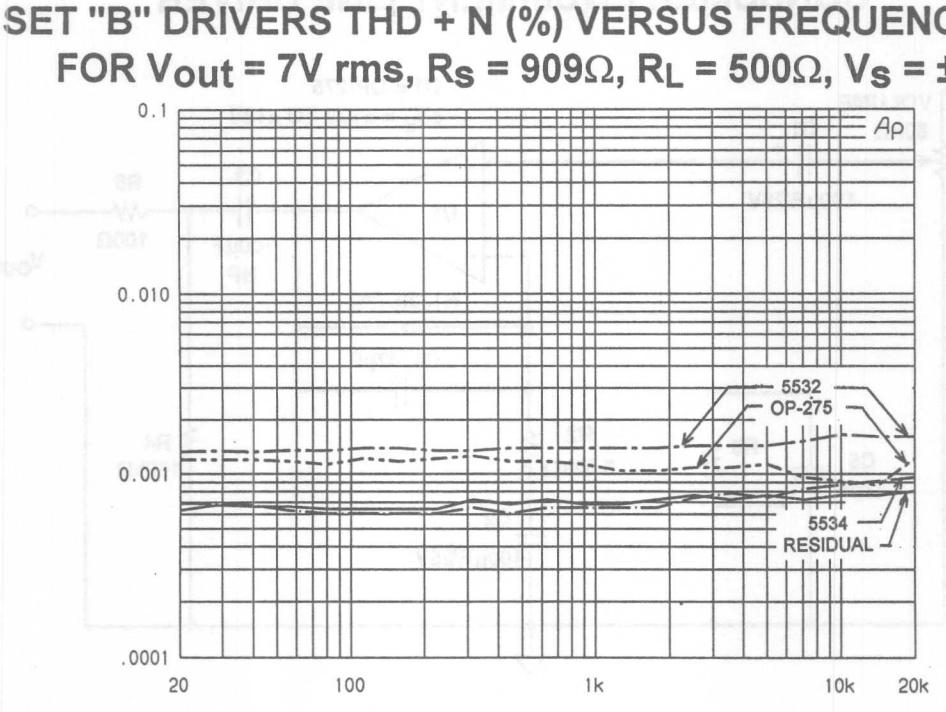


Figure 8.47

SINGLE-ENDED LINE DRIVERS

This section discusses a variety of line drivers which drive single-ended lines, optimized for different environments.

Consumer Equipment Line Driver

One common driver application is a line output stage for consumer preamps, CD players, etc. This is an economical stage with a nominal gain of 5 to 10 times operating from supplies of ±10V to ±18V, with a rated output of 2-3Vrms driving loads of 10kΩ or more. For simplicity of biasing and minimum output DC offset, AC coupling is used, and the circuit is often fed from a volume control. Such a stage is shown in Figure 8.48, using an OP-275 op amp as the gain element.

CONSUMER EQUIPMENT LINE DRIVER

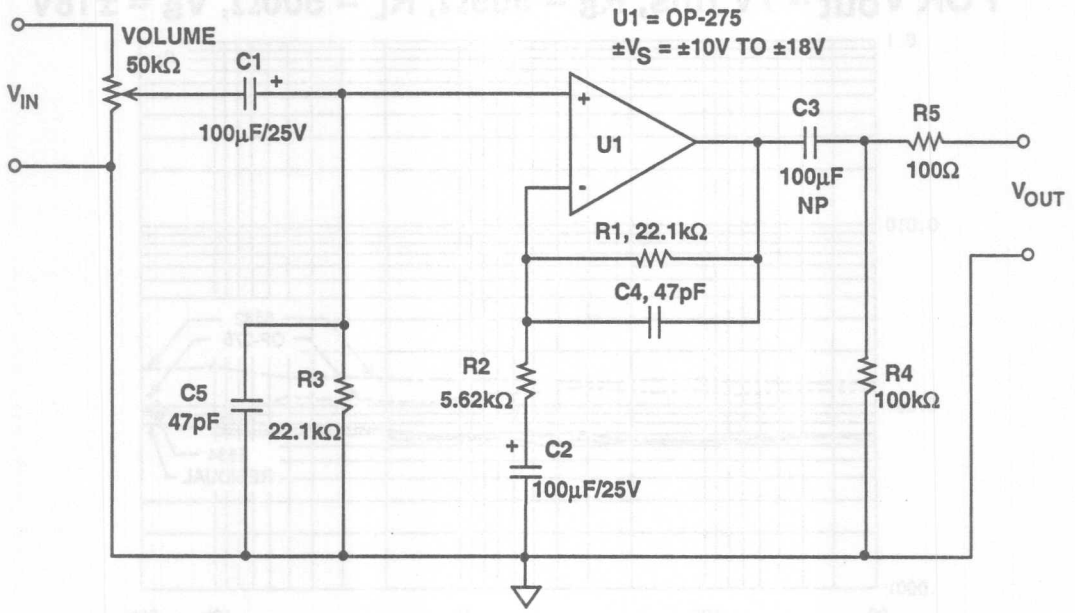


Figure 8.48

In this circuit input and feedback resistors R_1 and R_3 are made equal, so the nominal DC bias at U1's output is zero. The U1 bias current flowing in these resistors polarizes coupling capacitors C_1 and C_2. The OP-275 has PNP input transistors, so this bias is positive. If the OP-275 is replaced with an amplifier with NPN input transistors, the polarity will be reversed and the polarity of C_1 and C_2 should also be reversed. R_1 and R_2 set the stage gain (nominally 5). R_2 and C_2 set the LF rolloff at 0.3 Hz. This allows the gain to be increased by reducing R_2 without changing C_2. The output capacitor, C_3, must be non-polar, since the output offset may be of either polarity. If the output can tolerate a DC offset of ±10 mV (max - typical value is ±2.5mV), C_3 may be omitted.

THD+N performance of the stage is shown in Figure 8.49 for outputs of 1, 2, and 3Vrms into a 10kΩ/600pF load, using ±18V supplies with an R_S of 1kΩ. At lower output levels performance is noise limited, while at a 3V output level there is a slight increase in high frequency distortion. Although this application is an example of a circuit where the amplifier source impedances cannot be perfectly matched (due to variations of the volume control), performance is still good.

CONSUMER EQUIPMENT LINE DRIVER
THD + N (%) VERSUS FREQUENCY (Hz)
FOR V_{out} = 1, 2, 3V rms, R_L = 10kΩ/600pF, V_S = ±18V

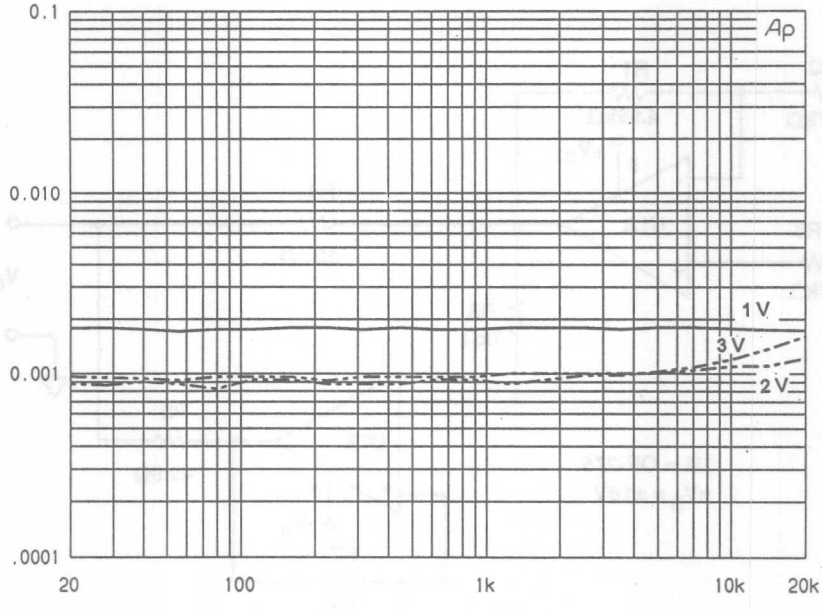


Figure 8.49

Noise is the limiting factor for lower level signals, and if lower noise is required, R_2 can be reduced. The practical limit to noise is the volume control's finite output resistance which causes higher noise at high output resistance, because of interaction with the noise current from U1. If the effective R_S at the volume control is 10kΩ, a 1.2pA/√Hz noise current from U1 will produce an input referred 12nV/√Hz noise voltage.

The driver stage of Figure 8.48 is flexible, and also operates at supplies as low as ±10V with outputs up to 3Vrms, with a slight distortion increase. At ±5V, outputs up to 2Vrms are possible, but with distortion still higher but remaining ≤0.01%.

Paralleled Output Line Driver

Often a modest increase in output may be needed from a driver, but circumstances may not warrant the use of an additional buffer. Figure 8.50 shows how the second section of a dual op amp can be used to provide additional load drive. In this circuit, the U1A section is an × 5 voltage amplifier, while U1B is a voltage follower, used simply to provide additional current to the load. Current sharing between the amplifier stages is determined by output resistors R_4 and R_5, and the composite stage drives 600Ω loads with lower distortion than a single OP-275 section. THD+N data is shown in Figure 8.51 operating from ±18V supplies, and for output levels of 1, 2, 5, and 9Vrms into 600Ω.

PARALLELED OUTPUT LINE DRIVER

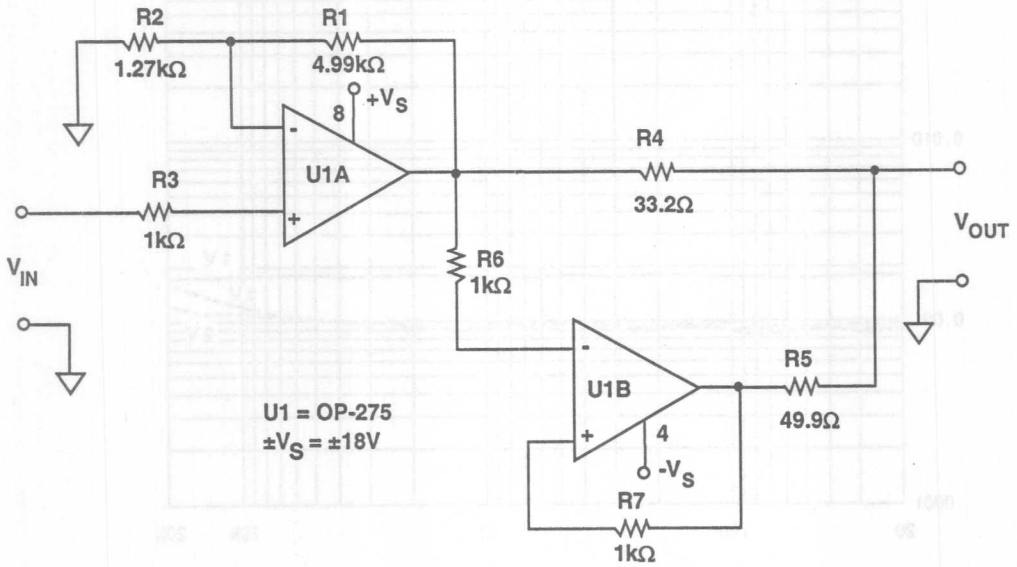


Figure 8.50

PARALLELED OUTPUT LINE DRIVER
THD + N (%) VERSUS FREQUENCY (Hz)
FOR Vout = 1, 2, 5, 9V rms, R_L = 600Ω, Vs = ±18V

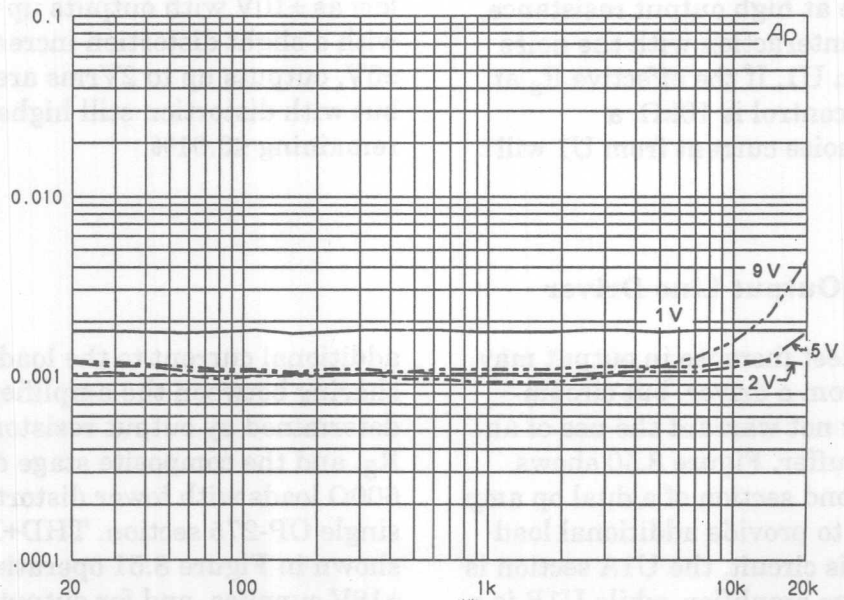


Figure 8.51

This scheme can be used with any unity gain stable dual op amp and various gain levels. For different devices and gains the ratio of R_4 and R_5 may need adjustment for lowest distortion into the load.

A WIDE DYNAMIC RANGE ULTRA LOW DISTORTION DRIVER

Single-ended line drivers may seem simple, but when both high dynamic range and low noise and distortion are necessary, it is difficult to choose a suitable amplifier.

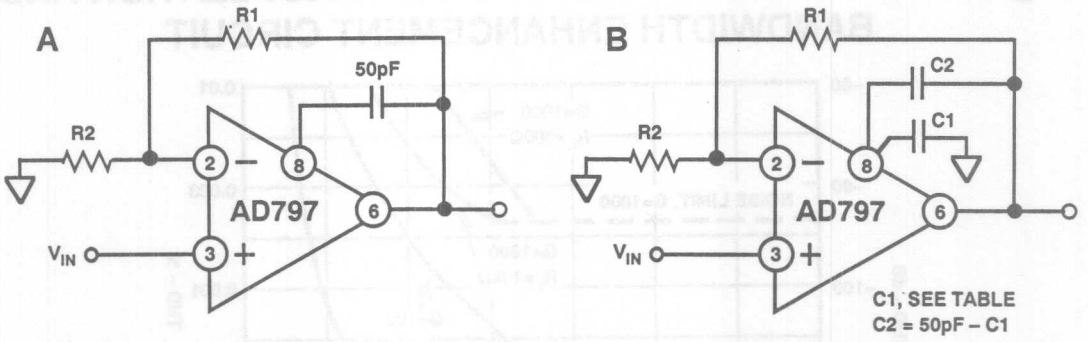
The AD797 has very low input noise of <1 nV/√Hz and a distortion cancelling output stage, and is exceptionally well-suited to line driver applications.[11]

The AD797 has a single voltage gain stage, which consists of a folded cascode input and a bootstrapped (and therefore very high impedance) current mirror load. The combination has a gain of about 146 dB. Using a single stage allows improvements in bandwidth, phase margin, settling time, and noise over more conventional two-stage op-amps.

The AD797 is used like any other 5 pin op amp (Figure 8.52). Low values for gain resistors R_1-R_2 are recommended for best noise, and selecting these resistors should be done with care, as values ≥100Ω will limit noise performance. Suggested values for gains of 10-1000 times are noted in the "A/B" column of the table in Figure 8.52. The AD797 can drive loads of up to 50mA, and is specified for distortion when driving loads of 600Ω.

8

AD797 RECOMMENDED CONNECTIONS FOR DISTORTION CANCELLATION AND BANDWIDTH ENHANCEMENT



	A / B		A			B		
	R1 Ω	R2 Ω	C1 pF	C2 pF	3dB BW	C1 pF	C2 pF	3dB BW
G=10	909	100	0	50	6 MHz	0	50	6 MHz
G=100	1k	10	0	50	1 MHz	15	33	1.5 MHz
G=1000	10k	10	0	50	110 kHz	33	15	450 kHz

Figure 8.52

For amplifier applications requiring the best possible distortion, the capacitors C_1 and C_2 should be used. The single 50 pF capacitor, C_2, in Figure 8.52A compensates for output stage distortion without affecting forward gain.

At higher gains a second capacitor, C_1, from the compensation node to ground, enhances open-loop bandwidth and improves high frequency performance by "decompensating" the amplifier and increasing its gain-bandwidth product (Figure 8.52B). The effects of C_2, and C_1 and C_2, are summarized in the table.

A family of distortion curves for various AD797 gain configurations driving 600Ω is shown in Figure 8.53. At low frequencies the noise is far greater than the distortion, which cannot be measured. At high frequencies distortion is measurable, but still extremely low. The distortion for a gain of 10 times at 20kHz for example, is ≈0.0001%, implying a dynamic range of 120dB referenced to 3Vrms, and even more at higher level signals.

TOTAL HARMONIC DISTORTION (THD) VERSUS FREQUENCY @ 3V rms FOR AD797 DISTORTION CANCELLATION AND BANDWIDTH ENHANCEMENT CIRCUIT

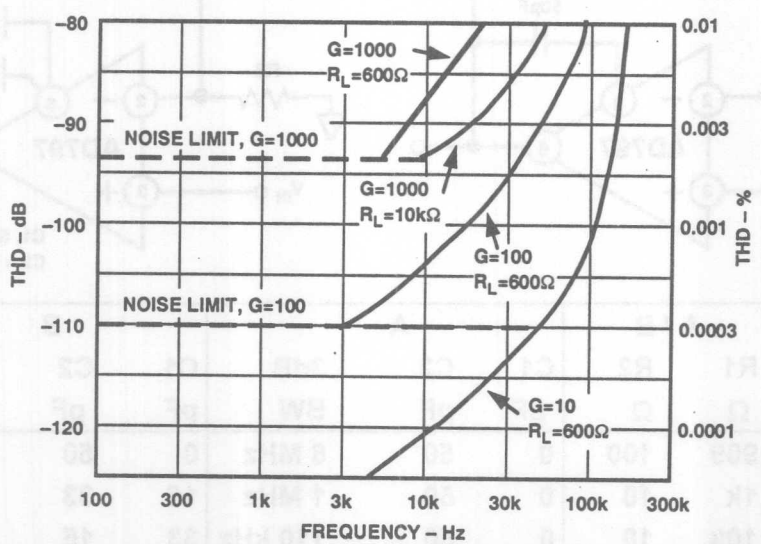


Figure 8.53

Current Boosted Line Drivers

When a driver must drive loads of less than 600 Ω, it is unlikely that an op-amp can handle the task unaided. In such cases a current-boosted design allows loads down to 150 Ω.

Figure 8.54 is an example of a high quality current boosted driver. It uses an AD845 as a gain stage and voltage driver, and a unity gain current booster. The overall voltage gain is × 5 , but may easily be modified by R_1/R_2. For lowest CM distortion, R_3 is set equal to $R_1 \mid\mid R_2$.

The amplifier used for U2 may be either the AD811 op amp, or the BUF-04 buffer. The AD811 op amp is configured as a follower, with R_5 connected as shown. The BUF-04 is internally connected as a follower. In either case, both the U1 and U2 devices *must* have a heat sink, and be used with supplies of ±17V or less. As usual, the power supplies must be well bypassed.

For loads of 150Ω, the series isolation resistor R_4 is only to 22.1Ω, to minimize power loss and to allow levels of 7Vrms or more. The THD+N data for this circuit is shown in Figure 8.55 and Figure 8.56 respectively, using the AD811 and BUF-04 as the U2 buffer. The test conditions are successive input sweeps resulting in 1, 2, 4 and 8Vrms out. The test power supplies are exactly ±18 V. *Production versions of this circuit, where the power supplies will be less accurately defined, should use nominal supplies no greater than ±17 V.*

CURRENT BOOSTED LINE DRIVER

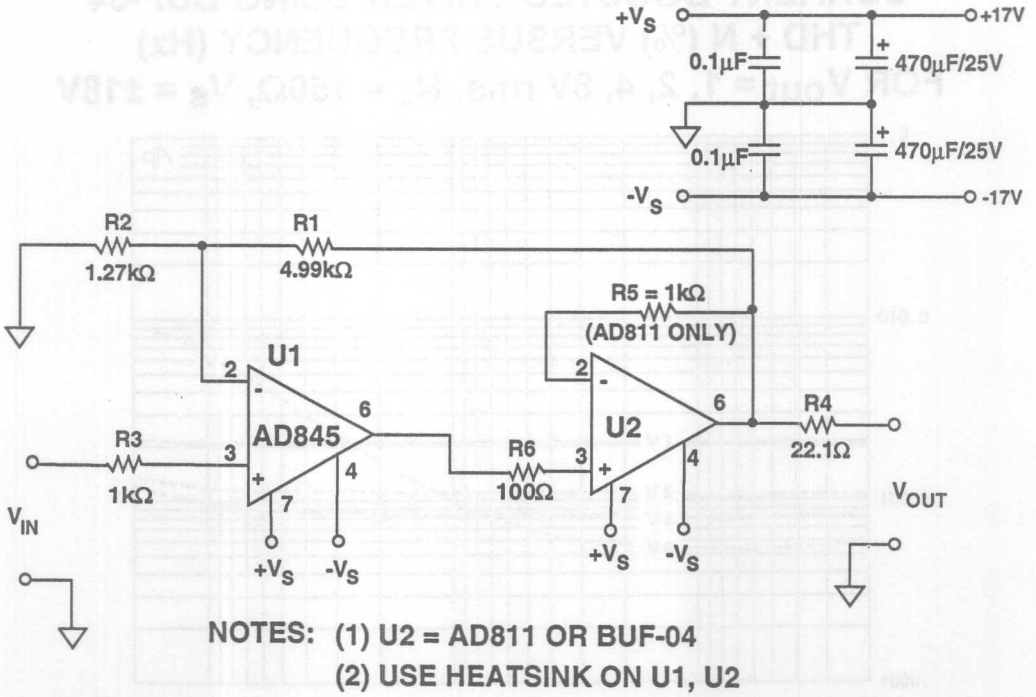


Figure 8.54

CURRENT BOOSTED DRIVER USING AD811
THD + N (%) VERSUS FREQUENCY (Hz)
FOR V_{out} = 1, 2, 4, 8V rms, R_L = 150Ω, V_S = ±18V

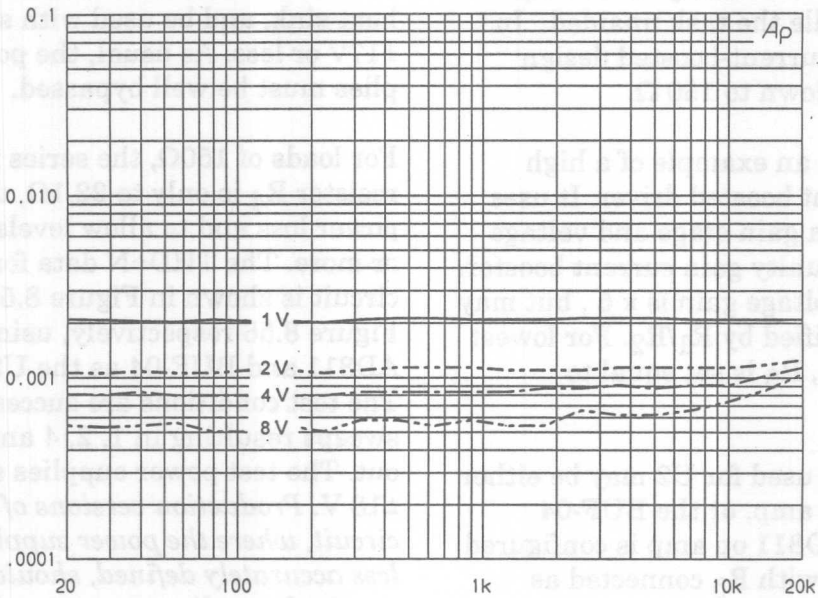


Figure 8.55

CURRENT BOOSTED DRIVER USING BUF-04
THD + N (%) VERSUS FREQUENCY (Hz)
FOR V_{out} = 1, 2, 4, 8V rms, R_L = 150Ω, V_S = ±18V

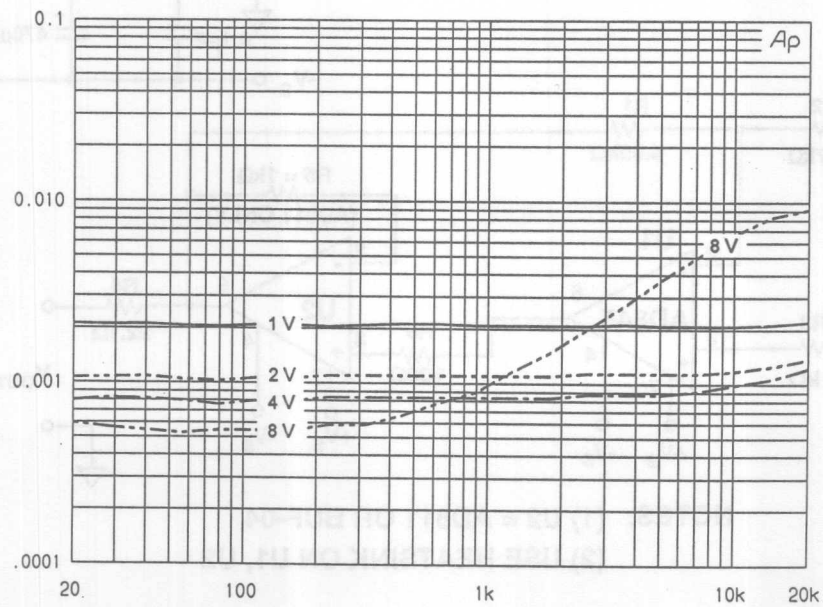


Figure 8.56

For the AD811 buffer, the data of Figure 8.55 shows THD+N dominated by noise and residual distortion at nearly all levels and frequencies while driving 150Ω. A very slight rise in distortion is noted above 10kHz, yet it is still ≈0.001%. The BUF-04 (Figure 8.56) is nearly as good at low output levels, but shows some distortion increase at the 8Vrms output at higher frequencies.

There is a tradeoff involved in the choice between these two devices. The BUF-04 has a standby dissipation of about 300mW, while the AD811 has nearly double this dissipation, 560mW. So while the AD811 yields lower distortion, it must be operated more conservatively. Only the minimum supply voltage required to sustain a given output should be used.

Variants of this circuit technique will be found in later parts of this section in other driver applications.

A Composite Current Boosted Driver

Another useful current-boosted circuit technique combines the best features of two different amplifiers into a single composite structure, producing a very high performance line driver.[12,13] With an FET input IC as the input stage, there is no noticeable dc offset change from source resistance variations of a typical volume control, allowing dc coupling. A high current, wide band current booster output stage drives line impedances down to 150Ω with excellent linearity.

A composite amplifier allows the best features of two dissimilar ICs to be exploited. Figure 8.57 shows a low distortion composite amplifier using two amplifier ICs.

A factor which aids performance is that U1 operates unloaded, and the compensation pin (5) drives U2. This removes possible U1 output stage distortion. The overall gain bandwidth and slew rate of U1 are boosted by the voltage gain of U2, an AD811. The AD811 is used for its ±150mA(max) output current.

The circuit has an overall gain of 5, set by R_1 and R_2. The gain of the output stage, which is set by R_3 and R_4, should be

$$\left[\frac{\text{Overall Gain}}{2} - 1\right].$$

As the AD811 is a transimpedance amplifier, there is an optimum value for R_3, which should be used, and the gain varied with R_4. Further design details are available in Reference 12.

The composite amplifier performance is remarkable for its modest complexity. For a typical audio load of 600Ω, THD+N at output levels of 1, 2, 4 and 8Vrms is shown in Figure 8.58. Distortion is only visible above the noise at the higher frequencies.The circuit will drive low impedance loads down to 150 Ω . At supply voltages above ±12 V, U2 requires a heat sink.

COMPOSITE CURRENT BOOSTED LINE AMPLIFIER

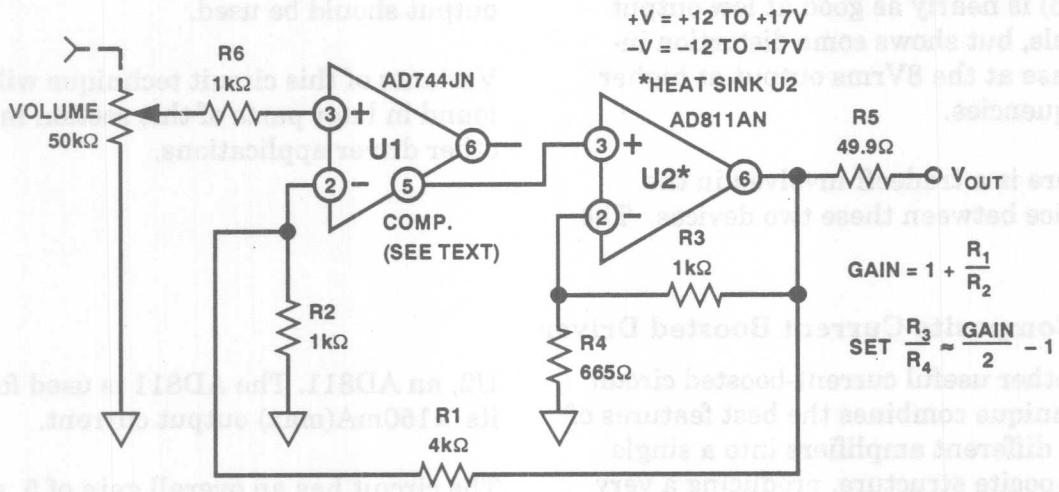


Figure 8.57

COMPOSITE CURRENT BOOSTED DRIVER THD + N (%) VERSUS FREQUENCY (Hz) FOR V_{out} = 1, 2, 4, 8V rms, R_L = 600Ω, V_S = ±18V

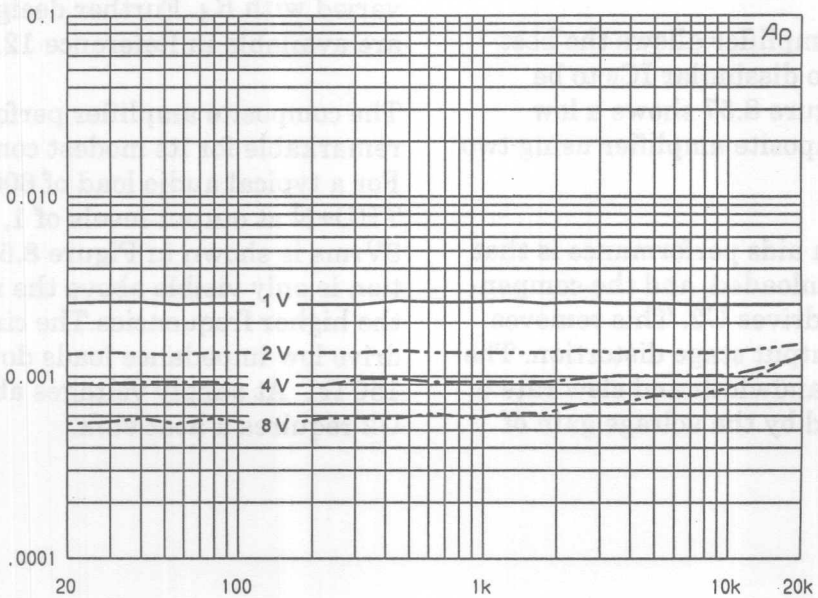


Figure 8.58

Differential Line Drivers

Standard circuits for line drivers are not nearly as well-defined as standard circuits for line receivers. This section discusses a variety of possible circuits, varying greatly in complexity and performance.

"Inverter-Follower" Differential Line Driver

A straightforward approach to developing a differential drive signal of $2V_{IN}$ is to amplify in complementary fashion a single-ended input V_{IN}, with equal gain inverter/follower op amps. With op amp gains of ±1, this develops outputs $-V_{IN}$ and $+V_{IN}$ with respect to common, or $V_{OUT} = 2V_{IN}$ differentially. V_{OUT} can be scaled further, but gains < ±1 are less practical.

This "inverter/follower" driver is easily built with a dual op amp such as the OP-275 and one 8x20k film resistor network (Figure 8.59). Here U1A provides the gain of -1, while U1B operates at a gain of +1. The differential output signal across the balanced output line is $2V_{IN}$, and the differential output impedance is equal to $R_A + R_B$, or 100Ω.

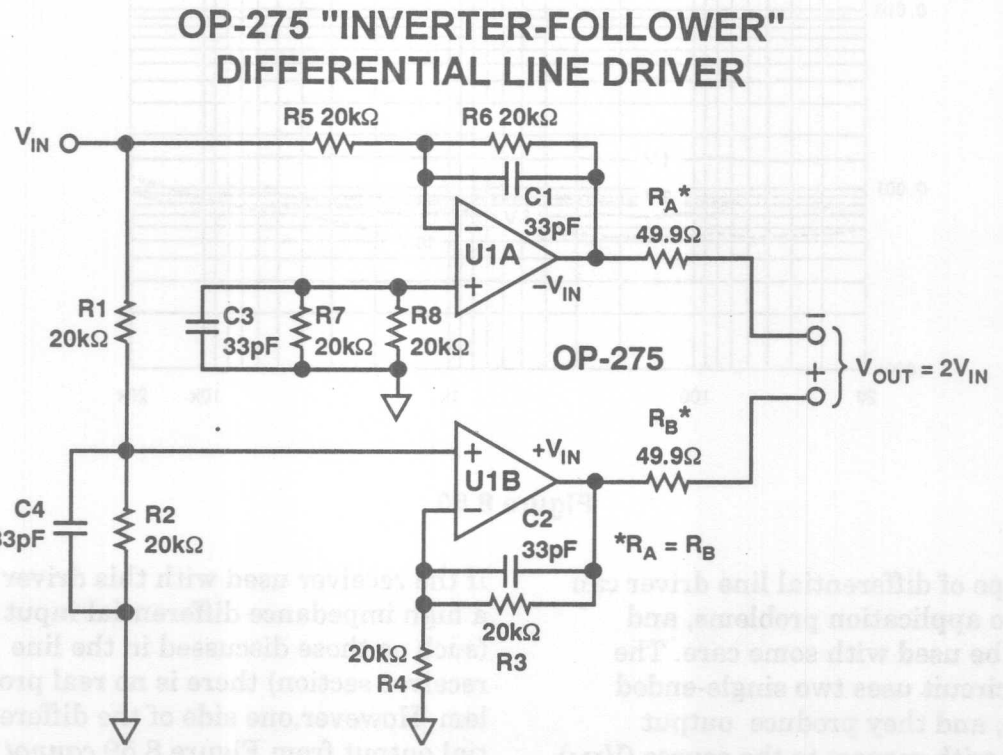


Figure 8.59

Use of similar values for gain resistors around the two amplifiers matches the channel noise gains, and makes the network easy to obtain. It also matches the source impedances seen by the op amp inputs. Capacitors C_1-C_2 provide HF rolloff, and enhance stability when driving capacitive lines. This circuit has high performance for its cost and simplicity. If a resistor network is used for R_1-R_7, it can be built with only 6 components.

THD+N performance of this circuit is shown in Figure 8.60. The distortion is about 0.001%, and somewhat higher at 1V output level (noise limited). Maximum output level is about 12Vrms into 600Ω before clipping.

OP-275 "INVERTER-FOLLOWER" DIFFERENTIAL DRIVER
THD + N (%) VERSUS FREQUENCY (Hz)
FOR V_{out} = 1, 2, 5, 10V rms, R_L = 600Ω, V_S = ±18V

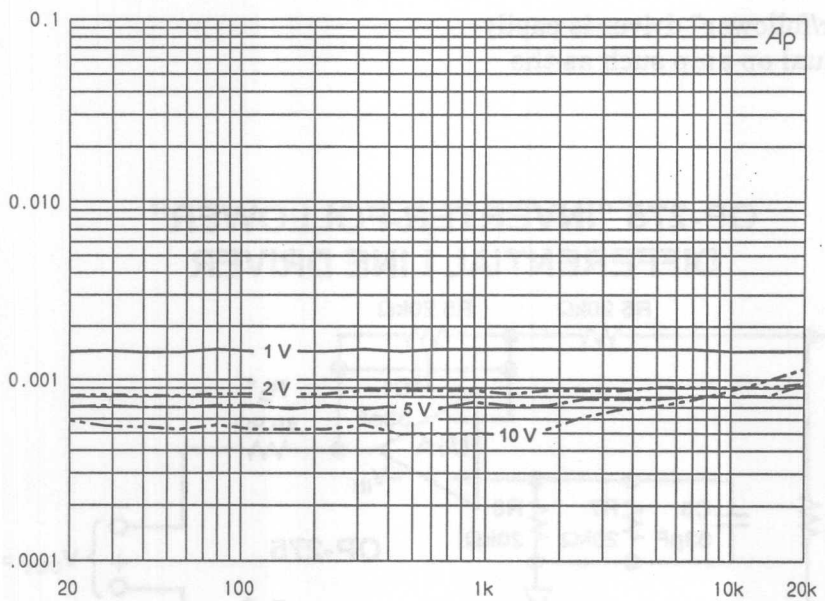


Figure 8.60

This type of differential line driver can run into application problems, and should be used with some care. The driver circuit uses two single-ended drivers, and they produce output signals with respect to the source (V_{IN}) common point.

If the receiver used with this driver has a high impedance differential input (such as those discussed in the line receiver section) there is no real problem. However,one side of the differential output from Figure 8.59 *cannot be grounded without side effect*. This is

because the source drive V_{OUT} is *not* floating.

In this sense, the circuit is *pseudo differential*, and it should not be used indiscriminately. Nevertheless, within small and well defined systems, it has the obvious advantage of simplicity and can achieve high performance. With the matched sources R_A and R_B of 49.9Ω there will be no damage even if one output is shorted, but half the signal will be lost.

Cross-Coupled Differential Line Driver

A more sophisticated form of differential line driver uses a pair of *cross-coupled* op amps with both positive and negative feedback paths. The general form of this type of circuit is a cross-coupled *Howland* circuit, named after the inventor of the classic resistor bridge current pump. The cross-coupled form was described by Pontis in a solid-state transformer emulator for high performance instrumentation.[14]

This configuration provides maximum flexibility, allowing a differential output signal V_{OUT} to be maintained independent of the load common connections. This means that either side can be shorted to common, as with a transformer.

Figure 8.61 shows the SSM-2142 balanced line driver IC use. The SSM-2142 consists of two cross-coupled Howland circuits, plus an input buffer. The trimmed multiple resistor array and three op amps are packaged in an 8 pin miniDIP IC.

8

SSM-2142 CROSS-COUPLED DIFFERENTIAL LINE DRIVER USED IN BALANCED DRIVER / RECEIVER SYSTEM

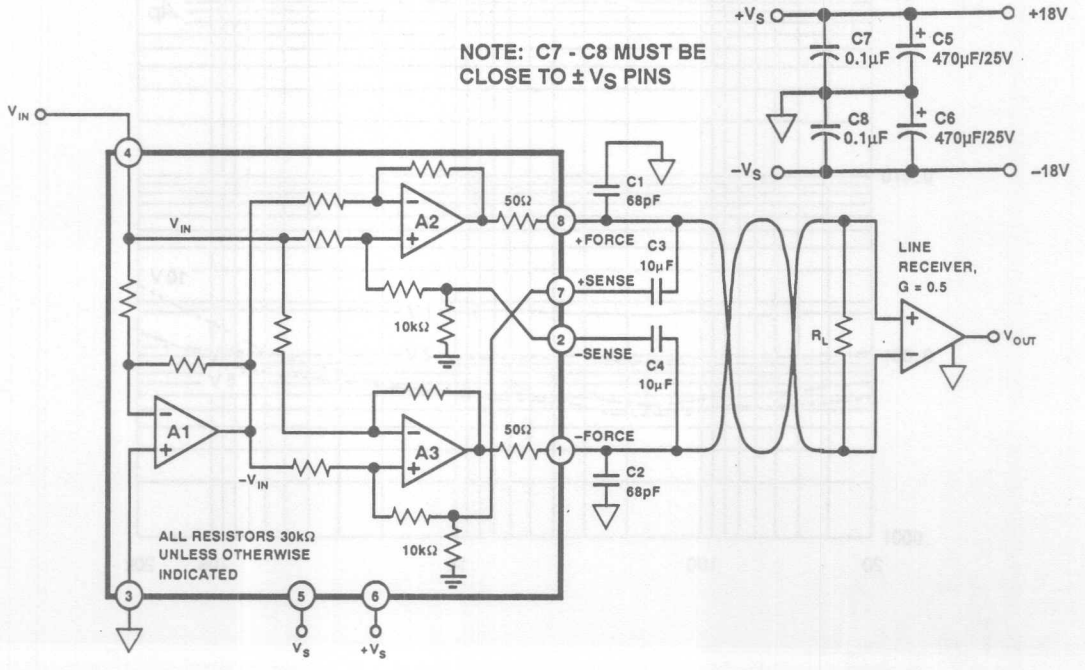


Figure 8.61

The SSM-2142 line driver is designed for a single-ended to differential gain of 2 and will drive a 600Ω load. In the simplest use, it is simply strapped with the respective output FORCE/SENSE pins tied together (7-8, 1-2). Small film capacitors C_1-C_2 preload the IC for stability against varying cable lengths. To decouple line dc offsets, the optional capacitors C_3-C_4 are used, which should be non-polar types, preferably films. The 0.1μF low inductance bypass caps C_7 & C_8 must be within 0.25" of power supply pins 5 and 6 as long lead lengths will cause excessive THD.

In a system application, the SSM-2142 is used with a gain of 0.5 receiver, either an SSM-2143, or one of the other line receivers discussed previously. The system shown in Figure 8.61 comprises an entire single-ended to differential and back to single-ended transmission system, with noise isolation, and net unity gain.

Figure 8.62 shows the THD+N performance of the SSM-2142 driver portion of Figure 8.61. Performance is noise limited for the 1V output curve, and distortion drops to ≤0.001% for higher levels, rising with higher frequencies and at 10V output.

SSM-2142 CROSS-COUPLED DIFFERENTIAL DRIVER
THD + N (%) VERSUS FREQUENCY (Hz)
FOR V_{out} = 1, 2, 5, 10V rms, R_L = 600Ω, V_S = ±18V

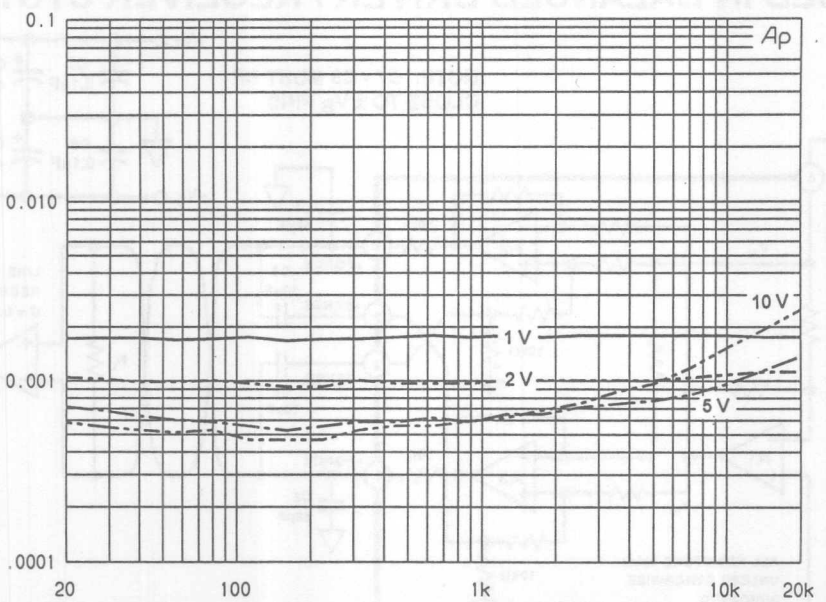


Figure 8.62

Transformer Coupled Line Driver

Transformers provide a unique method of signal coupling, which allows complete common-mode isolation. As noted in the section on line receivers, transformers are not without their technical and practical limitations, but their singular ability to galvanically isolate grounds maintains a place for them in difficult applications.[15,16]

The circuit of Figure 8.63 is a low DC offset, high linearity driver circuit using a high quality nickel core output transformer. U1 and U2 form a high current driver, similar to the current boosted driver of Figure 8.54.

In this circuit U1 is selected as a low bias current, low offset voltage FET input op amp, in order to hold the DC offset at the primary of T1 to a minimum (less than ±15mV). The DC current flowing into the primary winding of a transformer should be minimized, in order to minimize distortion. At the input to U1, C_1 (a high quality film capacitor) decouples any DC offset present on the signal input V_{IN}.

The U1-U2 device combination is capable of providing ±100mA or more, which allows this circuit to drive low impedances. Although T1 is shown with a 1:1 ratio, other winding configurations are possible, allowing the circuit to drive a wide range of load resistances.

TRANSFORMER COUPLED LINE DRIVER

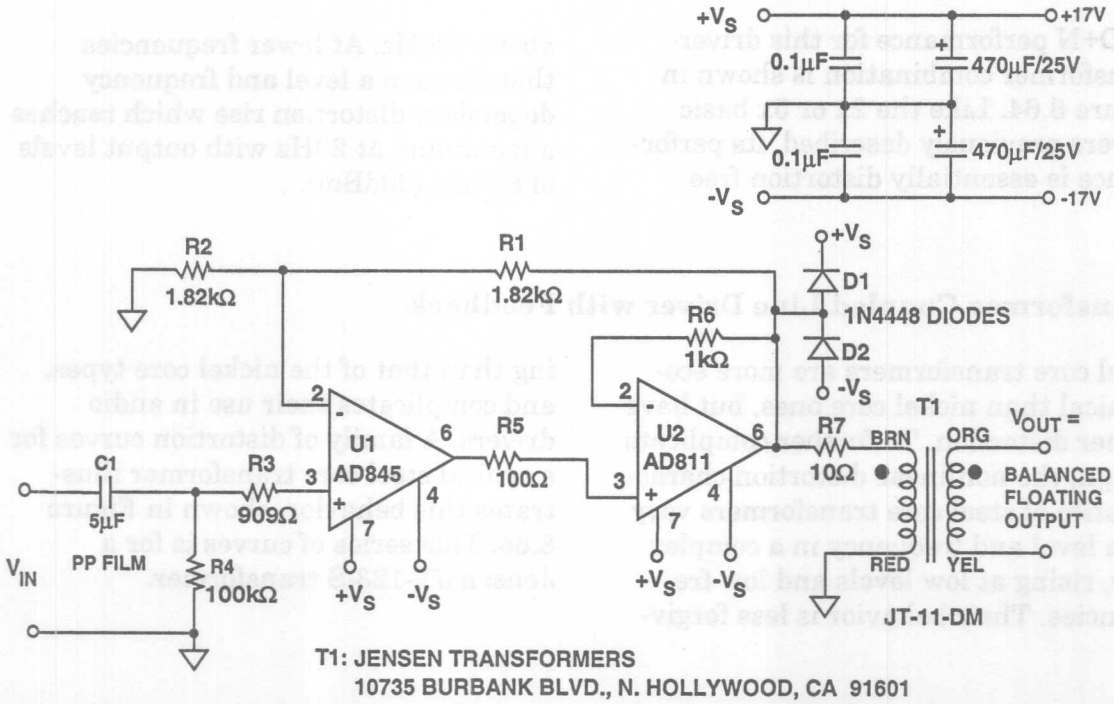


Figure 8.63

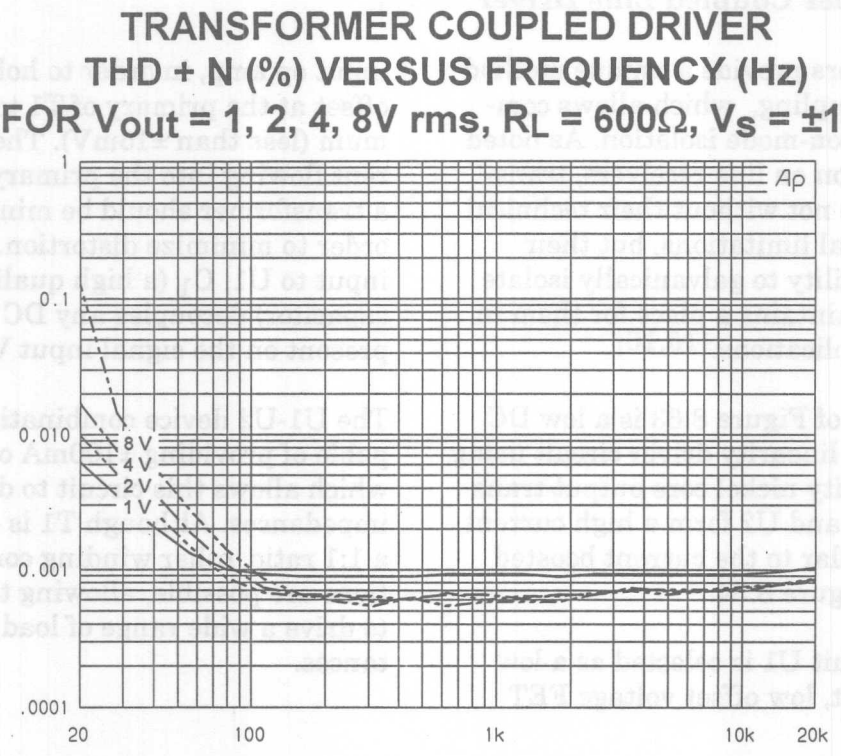


Figure 8.64

THD+N performance for this driver-transformer combination is shown in Figure 8.64. Like the 2x or 5x basic drivers previously described, its performance is essentially distortion free above 100Hz. At lower frequencies there is seen a level and frequency dependent distortion rise which reaches a maximum at 20Hz with output levels of 8Vrms (20dBm).

Transformer Coupled Line Driver with Feedback

Steel core transformers are more economical than nickel core ones, but have higher distortion. To further complicate design, the nonlinear distortion characteristics of steel core transformers vary with level and frequency in a complex way, rising at low levels and low frequencies. Their behavior is less forgiving than that of the nickel core types, and complicates their use in audio drivers. A family of distortion curves for a typical steel core transformer illustrates this behavior, shown in Figure 8.65. This series of curves is for a Jensen JT-123-S transformer.

STEEL CORE TRANSFORMER
THD + N (%) VERSUS FREQUENCY (Hz)
FOR V_{out} = 5, 2, 1, 0.5V rms, R_L = 600Ω

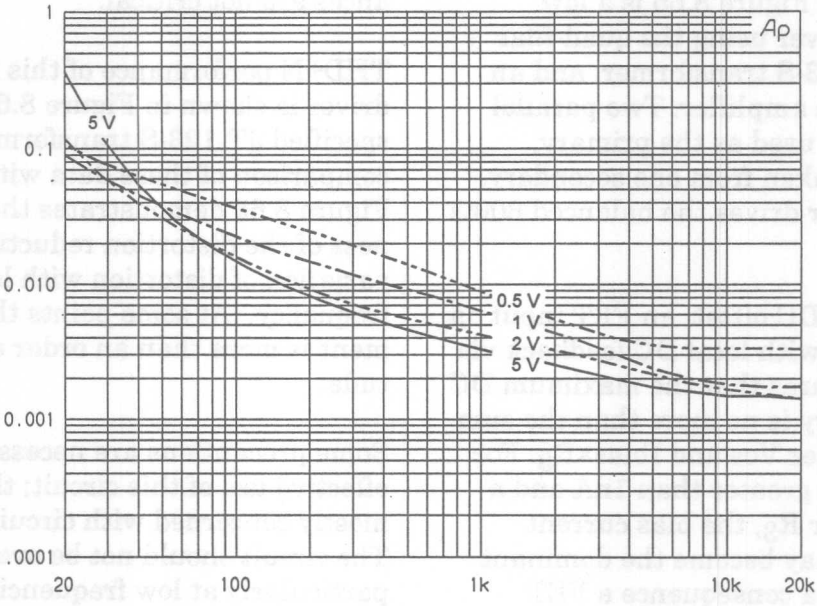


Figure 8.65

TRANSFORMER COUPLED LINE DRIVER
WITH TERTIARY FEEDBACK

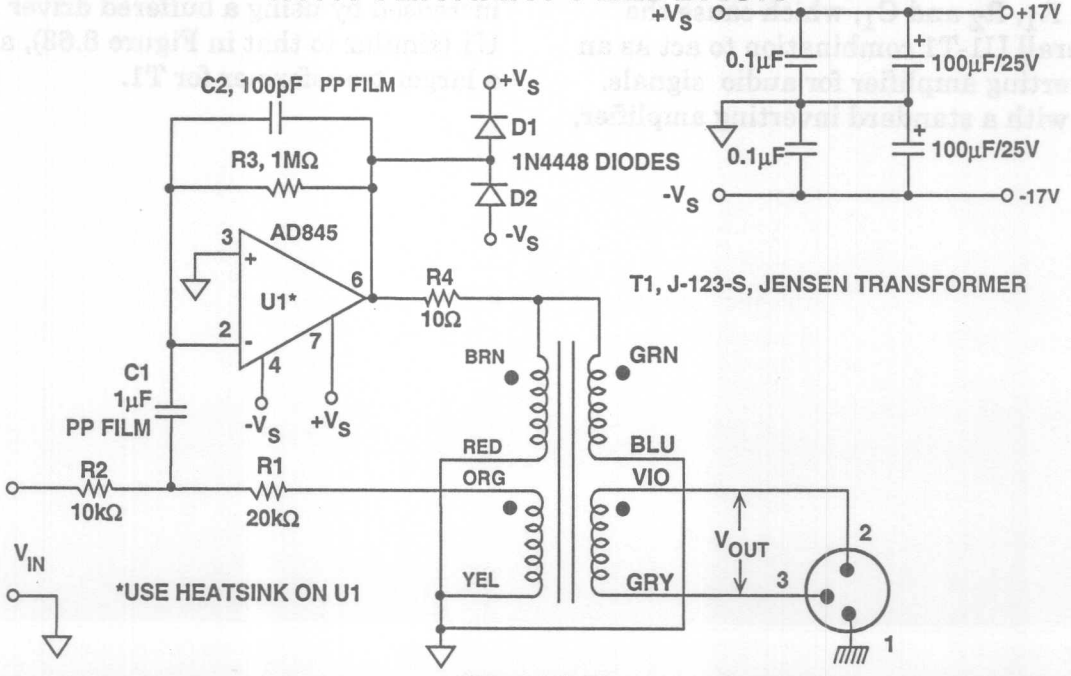


Figure 8.66

If a steel core transformer has several tightly-coupled windings, one may be used in a feedback loop to minimize the effects of the transformer non-linearity.

The circuit of Figure 8.66 is a low distortion driver using the quad-filar wound JT-123-S transformer, and an AD845 as the amplifier. Two parallel windings are used as the primary, feedback is taken from one secondary, and a another drives the balanced 600Ω load.

To minimize DC offset, an FET input op amp is used, with local DC feedback via R_3. This ensures that the maximum DC at the primary is no more than the sum of the amplifier Vos and Ibias×R_3. For bias currents greater than 1nA and a high value for R_3, the bias current component may become the dominant DC error. As a consequence a FET input device should be used for U1. Since the AD845 can also dissipate ≥300mW, a heat sink will minimize temperature and hence bias current.

The transformer feedback loop is closed via R_1, R_2 and C_1, which cause the overall U1-T1 combination to act as an inverting amplifier for audio signals. As with a standard inverting amplifier, gain is set via R_1 and R_2, which in this case provide an (unloaded) gain of 2x from V_{IN} to V_{OUT}. High quality film capacitors are recommended for C_1 and C_2, but their exact values and tolerances are not critical.

THD+N performance of this feedback driver is shown in Figure 8.67 using the specified JT-123-S transformer. A comparison of these data with those of Figure 8.65 demonstrates the effectiveness of the distortion reduction, and the variation of distortion with level and frequency. At some points the improvement is more than an order of magnitude.

Some precautions are necessary for the effective use of this circuit; they are mostly concerned with circuit dynamics. The circuit should not be overdriven, particularly at low frequencies, as the resulting distortion can be quite high. Clamping diodes D1 and D2 absorb any inductive kicks from T1 which might damage U1. The output of the basic circuit is limited to just over 5Vrms into 600Ω at low frequencies, but this can be increased by using a buffered driver for U1 (similar to that in Figure 8.63), and a larger transformer for T1.

STEEL CORE TRANSFORMER WITH FEEDBACK DRIVER THD + N (%) VERSUS FREQUENCY (Hz) FOR V_{out} = 5, 2, 1, 0.5V rms, R_L = 600Ω, V_S = ±17V

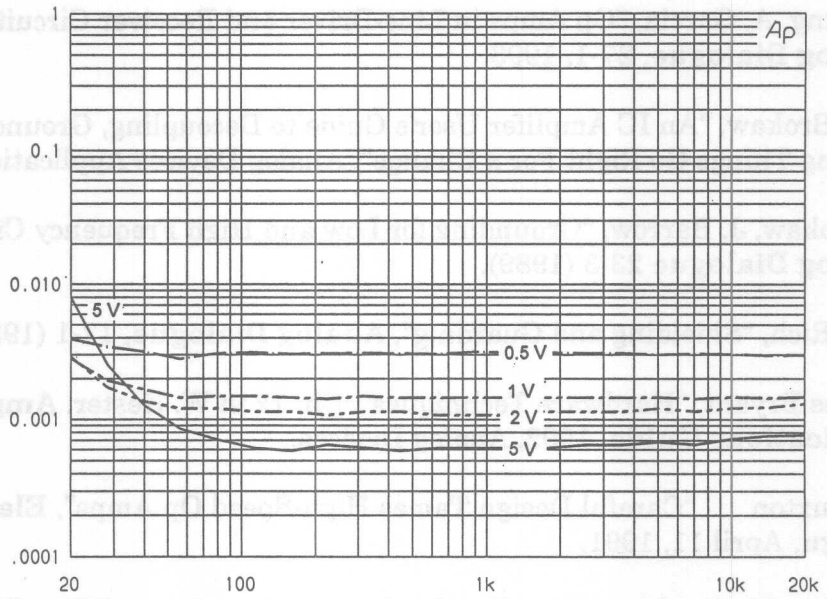


Figure 8.67

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APPENDIX: DC SERVO CONTROLLED AUDIO STAGES

With multiple stages of audio-frequency gain, the accumulation of DC offsets in various amplifiers can lead to problems. A classical solution to decoupling DC offset has been to employ input/output coupling capacitors. Typically, this involves the use of large value electrolytic capacitors (100 to 1000 μF) when operating into low impedances.

Modern low-bias-current, low-offset-voltage op amps allow simple elimination of coupling capacitors in many instances. For example, the use of low bias current, low offset voltage FET input amplifiers such as AD711/AD712/AD713, AD744/AD746, and OP-249 in a basic gain-of-10 stage will not generally require capacitive coupling. With an appropriate device choice, output offset can be held to as low as ±10mV or less, and will scarcely vary with source resistance.

This is one approach to the elimination of coupling capacitors. A more general approach which has come into vogue in recent years is the use of a *DC servo amplifier* stage, for output offset elimination.

8

NON INVERTING GAIN STAGE WITH SERVO

The circuit of Figure 8.68 is a standard non inverting audio voltage-amplifier gain stage (U1), with a non inverting integrator feedback stage connected around it (U2). For normal audio input signals, the gain of this stage is defined conventionally; that is, it is the ratio of the U1 feedback resistance (R_2) to the total resistance from the inverting input to ground plus 1. In this instance, the resistance to ground is made up of the parallel equivalent resistances of R_3 and R_4, so the net gain "$G_{(U1)}$" of stage U1 is:

$$G_{(U1)} = 1 + \frac{R_2}{R_3 || R_4} \qquad \text{Eq. 8.23}$$

In the servo circuit R_5-C_1 and R_6-C_2 form the integration time constants, which should be well matched in this form of integrator. The DC feedback from stage U2 is applied to the inverting input of U1 via R_4. The servo loop forces the net DC output of amplifier stage U1 to a very low level. In practice, the DC output offset of U1 becomes equal to the offset voltage of amplifier U2.

Two factors affect the low frequency rolloff of the U1 gain stage, as altered by the servo loop. One is the integrator RC time constant, which sets the integrator stage's -3dB frequency point, $f_{(U2)}$ (*not* the overall system -3dB point). The integrator 3dB point is:

NON-INVERTING GAIN STAGE WITH DC SERVO

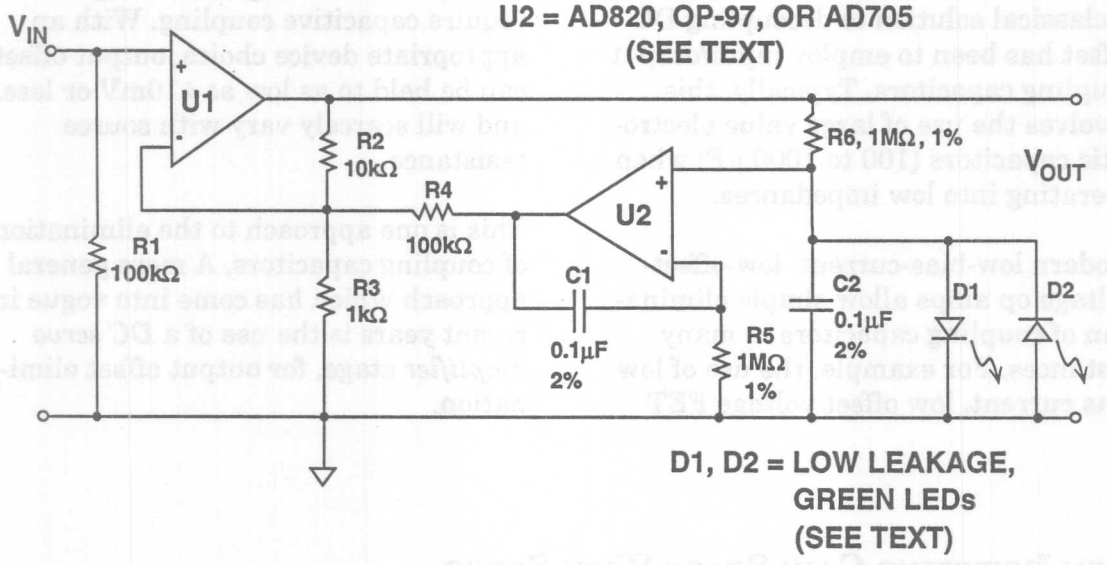


Figure 8.68

$$f_{(U2)} = \frac{1}{2\pi R_5 C_1} \qquad \text{Eq. 8.24}$$

where $R_5 = R_6$, & $C_1 = C_2$.

A second factor is the total DC transfer ratio of the circuit, measured from the U2 input to the U1 output, or servo sense point. If this is defined "1/n", then a modified expression for the overall circuit's -3dB point can be written as:

$$f_{(3dB)} = \frac{1}{n2\pi R_5 C_1} \qquad \text{Eq. 8.25}$$

where $n = R_4/R_2$, thus:

$$\frac{1}{n} = \frac{R_2}{R_4} \qquad \text{Eq. 8.26}$$

The servo RC values should be selected first for reasonable values. Then, feedback resistor R_4 is chosen several times higher than R_2, making "n" large and "1/n" small. In the example, 1/n is 0.1, so the the rolloff point is about 0.16 Hz. In general the rolloff frequency should be around 1% of the low frequency limit of the signal being processed.

At the U2 amplifier input, low-leakage (≤100 pA) clamp diodes should clamp C_2, to prevent possible latch up. Suitable diodes are ordinary green LEDs with a light shield such as shrink tubing (to eliminate photocurrents), or C-B junctions of 2N5088/89 NPN transistors. Servo amplifier U2 should be a unity gain compensated, low offset voltage, low-input-bias-current op amp. This can be either a FET-input device or a bias current compensated super-ß bipolar. Possible choices are the AD711 or the OP-41 (FETs); or an OP-97 or AD705 (bipolar).

Note that most FET input op amps will need the clamp diodes to prevent phase reversal. When working on a common rail design (i.e., both the servo amplifier and amplifier being servo'd operate from common rails), there are exceptions to this behavior. These are the AD820 and AD822 op amps, which, as single supply designs, have working input CM ranges which include the negative rail. As such they can be used without special precautions against latchup, and they also serve very well as integrators due to their very low bias current of 2pA and their rail-rail output swing. Given these characteristics, the AD820 and AD822 are especially suitable for the application.

Any servo amplifier IC working on supplies lower than that of the servo'd amplifier must use the clamping diodes. An audio power amp, for example, may swing ±50V at its output, and such potentials can cause malfunction or outright destruction in lower voltage servo ICs.

U1, and its associated circuitry, can take on many forms more complex than the one in this basic example. U1 might be a high output swing power amplifier. The servo loop would still operate as described, and correct not only offset errors due to U1, *but also any varying DC input level to U1*. The servo technique can be useful for continuous correction of high bias current, high offset or high drift. (It will even stabilize thermionic valves— another exercise for the historically minded reader).

Ensure that the worst-case offset to be corrected at the input of U1 is within the dynamic range defined by the values assigned for R_2-R_3-R_4, the specific supply voltages used for U1-U2, and the clamps. High-quality low-leakage 1 or 2% film capacitors should be used in the integrator along with 1%, 50ppm/°C metal-film resistors. Since these components will be high-impedance, lead lengths should be minimized around U2, and the assembled circuit should be carefully cleaned of any flux residue. The outside foils of both C_1 and C_2 should be connected to the lower impedance of the two nodes.

INVERTING GAIN STAGE WITH SERVO

An inverting stage with servo offset correction is shown in Figure 8.69, and uses a familiar inverting integrator for feedback. In this circuit, U1 is an inverting audio stage with a gain of R_2/R_1. DC feedback from the U2 integrator stage is applied to U1 through the divider, R_4-R_3.

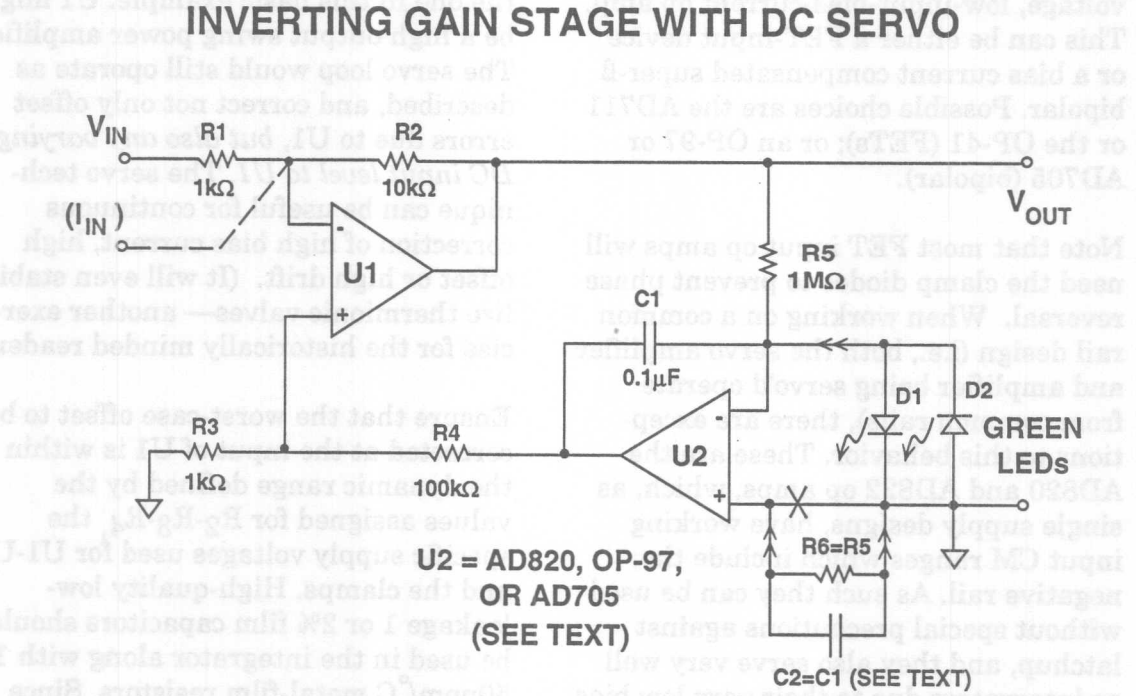


Figure 8.69

In this circuit the 1/n scaling factor around the U2-U1 DC loop is:

$$\frac{1}{n} = \left(\frac{R_3}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_1}\right) \qquad \text{Eq. 8.27}$$

which is used to calculate the circuit's effective rolloff. With the time-constant values shown and the scaling of R_4-R_3, the circuit of Figure 8.69 has a low frequency cutoff of about 0.17 Hz.

When used just as shown with the U2 noninverting input grounded, clamping diodes may not be necessary if they are integral to U2, as they are in the AD705 and OP-97. For higher bias current amplifiers at U2, the compensation network R_6-C_2 may be used, in which case low-leakage input clamp diodes are recommended. In any case, the use of quality components for R_5

and C_1 is important. Again, R_4 should be about ten times R_2 (with R_1 and R_3 equal), and the supply voltage used for U1-U2 must be sufficient to accommodate the worst DC offset expected of U1. This circuit also works with more complex inverting stages, including discrete ones.

In principle, a *non inverting* integrator could also be used, with DC feedback to the R_1-R_2 junction. The inverting integrator is more simple overall, however, and eliminates one RC network. This circuit works well when U1 has a current input.

From a system point of view, the "1/n" scaling factor of the servo can be very useful in extending the low frequency range of these two basic designs. A DC attenuator or "tee" network can be placed between the U1 output and the integrator, and will work in a similar fashion for 1/n frequency scaling.

However, this particular frequency scaling approach should be used with caution, as it has the side effect of increasing the input offset of integrator U2 by the amount of attenuation. The output offset of U1 is then higher. For modest attenuations prior to the integrator (≤10 times), the circuit can be useful with the AD705 or OP-97 or similar devices, as their worst case offset is below 100μV. In general, the offset multiplication effect prevents most amplifiers from being used with substantial (≥10 times) input attenuation prior to R_5.

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SPEAKER CROSSOVERS
Hank Zumbahlen

The physics of sound reproduction make it very difficult for one driver (loudspeaker) to handle all audio frequencies. Therefore, most speaker systems consist of multiple drivers, each reproducing a segment of the audio spectrum. A mass-controlled piston working into an acoustic load derives its response curve from the cancellation of two opposing effects. First is the cone excursion which is inversely proportional to the square of the frequency. The second is the resistance of the acoustic load which is proportional to the square of the frequency. These effects cancel in the center of a speaker's frequency response, creating a flat response.

SPEAKER CROSSOVER CONSIDERATIONS

- Frequency Division Between Speakers
- Speaker Impedance Versus Frequency (Compensation)
- Component Selection
- Passive Versus Active Crossover Networks

Figure 8.70

At some high frequency, where the wavelength of the acoustic wave is less than the circumference of the driver; the acoustic resistance levels off, and the response of the speaker rolls off at 12 dB/octave. At the resonant frequency of the driver, the excursion is dominated by the compliance of the suspension rather than the mass of the cone. This causes a roll off which is also 12 dB/octave. Therefore, reproduction of low frequencies requires a speaker that has a large surface area, allowing it to move a large amount of air. The driver surface should also have relatively high stiffness so that the surface moves as a uniform piston with no flexing. This usually implies higher mass.

For high frequencies, the tweeter should have as little mass as possible so that it can respond to the input signal quickly. Even though a zero-mass tweeter would be ideal, the tweeter still needs stiffness so that it does not flex.

Most speakers work well over a frequency range of about 10:1. This means that we would customarily use three drivers to cover the audio spectrum of 20 Hz to 20 kHz. For reasons of simplicity (and cost), designers sometimes try to cover the frequency spectrum with only two drivers. This places higher demands on each driver and usually requires sharper cutoff rates on the crossover filter to limit the out-of-band driver signals. It is especially important to limit the low frequency energy to the tweeter in order to limit its excursion.

Since we have separate speakers covering different portions of the spectrum, we need to divide the input signal spectrum and then direct the proper portions to the proper drivers. These crossovers are usually passive filters placed between the power amplifier and the drivers. Sometimes, however, we may want to implement the crossover function at line level. There are some advantages as well as disadvantages to this approach.

The passive crossover is simply a high-level passive filter. The speaker is the load impedance of the network. We generally assume zero source impedance (as opposed to using a source termination). This ensures the maximum power is delivered to the load. Next we determine the crossover type. The two configurations used most often in speaker crossover design are the all-pass configuration (APC) and the constant-power configuration (CPC).

The APC, introduced by Garde, is the current favorite. When the outputs of the filters are combined, the resultant has the same magnitude as the input at all frequencies. This is shown in the following equation (Eq. 1) where V_{IN} is the input voltage, V_L is the low pass output voltage, V_M is the bandpass output voltage and V_H is the high pass output voltage. Phase does not appear in this equation.

$$|V_L + V_M + V_H| = |V_{IN}| \qquad \text{Eq. 1}$$

It is not possible to pass a signal through a ladder network and preserve both magnitude and phase. APCs are desirable because they do not introduce variations in the speakers amplitude response.

The other popular network is the CPC (constant power crossover). In the CPC, the output *power* of the network is equal to the input (Eq. 2).

$$|V_L|^2 + |V_M|^2 + |V_H|^2 = |V_{IN}|^2 \qquad \text{Eq. 2}$$

The use of this type of crossover predates the APC in commercial systems by many years. It is interesting to note that odd-order systems are both APC and CPC.

The next thing that must be determined is the order (number of poles) of the system. All-pole systems roll off at 6n dB/octave, where n is the order.

First order systems are attractive because few components are required. However, because of the low rolloff rate, the response of the drivers must be flat far beyond the crossover frequency. As

a practical matter, the speaker responses overlap so much that problems such as interdriver cancellation are more troublesome. (Interdriver cancellation occurs when two drivers operate at the same frequency, and the speakers are separated by an odd multiple of 1/2 the wavelength of the signal.) A first order system is a minimum phase system as well.

Second order systems are considered by many to be the lowest acceptable order for a crossover network. The number of components is still manageable, the operational range is better controlled, and the phase shift of the network is still quite low. In contrast to odd order crossovers, 2nd order (and all even order) crossovers are insensitive to system phase relationships.

Third order systems are also very popular. Since they are odd order, they are both APC and CPC. The number of components is still manageable, but the phase shift of the network is greater.

Fourth order systems are sometimes used where a high cutoff rate is required (often to reduce the excursion of a tweeter). The disadvantages of fourth order systems are high component count (high cost), and high phase shift in the network.

IMPEDANCE COMPENSATION

All design equations for crossover networks assume a constant load impedance. The impedance of a speaker is far from constant as shown in Figure 8.71. We should therefore add networks to try to equalize this impedance. Typically, this network takes the form of a series R-C across the speaker terminals (called a Zobel network) as shown in Figure 8.72.

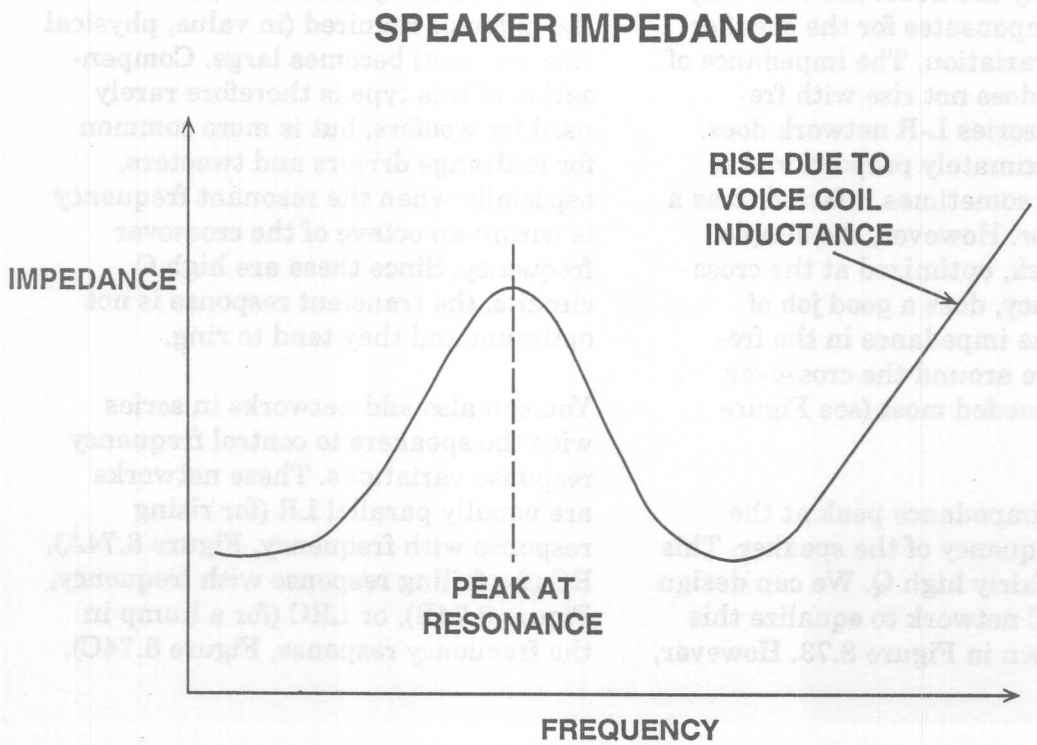


Figure 8.71

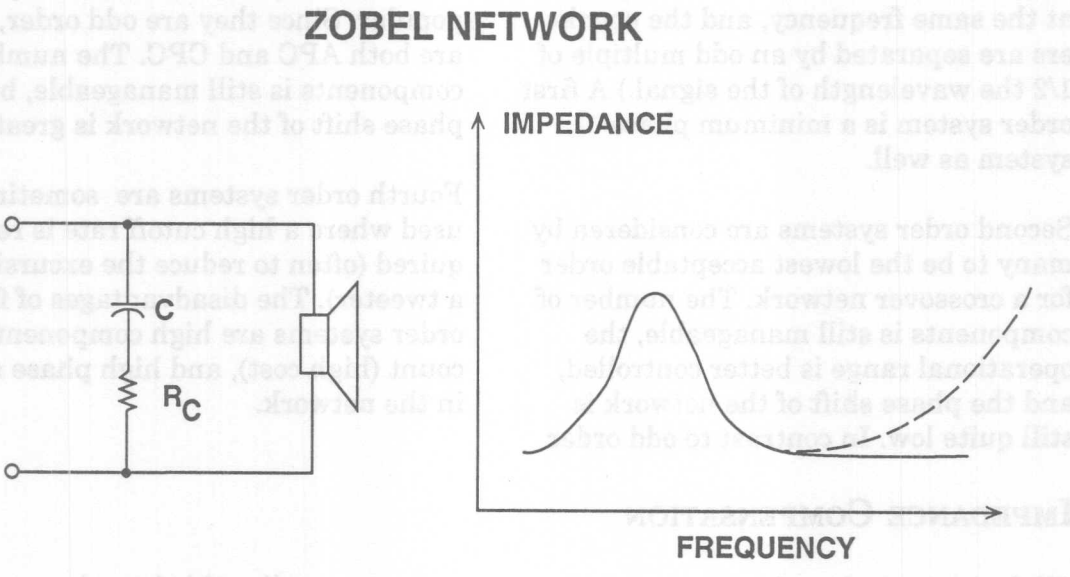


Figure 8.72

Unfortunately the Zobel network only partially compensates for the speaker impedance variation. The impedance of the speaker does not rise with frequency as a series L-R network does, but is approximately proportional to $R\sqrt{L}$. This is sometimes referred to as a *semi-inductor*. However, the simple Zobel network, optimized at the crossover frequency, does a good job of flattening the impedance in the frequency range around the crossover where it is needed most (see Figure 8.72).

There is an impedance peak at the resonant frequency of the speaker. This peak has a fairly high Q. We can design a series LRC network to equalize this peak as shown in Figure 8.73. However, as the frequency goes down, the size of the inductor required (in value, physical size and cost) becomes large. Compensation of this type is therefore rarely used for woofers, but is more common for midrange drivers and tweeters, especially when the resonant frequency is within an octave of the crossover frequency. Since these are high Q circuits, the transient response is not optimum and they tend to ring.

You can also add networks in series with the speakers to control frequency response variations. These networks are usually parallel LR (for rising response with frequency, Figure 8.74A), RC (for falling response with frequency, Figure 8.74B), or LRC (for a hump in the frequency response, Figure 8.74C).

RESONANCE COMPENSATION

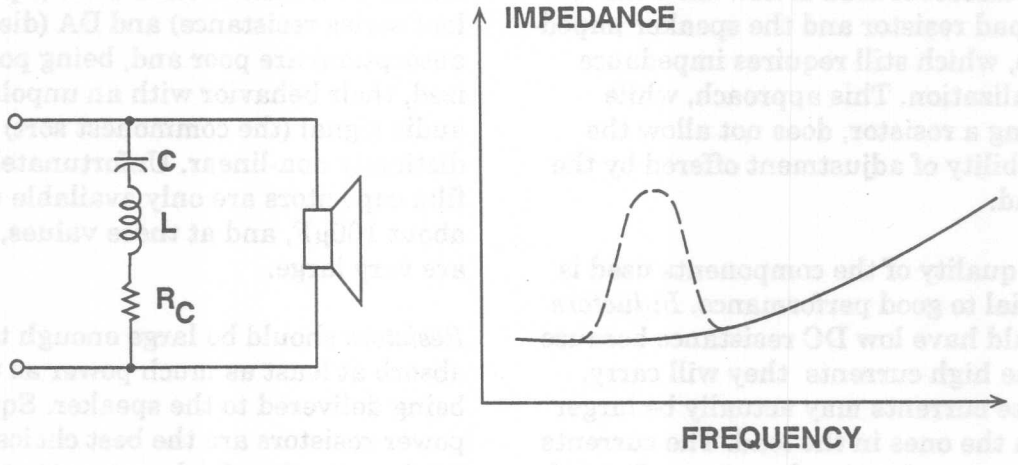


Figure 8.73

SERIES NETWORKS OFTEN USED TO CONTROL SPEAKER IMPEDANCE

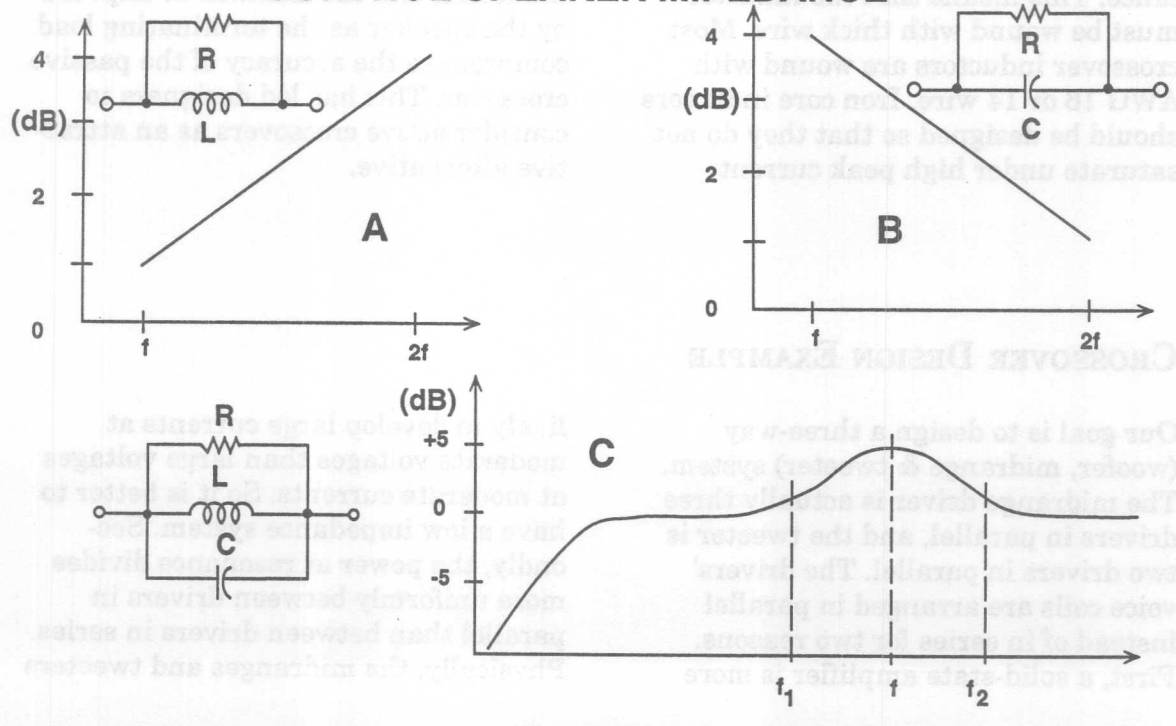


Figure 8.74

A last function which should be accomplished by the crossover is to equalize the sensitivities of the drivers. This is normally accomplished with an L-pad so that the signal level can be adjusted without affecting the load impedance seen by the network. An alternative is to use a resistor in series with the load. The crossover load is now the sum of the pad resistor and the speaker impedance, which still requires impedance equalization. This approach, while saving a resistor, does not allow the flexibility of adjustment offered by the L-pad.

The quality of the components used is crucial to good performance. *Inductors* should have low DC resistance because of the high currents they will carry. These currents may actually be larger than the ones in the load. The currents can approach tens of amperes. Since the impedance levels are low, it only takes a small amount of resistance to turn a LC network into a LRC network. The formulas for passive crossovers assume ideal inductors with no series resistance. This means that the inductor must be wound with thick wire. Most crossover inductors are wound with AWG 16 or 14 wire. Iron core inductors should be designed so that they do not saturate under high peak current conditions. Many audiophiles dislike iron core inductors for this reason, but they do allow higher inductance values for a given amount of wire and provide lower DC resistance.

Capacitors for audio use should have a film dielectric. Electrolytic capacitors should be avoided. Their ESR (equivalent series resistance) and DA (dielectric absorption) are poor and, being polarized, their behavior with an unpolarized audio signal (the commonest sort) is distinctly non-linear. Unfortunately, film capacitors are only available up to about 100μF, and at these values, they are very large.

Resistors should be large enough to absorb at least as much power as that being delivered to the speaker. Square power resistors are the best choice. The are inexpensive, fairly accurate, and they are resistive rather than reactive throughout the audio frequency range.

The physical size of the components, the series resistance of even high quality inductors, and the limitations imposed by the speaker as the terminating load compromise the accuracy of the passive crossover. This has led designers to consider active crossovers as an attractive alternative.

CROSSOVER DESIGN EXAMPLE

Our goal is to design a three-way (woofer, midrange & tweeter) system. The midrange driver is actually three drivers in parallel, and the tweeter is two drivers in parallel. The drivers' voice coils are arranged in parallel instead of in series for two reasons. First, a solid-state amplifier is more likely to develop large currents at moderate voltages than large voltages at moderate currents. So it is better to have a low impedance system. Secondly, the power at resonance divides more uniformly between drivers in parallel than between drivers in series. Physically, the midranges and tweeters

alternate in a line-array arrangement. This is variation on the D'Appolito configuration. This configuration has the advantage of a very uniform horizontal frequency response.

First we measure the impedance of the speakers versus frequency. We use the setup of Figure 8.75. This approximates a constant current source. We first substitute a 10Ω resistor for the speaker. We then adjust the level of the oscillator for 10mV across the resistor. Now, leaving the oscillator level fixed, we replace the speaker and measure the impedance directly; 1mV corresponds to 1Ω impedance.

IMPEDANCE MEASURING

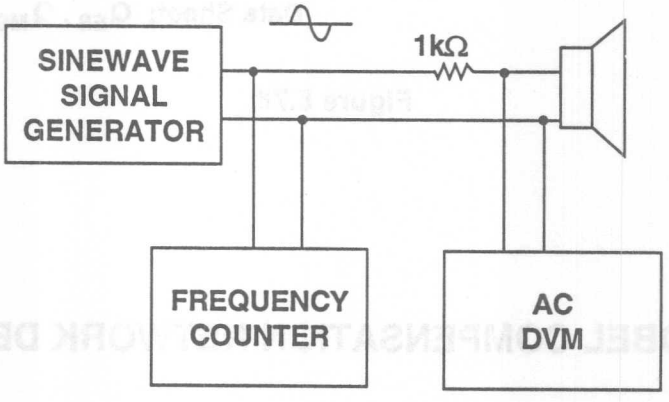
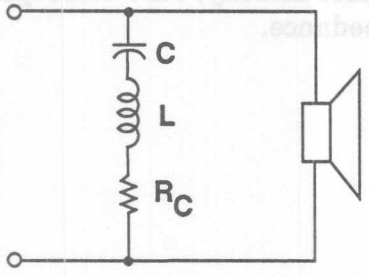


Figure 8.75

As it is desirable to load the passive filter with a fixed impedance, the impedance versus frequency should be as flat as possible.

The design equations shown in Figure 8.76 and Figure 8.77 are now used to determine the passive crossover network component values (Figure 8.78).

RESONANCE COMPENSATION NETWORK DESIGN



Design Equations:

$$C = \frac{0.1592}{R_E Q_{ES} f_s}$$

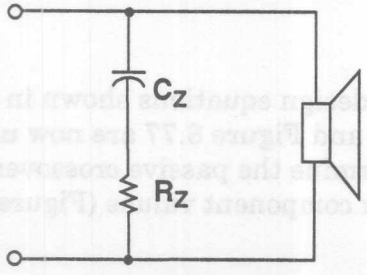
$$L = \frac{0.1592\, R_E Q_{ES}}{f_s}$$

$$R_C = R_E + \frac{Q_{ES} R_E}{Q_{MS}}$$

Obtain From Speaker Manufacturer's Data Sheet: Q_{ES}, Q_{MS}, R_E, f_s

Figure 8.76

ZOBEL COMPENSATION NETWORK DESIGN



Design Equations:

$$R_Z = 1.25 R_E$$

$$C_Z = \frac{L_E}{R_Z^2}$$

L_E = Driver Voice Coil Inductance in Henries

Figure 8.77

IMPEDANCE MATCHING NETWORKS

DRIVER	C	L	R_C	C_Z	R_Z
Midrange	466µF	1.23mH	2.4Ω	23.2µF	2.2Ω
Woofer	7538µF	9.3mH	3.0Ω	66.9µF	3.5Ω

NOTE: TWEETER REQUIRES NO IMPEDANCE COMPENSATION

Figure 8.78

The capacitance value of 7538µF for impedance compensation (C, L & R_C) is not practical for the woofer because the frequency of the impedance peak is so low. We will therefore ignore this part of the compensation. If this were a ported enclosure, the impedance hump would actually be partially tuned out by the enclosure. This would reduce the large hump and add an additional smaller hump. This system is a transmission line, however, which tends to flatten impedance peaks.

For the remaining components we use the nearest standard value for the inductors and resistors. We synthesize the desired capacitor values by paralleling standard values. The 466µF capacitor is made by paralleling 280µF + 140µF + 47µF. Because of the size of the capacitors, we are forced to use electrolytics for values >100 µF. This is not a significant problem in this design, since the resonant tank circuit functions over a relatively small frequency range. Also, since it is a shunt circuit, its effects are not heard in the speaker. In addition, the frequency of the resonance is low so the ESR of the cap is minimized. To eliminate the requirement of a polarization voltage, we use non-polarized electrolytics (back-to-back electrolytics arranged so that either one or the other is properly polarized). The effectiveness of this compensation is shown in Figure 8.79 for the woofer and in Figures 8.80 and 8.81 for the midrange driver.

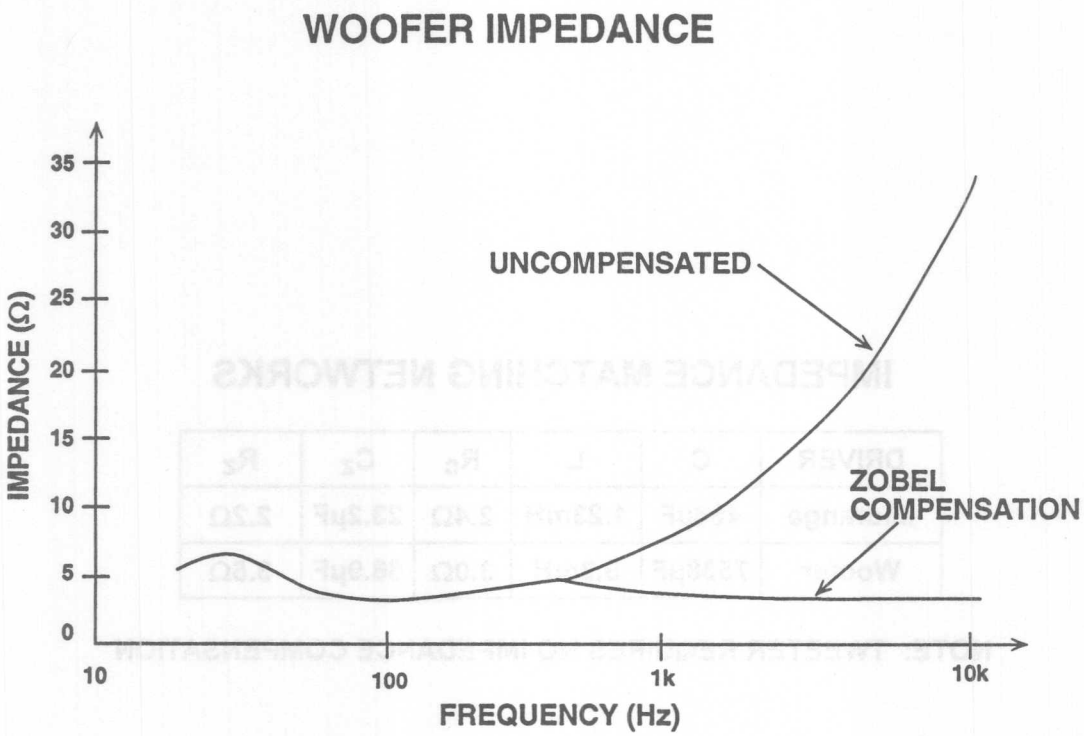


Figure 8.79

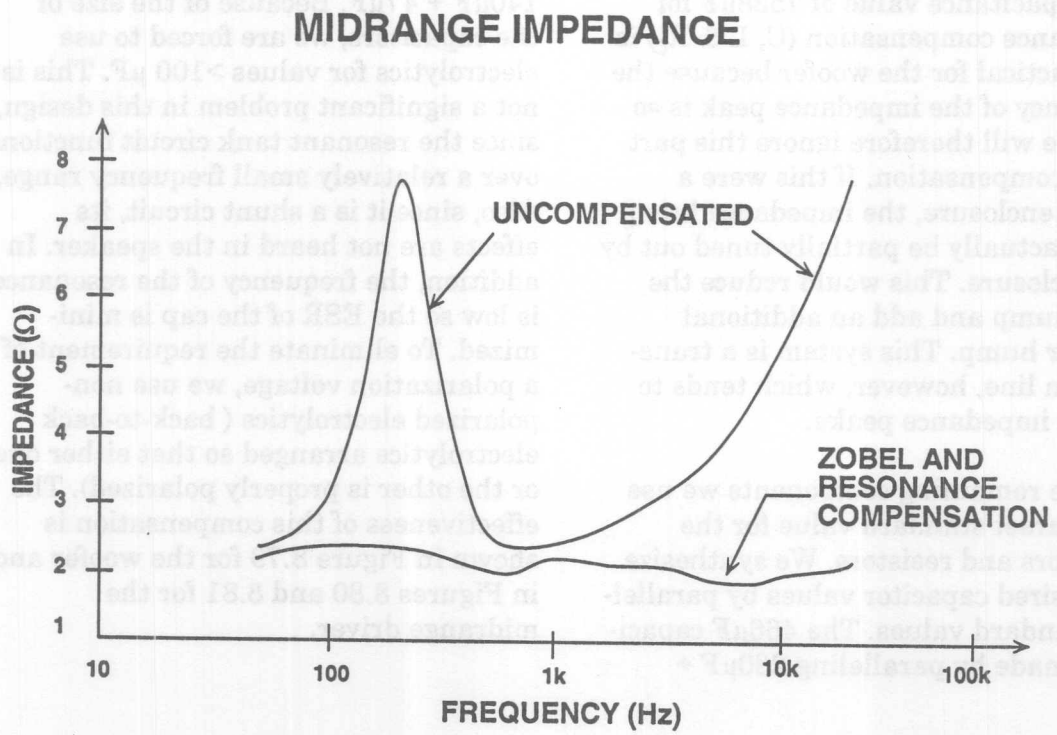


Figure 8.80

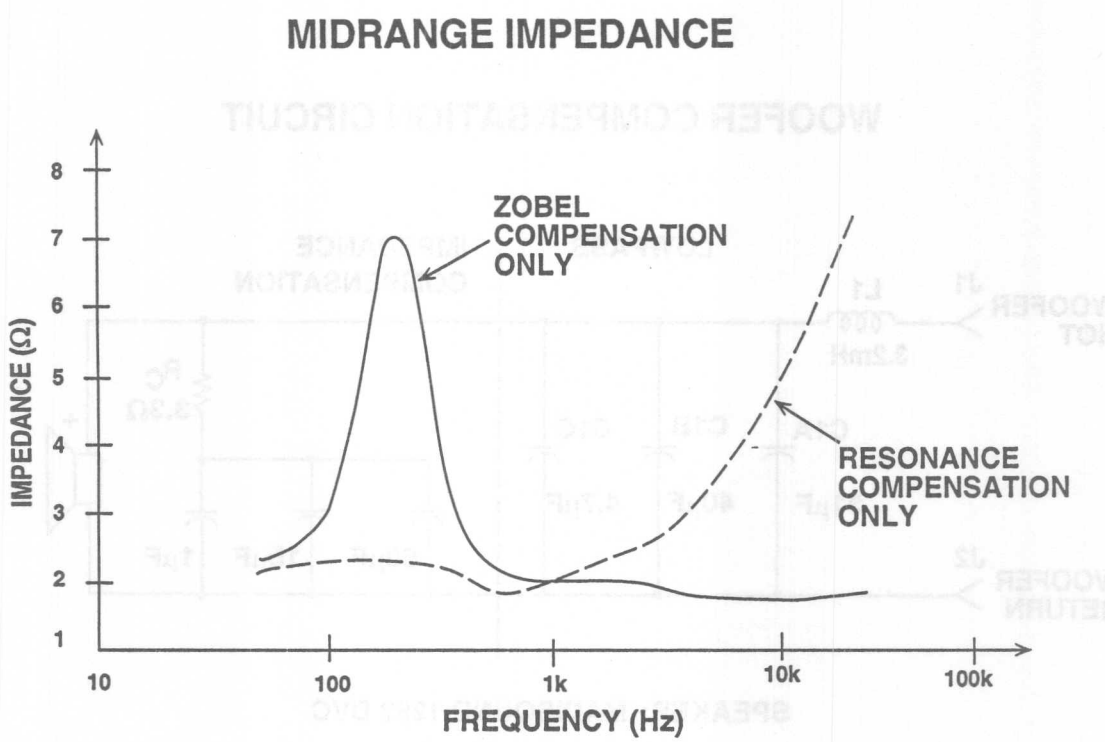
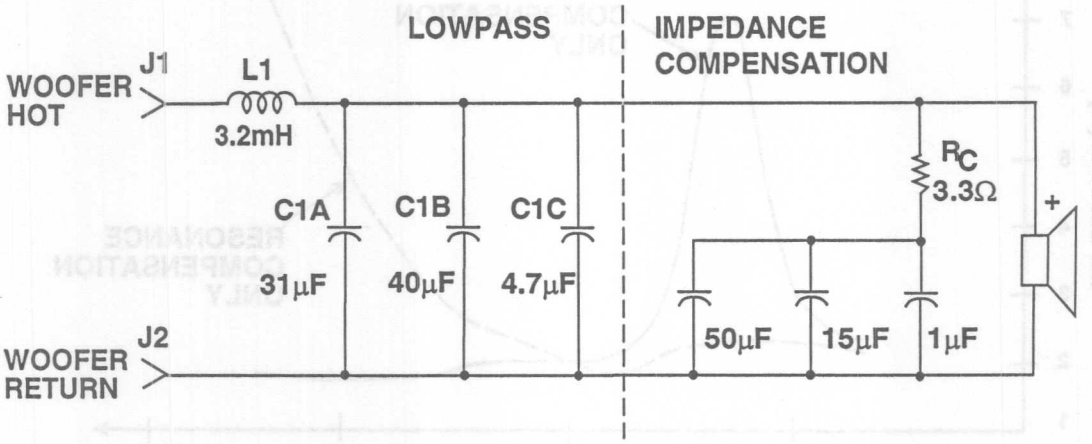


Figure 8.81

We do not attempt to compensate the tweeter because the impedance peak is relatively small and far away from the tweeter passband. Also, the impedance does not begin to rise with frequency until beyond 20 kHz. While this is true of this particular set of drivers, it is not necessarily so, and impedance compensation may be required if other drivers are used.

With the speaker impedances compensated, we design the actual crossovers. We choose a 2nd order APC. We start by using the equations of Bullock in his classic series on crossovers in *Speaker Builder* (1/85 - 3/85, 1/86 & 4/87). The equations were put into a spreadsheet to allow for easy manipulation of the numbers. The cutoff frequencies were then modified slightly so that the inductors required fall as close as possible to standard values. The calculations used are in Appendix 1. The capacitor values are synthesized by paralleling standard values. The final schematics are shown in Figures 8.82, 8.83, and 8.84. Note that the polarity of the midrange drivers are reversed. This is critical for the proper response.

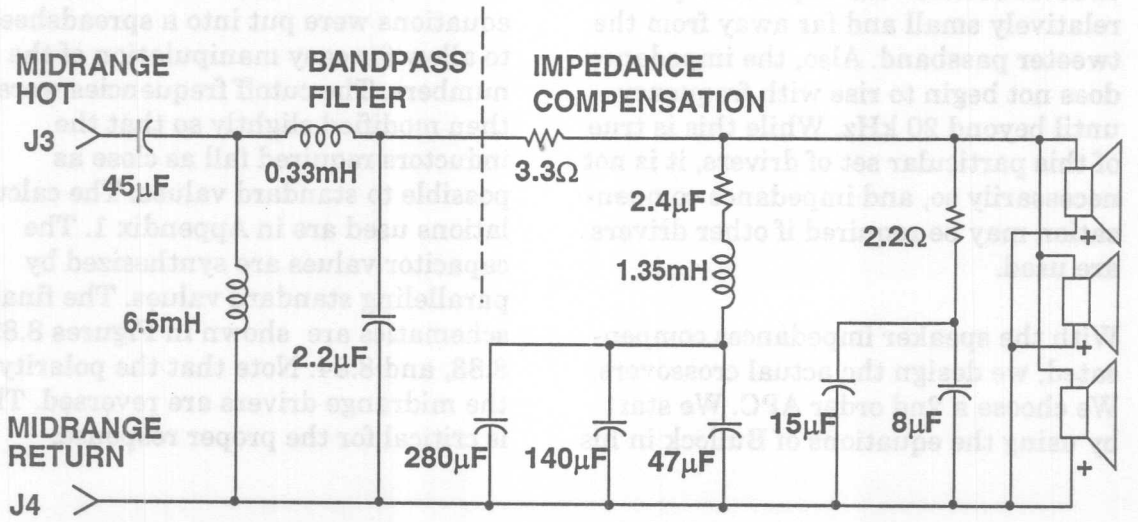
WOOFER COMPENSATION CIRCUIT



SPEAKER: MADISOUND 1252 DVC

Figure 8.82

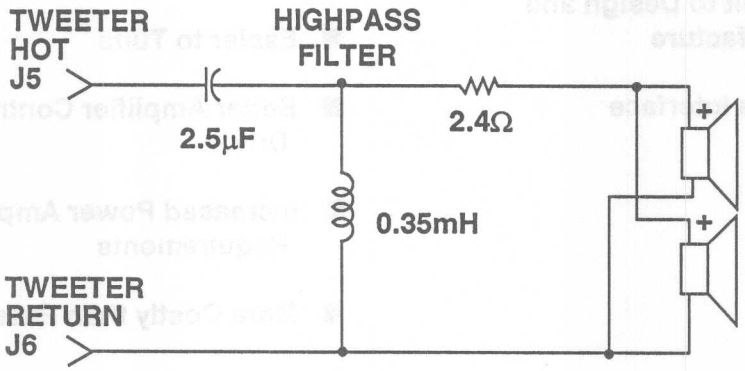
MIDRANGE COMPENSATION CIRCUIT



SPEAKERS: AUDAX HD12P25FSM
NOTE: SPEAKERS WIRED OUT OF PHASE

Figure 8.83

TWEETER COMPENSATION CIRCUIT



SPEAKERS: AUDAX HD100D25

Figure 8.84

Some final points regarding the passive crossover are in order. If the inductors are oriented so that their magnetic fields overlap, unwanted voltages may be induced from one inductor to the other by mutual inductance. This can be avoided by orienting coils in close proximity and at right angles to each other.

In wiring the drivers, use two separate wires (hot and common) to each set of drivers rather than use a common return for all drivers. This minimizes inductance and impedance in the return path and prevents the modulation of one speaker by the other. This idea may be extended by providing two separate cables between the power amplifier and the speakers: one for the woofer, and one for the midrange and tweeter. This is referred to as *bi-wiring*.

Active Crossover Network Design

Active crossovers are active filters which partition the frequency spectrum. They are line level circuits which are placed in front of the power amplifiers. A separate power amplifier is therefore required for each frequency range speaker. This is the active crossover's chief disadvantage. Since a separate amplifier is required for each band, the cost of the system is much higher. However, there are many advantages to active crossovers.

PASSIVE VERSUS ACTIVE CROSSOVERS

PASSIVE	ACTIVE
■ Large, Expensive Components	■ More Component Spread Allowed
■ Difficult to Design and Manufacture	■ Easier to Tune
■ Simple Interface	■ Better Amplifier Control of Driver
	■ Increased Power Amp Requirements
	■ More Costly than Passive
	■ Time Domain Compensation Possible

Figure 8.85

First, the active crossover network is isolated from the speaker impedance by the power amplifier. This makes the design of the filter simpler and more accurate. Second, the impedance of the filter may now be scaled so that component values can be made more practical. Another advantage is that inductors are not used in active filters, and it is much easier to tune an active filter than a passive filter because of the isolation between the sections of the active filter.

Another possible feature which can be implemented in an active crossover is time delay. The acoustic center of a speaker is located approximately at the point where the voice coil attaches to the cone (or dome). When different speakers are mounted on a common baffle, their acoustic centers do not line up. This results in a time difference which can be canceled by delaying the signal to one speaker relative to another. This can be accomplished with an all-pass filter. Time alignment can also be accomplished by mounting the different speakers on baffles that are offset from each other. However, this increases manufacturing difficulty and may cause problems with diffraction around the baffle edges.

In the active design, impedance matching circuits may be eliminated. Almost all modern audio power amplifiers have very low output impedances at audio frequencies. This means that they will provide whatever current is required (within the amplifiers' current output capability), to develop the correct voltage across the load. Therefore, speaker impedance changes with frequency do not affect overall performance.

Another advantage of an active crossover is that since the speakers are connected directly to the amplifier, the damping ratio of the amplifier can control the back-EMF of the speaker. This is especially true for the woofer. A dynamic driver works by developing a voltage in a coil of wire (in this case called a voice coil) which then moves relative to a fixed magnet. Back-EMF is produced by the speaker's voice coil moving through a magnetic field due to the momentum of the cone, not because of an input signal. This sets up a voltage in the coil. If the coil is connected to a low impedance source, such as the power amplifier, the induced voltage is essentially shorted out. If there were a passive crossover between the speaker and the driver, this back EMF would distort the signal because of the finite driving impedance. Eliminating this effect results in better transient behavior (i.e.,"faster" bass).

We can now design the active frequency crossover network. We would typically use a standard filter realization such as the Sallen and Key or Multiple Feedback (MFB). For a second order filter, the "a" parameter in Bullock's article is α (1/Q) for the filter. The "H" parameter is the gain peaking function of the bandpass. If we had used a CPC filter we would probably implement the active crossover as a Butterworth filter of the proper order. For an APC filter it is more complicated if the proper response is to be maintained, as the equations are a function of the spread in the two crossover frequencies.

First select the circuit topology. It may seem attractive to form the bandpass section by subtracting the lowpass and highpass sections from the input signal. The problem with this approach is that the response does not turn out the way that we would expect.

Take for example subtraction of a lowpass from the input signal to form a high pass (HP = high pass response, LP = low pass response) :

$$HP = 1 - LP$$

$$HP = 1 - \frac{1}{s^2 + 2s + 1}$$

$$HP = \frac{s^2 + 2s}{s^2 + 2s + 1}$$

This is not the same as a standard high pass transfer equation:

$$HP = \frac{s^2}{s^2 + 2s + 1}$$

Thus we get an asymmetrical transfer function that will meet the constant voltage requirement of the CPC but not the constant power requirement of the APC.

The second option is a slight variation on the first: cascading two state-variable filters. The first will be tuned for the lower crossover frequency and the second for the upper crossover frequency. State variable filters have both high pass and lowpass (as well as bandpass) outputs. The lowpass output of the first section will be the woofer signal. The highpass output of the first section will be the input of the second section. The second section's lowpass output will then be a bandpass output which will be our midrange signal. The highpass output will be the tweeter signal.

This approach has the advantage of having no possible "hole" in the frequency response due to misalignment of the filter response. Since the same frequency determining components determine both high and low pass responses for each section, the responses must be the same. The disadvantage to this approach is that the number of components is increased. The signal passes through more op amps in this configuration.

Next we look at the brute force approach of building the filters out of second-order sections. We shall build the bandpass section as a combination of lowpass and high pass sections, since the crossover frequencies are more than an octave apart. We will use Sallen-Key filters, since they are the least dependent on the op amp parameters (although at the frequencies at which we are working, this is probably not a major consideration).

We have chosen a second order APC, also known as a Linkwitz-Riley response. This response is a Butterworth squared response. Therefore, the damping ratio is 1. The lower crossover point is 319 Hz. and the upper is 5300 Hz, the same as in the passive implementation. The component calculations are given in Appendix II. The final schematic is Figure 8.88. Note that the inversion required for the midrange is not provided for in the crossover, and must be accomplished in the system wiring. The measured frequency response of the active network is given in Figure 8.89.

It is advisable to insert a coupling capacitor between the power amplifier and the tweeter to protect it from turn on transients which can contain significant low frequency energy. These transients can easily turn the tweeter voice coil into an expensive fuse! The capacitor should be chosen so that it does not affect the transfer equation. Positioning the corner frequency a decade or greater below the upper crossover frequency is more than sufficient. Use a high quality film capacitor.

There are several other functions active crossovers can accomplish. The main one is to introduce time delays into the signal path. This allows the speakers to appear to have their acoustic centers aligned, even though they are mounted on a common baffle. This has an effect on the imaging characteristics of the system. The time delay can be implemented with *allpass* filters, which give a constant time delay (phase shift) and a flat amplitude response.

Subjective evaluations indicate active crossover networks sound better than their passive equivalents. Although they offer the ultimate in audio performance, the cost effectiveness of the active crossover must be determined by the designer.

REFERENCES ON CROSSOVERS

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CROSSOVER NETWORK: APPENDIX 1

PASSIVE CROSSOVER CALCULATIONS

The following design equations are from Robert Bullock's *Passive Crossover Networks Part II*. The equations were entered into a spreadsheet to facilitate manipulation. The crossover frequencies were manipulated so that inductor values fell as close as possible to standard values.

DRIVER	PART NO.	IMPEDANCE	SENSITIVITY
WOOFER	MADISOUND 1252DVC	3.2Ω	90
MIDRANGE	AUDAX HD12P25FSM	6.5Ω	93.6
TWEETER	AUDAX HD100D25	7Ω	91.5

LOW CROSSOVER FREQ: 319 Hz		(FL)	W1	=	2*PI*FL
HIGH CROSSOVER FREQ:5300 Hz		(FH)	W3	=	2*PI*FH
			FM	=	SQRT(FL*FH)
			W2	=	2*PI*FM
FREQUENCY SPREAD	16.61442		(S	=	FH/FL)
SQUARE ROOT OF S	4.076079		(R	=	SQRT S)

The sensitivities of the drivers are rarely the same. This means that if we provide the same signal level to the drivers, their acoustic outputs would differ. The fact that we are using an unequal number of multiple drivers also affects the sensitivity. The excess gain calculation allows the level equalization. From this we get a pad resistor. The sum of the pad resistor and the equalized driver impedance is the load resistance for the design equations:

EXCESS GAIN CALCULATIONS:

MINIMUM SENSITIVITY	=	90	(WOOFER)	
TOTAL SENSITIVITY:	WOOFER	=	90	
	MIDRANGE	=	98.37121	
	TWEETER	=	94.5103	
EXCESS GAIN:	MIDRANGE	=	8.371 dB	(2.622)
	TWEETER	=	4.510 dB	(1.681)
PAD RESISTORS:	MIDRANGE	=	3.5Ω	(RM)
	TWEETER	=	2.38Ω	(RT)
DESIGN IMPEDANCE:	WOOFER	=	3.2Ω	
	MIDRANGE	=	5.68Ω	
	TWEETER	=	5.88Ω	

CROSSOVER CALCULATIONS:

FILTER SHAPE	a	=	$2(S-1)/(S^2-2S)$	
		=	2.004114	
GAIN PARAMETER	H	=	$S+a^2-4+(3/S)$	
		=	16.81146	
BP SHAPE A	A	=	a*(R+1/R)	
		=	8.414262	
BP SHAPE B	B	=	$S+A^2+(1/S)$	
		=	20.69108	

					ACTUAL VALUE
					==========
C11	=	1/a/RL/W1	=	77.79596µF	31µF+40µF+4.7µF
L12	=	a/RL/W1	=	3.1996mH	3.2mH
L31	=	a*RH/W3	=	0.354mH	0.35mH
C32	=	1/a/RH/W3	=	2.547µF	2.5µF
	K	= B–1	=	19.69108	
	E	= A(1–1/K)	=	7.986948	
	RA	= RM(K/H–1)	=	0.972933Ω	
	R0	= RA+RM	=	4.486Ω	4.5Ω
C21	=	1/A/R0/W2	=	2.186µF	2.2µF
L22	=	A*R0/W2/K	=	0.3479mH	0.35mH
L23	=	E*R0/W2	=	0.354038mH	0.35mH
C24	=	K/E/R0/W2	=	45.3585µF	45µF

The design equations for the compensation network appear in Figures 8.76 and 8.77.

COMPENSATION COMPONENTS:

			CALCULATED	ACTUAL
			==========	==========
MIDRANGE:	RC	=	2.208Ω	2.2Ω
	CC	=	23.24µF	15µF+8µF
	RR	=	2.39Ω	2.4Ω
	LR	=	1.232mH	1.25mH
	CR	=	466.4µF	280µF+140µF+47µF
WOOFER:	RC	=	3.56Ω	3.3Ω
	CC	=	66.97µF	50µF+15µF+1µF

SPEAKER CROSSOVERS: APPENDIX II

ACTIVE CROSSOVER DESIGN

We will design the active crossover to have the same crossover frequencies as the passive crossover, namely 319 Hz. and 5300 Hz. We will also define the crossover as having the Linkwitz-Riely response which is a Butterworth squared response. Therefore the α of the 2nd order section is 2. All sections are unity gain Sallen-Key as shown in Figure 8.86.

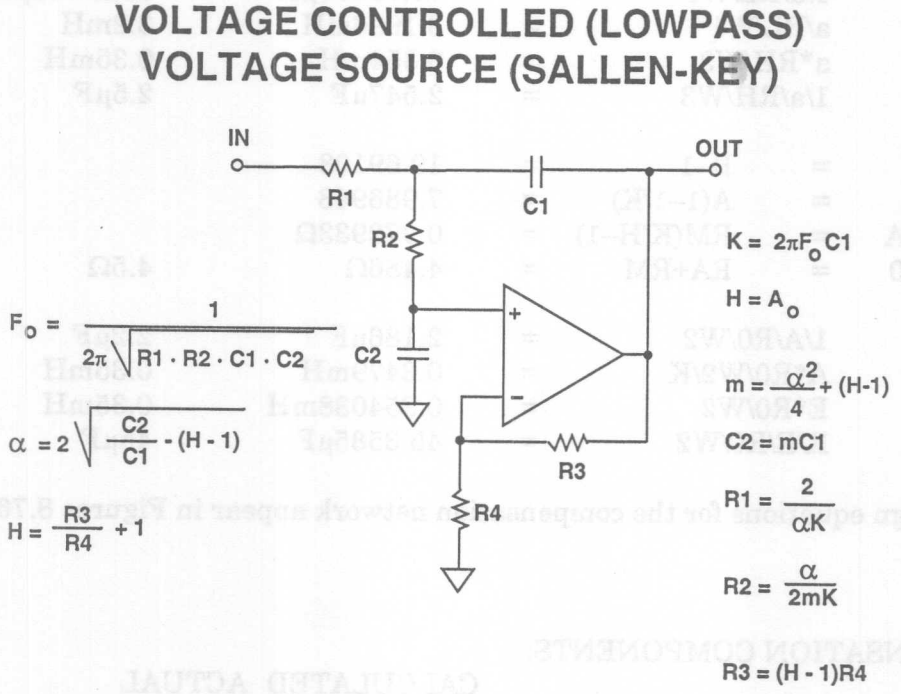


Figure 8.86

LOWPASS DESIGN

SECTION 1, 319 Hz:

Choose	C1	=	0.1μF	
	k	=	2*PI*F0*C1	
		=	200.4×10^{-6}	
	m	=	$\alpha^2/4 + (H-1)$	
		=	1	
	C2	=	m*C1	
		=	0.1 μF	
	R1	=	2/(α*k)	
		=	4.989kΩ	use 4.99kΩ
	R2	=	α/(2*m*k)	
		=	4.989kΩ	use 4.99kΩ

Since we cannot get the exact value required for the resistors and we don't particularly care what the exact crossover frequency is, we will calculate the exact frequency and use it for subsequent calculations.

F1	=	1/[2*PI*SQRT(R1*R2*C1*C2)]
	=	319 Hz

SECTION 2, 5300 Hz:

Choose	C1	=	1000 pF	
	k	=	33.30×10^{-6}	
	m	=	1	
	C2	=	1000 pF	
	R1	=	30.03kΩ	use 30.1kΩ
	R2	=	30.03kΩ	use 30.1kΩ

Again, we calculate the actual frequency value.

F2 = 5287 Hz.

HIGHPASS SECTIONS

HIGHPASS SECTION (SALLEN-KEY)

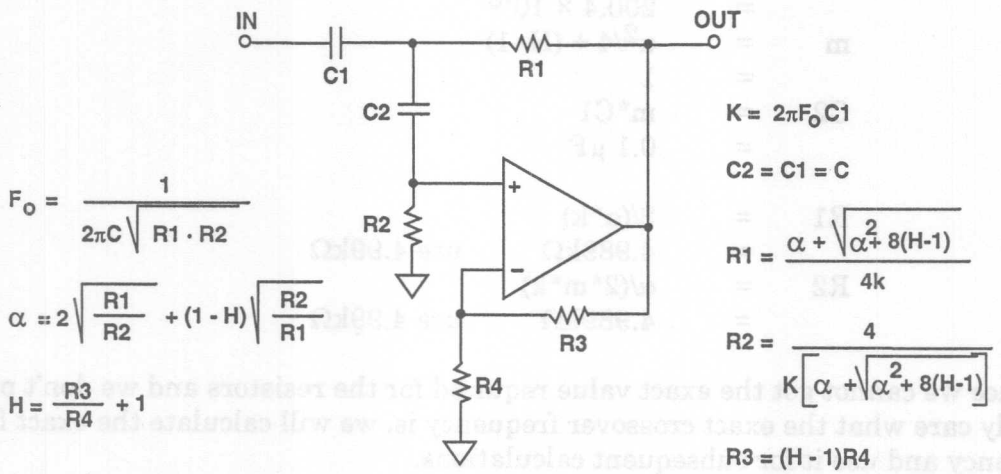


Figure 8.87

SECTION 3, 319 Hz:

Choose	C	=	0.1μF	
	k	=	200×10^{-6}	
	m	=	1	
	R1	=	(1/4k)*[α+SQRT(α^2+8(H–1)]	
		=	(1/4k)*[α+SQRT(α^2)]	
		=	α/2k	
		=	4.989kΩ	use 4.99kΩ
	R2	=	(4/k)/[α+SQRT(α^2+8(H–1))]	
		=	2/αk	
		=	4.989kΩ	use 4.99kΩ

SECTION 4, 5270 Hz:

Choose	C	=	1000pF	
	k	=	33.11×10^{-6}	
	m	=	0.25	
	R1	=	15.1kΩ	use 15kΩ
	R2	=	60.4kΩ	

ACTIVE CROSSOVER NETWORK

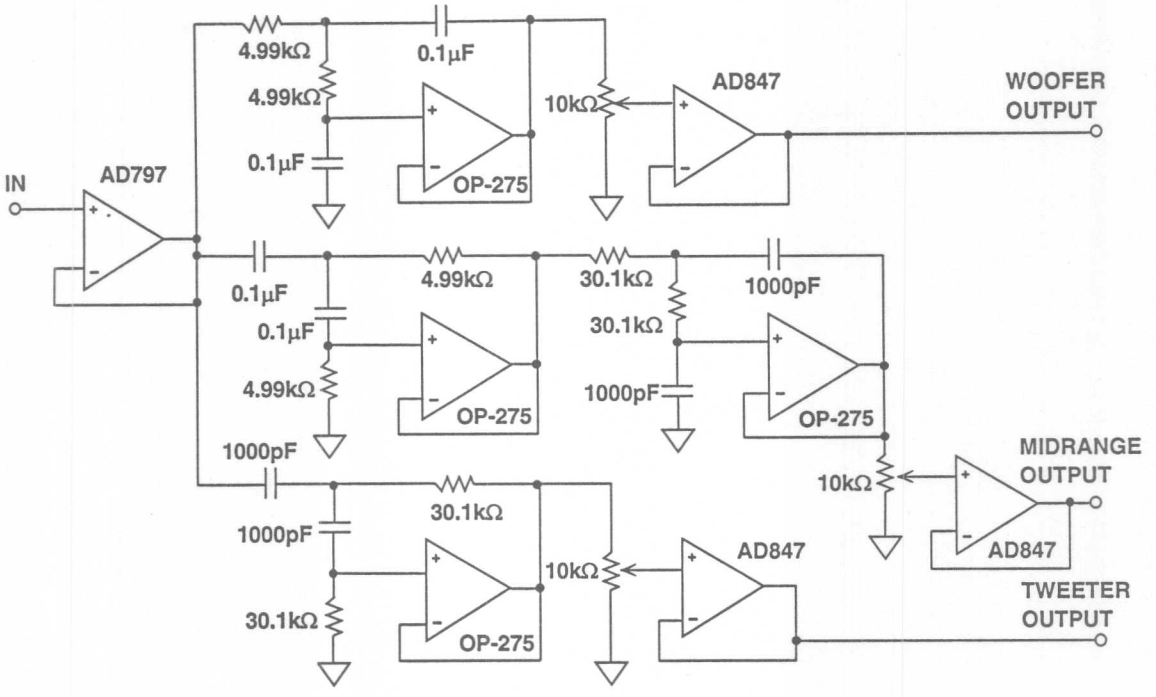


Figure 8.88

ACTIVE CROSSOVER FREQUENCY RESPONSE

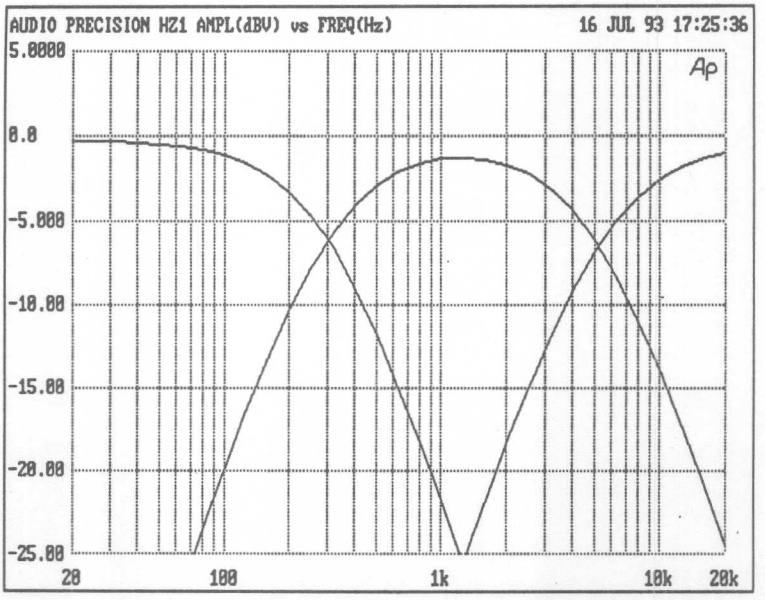


Figure 8.89

DIGITAL AUDIO APPLICATIONS
Walt Kester

Activities related to studio recording are complex and varied. Generally, many channels are used, with each dedicated to one or more signal sources (instruments/voices). All channels need not be recorded at the same time. Each channel is subjected to extensive processing such as gain control, filtering, nonlinear compression or expansion, reverberation, spectral equalization, and other special-effects enhancements. The channels are then mixed together to obtain a final arrangement with the desired overall effect.

Traditionally, channel processing and mixing were implemented entirely in the analog domain—with numerous disadvantages. Each channel's information—stored as an analog signal on magnetic tape—degrades as the cutting, splicing, and re-recording process progresses, undermining the benefits of the processing. The limited performance range available with analog processing sets a ceiling on the signal enhancement that can be obtained. Also, analog circuitry can only handle one channel at a time; multi-channel mixers are expensive and difficult to control. Finally, if analog processing hardware is used, overall mixing flexibility can be achieved only through hardware modifications. In practice, this means that the mixing process loses its ability to creatively explore special effects.

DIGITAL AUDIO STUDIO TECHNIQUES

- Digital Recording: 16, 18 or 20 Bits for ADC
- Digital Mixing
- Gain Control
- Reverberation and Special Effects
- Equalization using Digital Filters

Figure 8.90

Increasingly, audio processing is relying on digital techniques to improve audio quality. The first step in this transition was digital recording, which became prevalent in the early 1980s. Audio signals are converted to digital form before being stored on magnetic tape. Digital recording eliminates several sources of degradation that affect analog recordings, including the effects of non-linearities and additive noise in the magnetic materials used for recording, and wow and flutter in the tape playback mechanism.

In studio mixing applications, however, digital recording does not eliminate all complications. In the mixing and enhancement process, information is passed from one tape to another—requiring both ADCs and DACs, a source of noise. These conversions are no longer necessary if all processing and mixing are handled with DSP techniques.

In the DSP-based studio recording system shown in Figure 8.91, signals are digitized as early as possible, usually to 16, 18, or 20-bit resolution. After conversion, the audio processing is handled digitally with high performance DSP processors. Gain factors are handled with digital multiplication. Filtering and equalization can be handled with linear-phase FIR filters. Dynamic-range control is easily included in the system by using a multiplier for non-linear compression/expansion computations.

DIGITAL AUDIO STUDIO SYSTEM

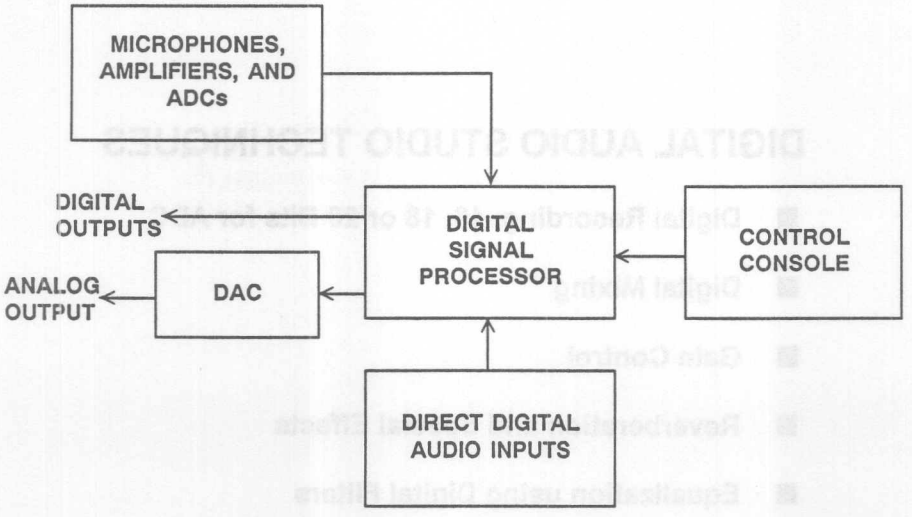


Figure 8.91

The traditional mixing process is also easily implemented with DSP. Digital channels to be mixed are simply added together. Delays can be introduced easily into channels, allowing phase delays to be equalized. Channel interconnections—which must be hardwired in an analog processor—can be reconfigured easily in a DSP system.

In addition to improving on traditional systems, a DSP studio recording system opens up numerous new options. Unusual special effects are readily included in the system. Reverberation effects can be modeled, simulated, and integrated into the final recording. Digital reverberation can give concert hall or cathedral ambience to what might have been recorded in a dry studio. An FFT routine's spectral analysis of the signal can form the basis for adaptive digital filters that provide optimal equalization.

With the advent of compact disc (CD) and digital audio tape (DAT) players, there is no requirement for digital-to-analog conversion anywhere in the studio recording process, except for monitoring. The final digital recording can be transferred directly to the CD or DAT in digital form with no loss in fidelity.

Although 18 and 20-bit ADCs may be used in the recording process, the standard for CD and DAT has been set at 16 bits. Additional bits may be used in the DSP studio processing to allow for roundoff errors, overflows, etc., but the final recording is truncated to 16 bits per sample on the CD or DAT. The sampling-rate standard for CD recordings is 44.1kSPS, and 48kSPS for DAT.

DIGITAL AUDIO RECORDING STANDARDS

- 16-20 bits ADC Resolution, Truncated to 16 bits for Compact Disc
- 44.1kSPS Sampling Rate for CD Players
- 48kSPS Sampling Rate for Digital Audio Tape (DAT) Players

Figure 8.92

Performance of audio systems is primarily measured in terms of three dynamic specifications: Total harmonic distortion plus noise (THD+N), D-Range distortion, and signal-to-noise ratio. These are defined in Figure 8.93.

KEY AUDIO PERFORMANCE SPECIFICATIONS

- **THD + N: Ratio of the Power of the Values of the Harmonics and Noise to the Power of the Fundamental Input Frequency Expressed in % or dB**
- **D-Range Distortion: Ratio of the Distortion Plus Noise to the Signal at a Signal Amplitude of -60dB FS. Add 60dB to the Ratio to Obtain D-Range Distortion Value**
- **Signal-to-Noise Ratio: Ratio of the Output Power with No Signal Present to the Output Power at Fullscale**

Figure 8.93

THE AD1879 18 BIT SIGMA-DELTA AUDIO ADC

The AD1879 is a dual 18 bit sigma-delta ADC designed to meet the stringent requirements of professional digital audio. A block diagram of the device is shown in Figure 8.94, and performance specifications are summarized in Figure 8.95. The input sigma-delta modulator is a fifth-order differential switched capacitor design which performs the quantization noise shaping function. The oversampling ratio is 64x, which places the oversampling frequency at 3.072MHz for the standard audio sampling rate of 48kSPS. Because of the high oversampling ratio, a single-pole analog antialiasing filter is sufficient at the input of the ADC. For less exacting applications, the AD1878 is a 16-bit version of the AD1879.

AD1879 DUAL 18-BIT SIGMA-DELTA AUDIO ADC

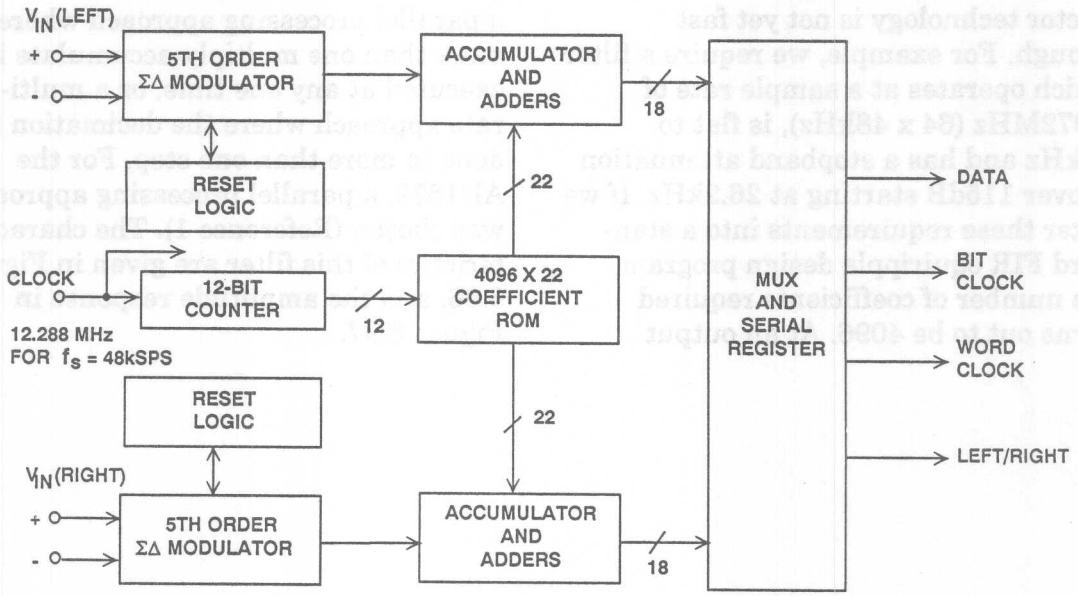


Figure 8.94

AD1879 18 BIT SIGMA-DELTA ADC KEY SPECIFICATIONS

- Two 18 Bit Channels for Stereo Digital Audio
- Interchannel Crosstalk: -110dB at 1kHz
- SNR: 104dB
- THD: 100dB
- Oversampling Ratio: 64x
- Output Word Rate: 55kHz Maximum
- Linear Phase Digital Filter
- Power: 900mW
- 28 Pin, 600-mil Plastic Package

Figure 8.95

For audio ADCs such as the AD1879, the digital lowpass filter cannot be implemented using standard multiply-accumulate structures because semiconductor technology is not yet fast enough. For example, we require a filter which operates at a sample rate of 3.072MHz (64 x 48kHz), is flat to 20kHz and has a stopband attenuation of over 115dB starting at 26.2kHz. If we enter these requirements into a standard FIR equiripple design program, the number of coefficients required turns out to be 4096. At an output sample rate of 48kHz, we would require a multiply-accumulate time of 5.1ns. This is too fast for a standard FIR filter structure. Therefore we must use either a parallel processing approach where more than one multiply-accumulate is executed at any one time, or a multi-rate approach where the decimation is done in more than one step. For the AD1879, a parallel processing approach was chosen (Reference 1). The characteristics of this filter are given in Figure 8.96, and the amplitude response in Figure 8.97.

AD1879 DIGITAL FILTER CHARACTERISTICS

- Stopband Attenuation: 118dB
- Passband Ripple: ± 0.0008dB
- Cutoff Frequency (48kHz output rate): 21.7kHz
- Stopband Frequency (48kHz output rate): 26.2kHz
- Number of Parallel Accumulators: 64 27-bit accumulators
- Coefficient Wordlength: 22bits
- Number of Taps: 4096

Figure 8.96

AD1879 DIGITAL FILTER RESPONSE

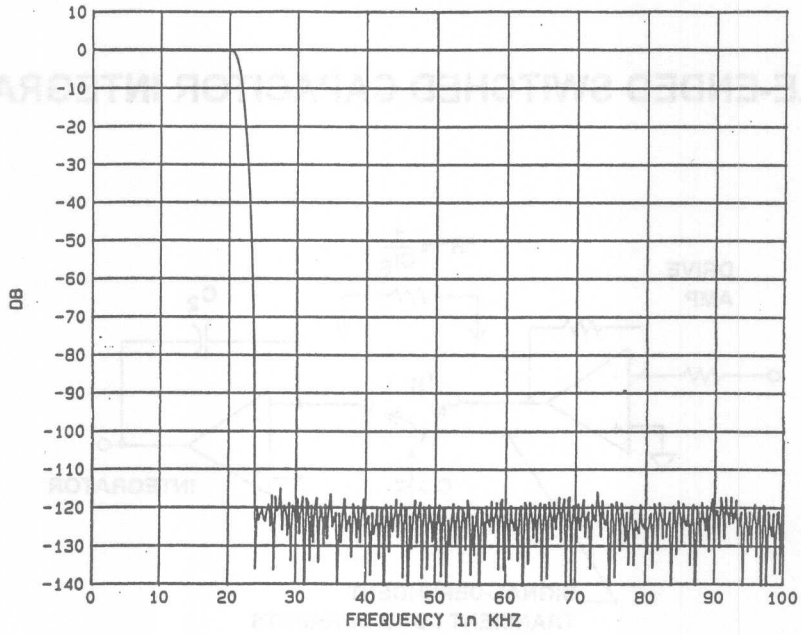


Figure 8.97

The AD1879 switched capacitor input circuit presents a special set of problems for the drive amplifier because of signal-dependent transient input currents. In order to understand the phenomenon better, Figure 8.98 shows the basic circuit for a single-ended switched capacitor integrator. The capacitor is switched at the oversampling rate, f_S, and acts as a resistor having a resistance equal to $1/Cf_S$. The integrator time constant is therefore determined by capacitance *ratios* which can be accurately controlled in a CMOS process. The switched capacitor is implemented in CMOS using the T-switch circuit shown in Figure 8.99. Because the input signal to the switch modulates the FET bias voltages, the charge injected into the drive amplifier is signal dependent.

SINGLE-ENDED SWITCHED CAPACITOR INTEGRATOR

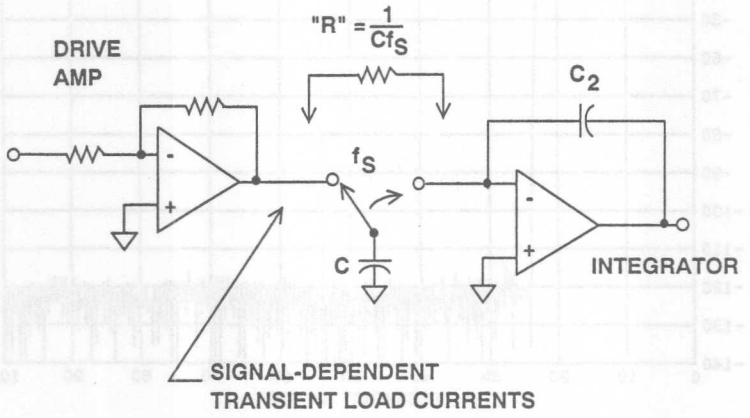


Figure 8.98

CMOS IMPLEMENTATION OF SWITCHED CAPACITOR

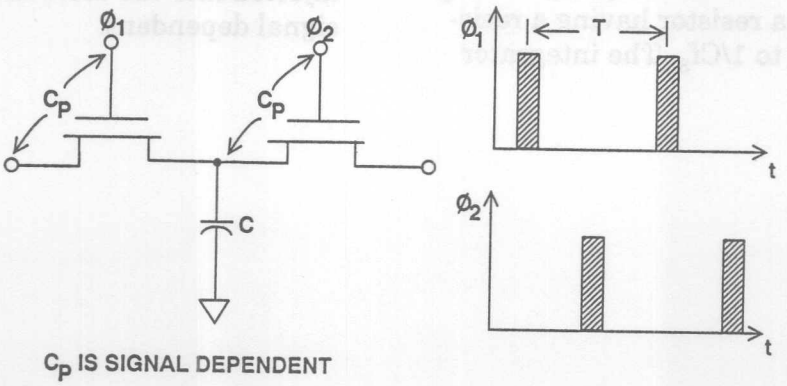


Figure 8.99

The sigma-delta modulator in the AD1879 is fully differential and has the equivalent input circuit shown in Figure 8.100 (only one input channel shown). For optimum common mode rejection of transient load currents, the input should be driven differentially. The differentially connected 0.0047μF capacitor supplies most of the differential-mode transient currents, while the 0.01μF capacitors connected to ground absorb spike currents which are common mode. The 51Ω series resistors isolate the remaining transient current from the drive amplifiers as well as isolate the capacitive loads from the op amp outputs. These resistors must be small, however, in order to avoid distortion because of the signal-dependent transients caused by charge injection. The OP-275 (dual) op amp is recommended as a suitable precision low-distortion drive amplifier.

DIFFERENTIAL DRIVER (ONE CHANNEL) FOR AD1879 SIGMA-DELTA AUDIO ADC

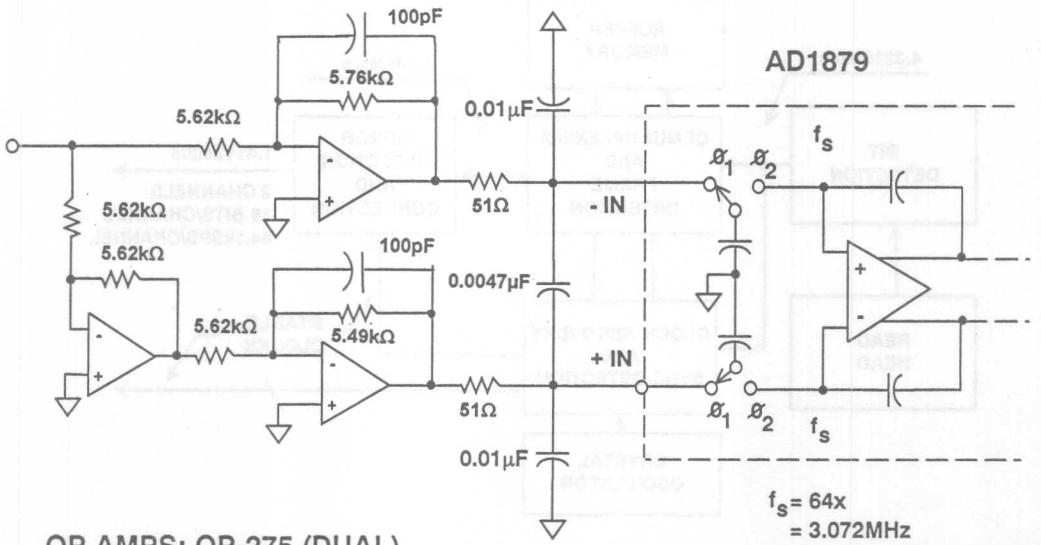


Figure 8.100

APPLICATIONS FOR AUDIO DACS IN COMPACT DISC (CD) PLAYER ELECTRONICS

A simplified block diagram of the read electronics for a typical CD player is shown in Figure 8.101. The read electronics takes the data from the CD read head and performs the necessary data qualification, error detection and error correction. Data from the read electronics is in serial format, 16 bits per sample, at an effective sampling rate of 44.1kHz per channel. Data for the two channels is usually multiplexed in a single 1.4112MHz bit stream. In theory, it is possible to reconstruct the audio signal using two 16-bit DACs preceded by a digital demultiplexer and parallel-to-serial converters operating at an update rate of 44.1kHz followed by analog anti-imaging filters.

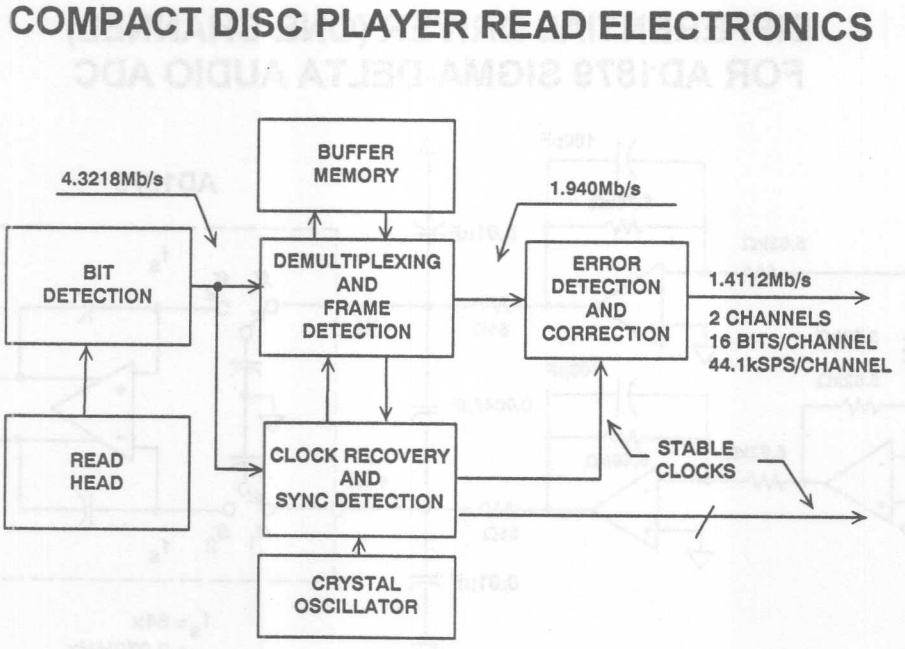


Figure 8.101

First-generation CD players used this approach as shown in Figure 8.102. An alternative is a single 16 bit DAC with output multiplexing for left and right channel. But sampling at 44.1kHz places severe requirements on the antialiasing filters. The audio bandwidth extends from 20Hz to 20,000Hz, and the filters must exhibit a flat frequency response over this frequency. In order to prevent aliasing, the filters must have at least 40dB to 50dB attenuation at 22.05kHz which implies a complicated and costly 9- to 13-pole analog filter. Higher-order filters typically have non-linear phase response which is undesirable in audio applications. For this reason, the principles of oversampling and digital filtering are now in widespread use to simplify the design of the analog filter as well as increase the overall signal-to-noise ratio.

FIRST-GENERATION CD PLAYER RECONSTRUCTION ELECTRONICS

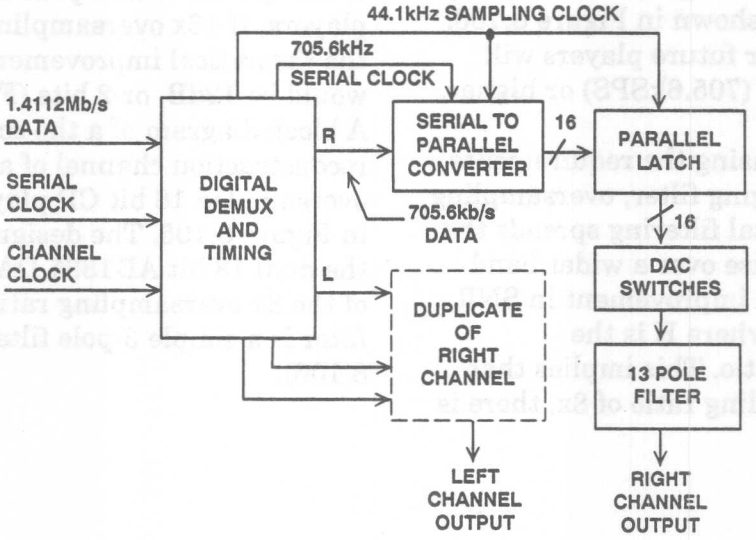


Figure 8.102

8X OVERSAMPLED 18-BIT CD PLAYER RECONSTRUCTION ELECTRONICS

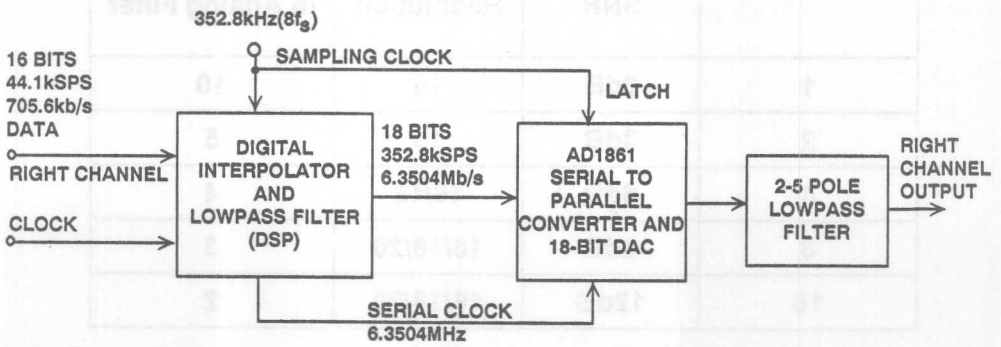


Figure 8.103

Second-generation CD players typically used oversampling ratios of 2x (88.2kSPS) or 4x(176.4kSPS) in conjunction with linear phase FIR digital interpolation filter chips. Third-generation players are using 8x oversampling (352.8kSPS) as shown in Figure 8.103, and the trend for future players will probably be 16x (705.6kSPS) or higher.

In addition to easing the requirements on the anti-imaging filter, oversampling followed by digital filtering spreads the quantization noise over a wider bandwidth, giving an improvement in SNR of 10 $\log_{10}$(K), where K is the oversampling ratio. This implies that for an oversampling ratio of 8x, there is a theoretical 9dB (or 1.5bits) improvement in SNR. It is possible to carry the arithmetic in the digital interpolation filter out to 18 bits, drive an 18-bit audio DAC with the result, and realize this improvement in practical CD players. If 16x oversampling were used, the theoretical improvement in SNR would be 12dB, or 2 bits (Figure 8.104). A block diagram of a the complete reconstruction channel of an 8x oversampled 18 bit CD player is shown in Figure 8.105. The design is based on the dual 18 bit AD1865 DAC. Because of the 8x oversampling ratio, the output filter is a simple 3-pole filter (Figure 8.106).

EFFECTS OF OVERSAMPLING AND DIGITAL FILTERING ON CD PLAYER DESIGN

Oversampling Ratio K	Theoretical Increase in SNR	Useful Bits of DAC Resolution	Number of Poles Required in Analog Filter
1	0dB	16	10
2	3dB	16	5
4	6dB	16/18	4
8	9dB	16/18/20	3
16	12dB	16/18/20	2

Figure 8.104

8X OVERSAMPLED CD PLAYER RECONSTRUCTION ELECTRONICS USING AD1865 DUAL 18-BIT AUDIO DAC

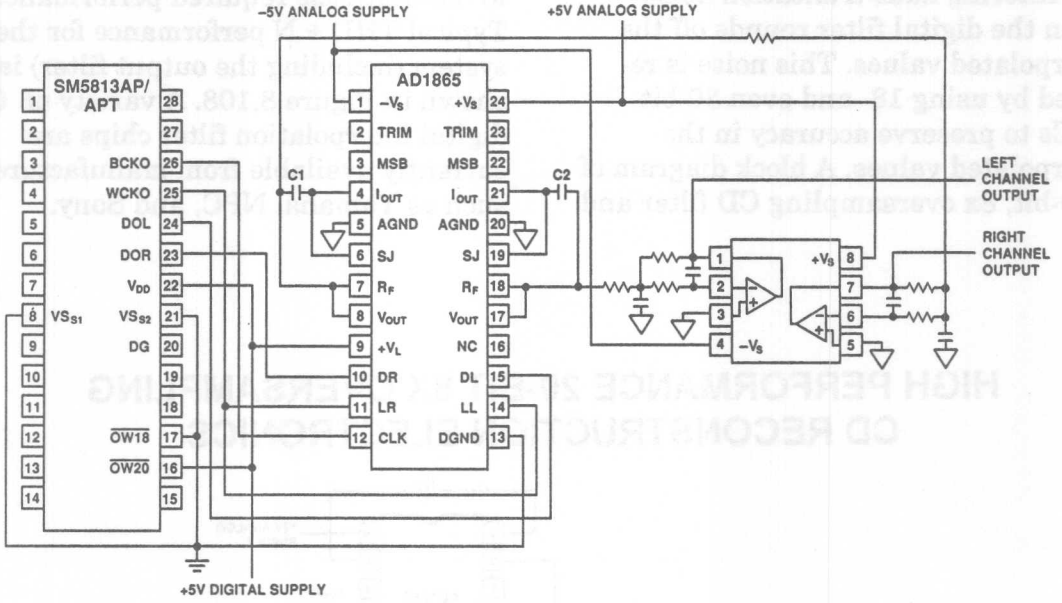


Figure 8.105

3-POLE ANTIALIASING FILTER FOR 18-BIT, 8X OVERSAMPLING

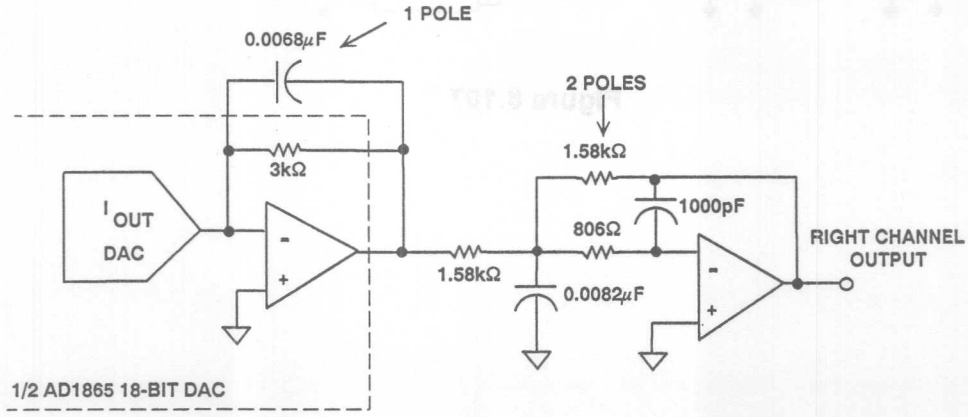


Figure 8.106

An additional reason for using DACs with greater than 16-bit resolution is that the process of digital interpolation and filtering adds truncation noise when the digital filter rounds off the interpolated values. This noise is reduced by using 18- and even 20-bit DACs to preserve accuracy in the interpolated values. A block diagram of a 20-bit, 8x oversampling CD filter and DAC configuration is shown in Figure 8.107. Because of the 8x oversampling ratio, a 5-pole lowpass filter is sufficient to maintain the required performance. Typical THD + N performance for the system (including the output filter) is shown in Figure 8.108. A variety of CD digital interpolation filter chips are currently available from manufacturers such as Yamaha, NPC, and Sony.

HIGH PERFORMANCE 20-BIT 8X OVERSAMPLING CD RECONSTRUCTION ELECTRONICS

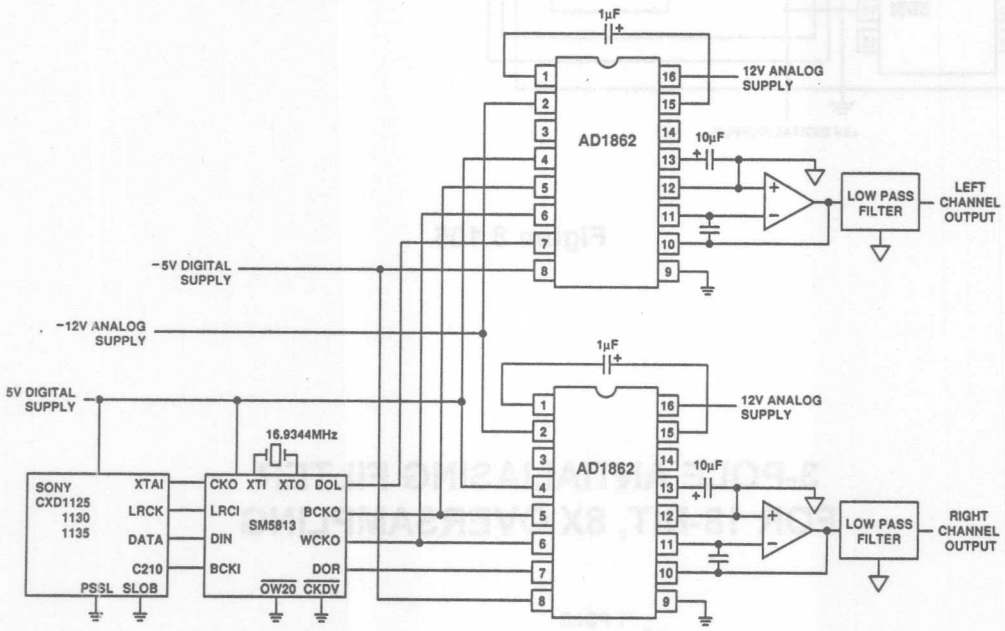


Figure 8.107

THD + N PERFORMANCE OF 20-BIT, 8X OVERSAMPLING CD ELECTRONICS USING THE AD1862 AUDIO DAC

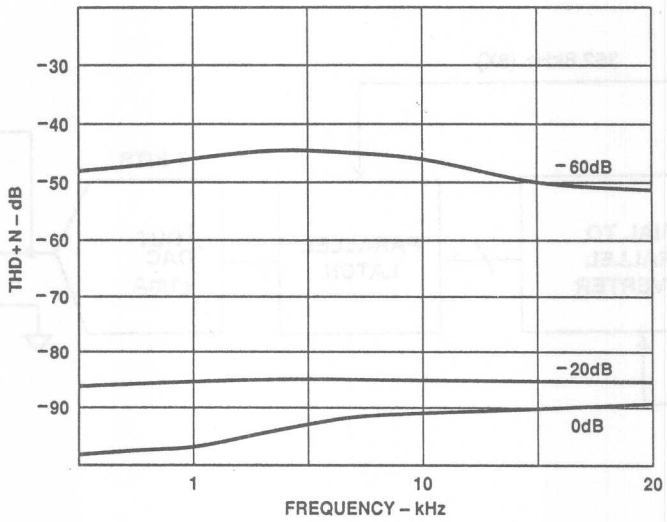


Figure 8.108

There are a number of audio DACs currently available on the market ranging from 16 to 20-bit resolution. Newer devices are capable of sampling rates up to 768kSPS, allowing 16x oversampling. Unlike traditional DACs, audio DACs are specified in terms of ac parameters such as THD + N, SNR, and D-Range Distortion because traditional dc specifications are not critical for audio applications. Audio DACs accept serial inputs and have internal serial-to-parallel converters followed by a parallel latch. Two clock inputs are therefore required to operate an audio DAC. A serial clock is needed to strobe the serial data into the serial-to-parallel converter, and a latch-enable clock is required to strobe the parallel latch. A simplified block diagram of a typical digital audio DAC is shown in Figure 8.109.

TYPICAL CD AUDIO DAC (SINGLE CHANNEL, 18 BITS, 8X OVERSAMPLING)

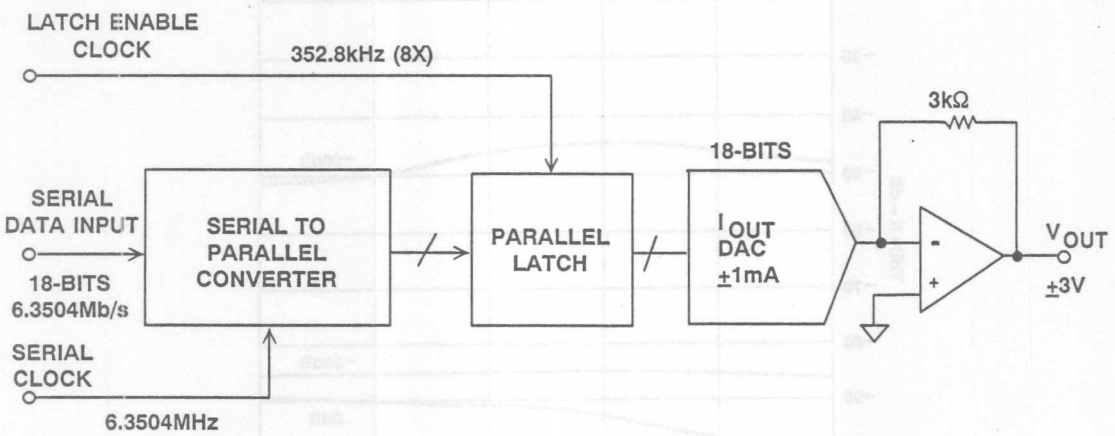


Figure 8.109

DAC ARCHITECTURES

CMOS DACs for audio applications are often based on the current-mode steering circuit shown in Figure 8.110. An external reference is applied to the V_{ref} pin, and the R-2R ladder divides the input current I into binary-weighted currents as shown. The output drives the virtual ground of an inverting op amp. The finite "on" resistance of the FET switches is compensated for by placing an equivalent compensating FET in series with the feedback resistor R.

For high-performance DACs in the voiceband and audio range, BiMOS processes (bipolar and CMOS devices on the same process) offer the advantages of low-power CMOS for the digital circuits (such as parallel-to-serial converters and latches) along with the low-glitch fast-switching performance of bipolar transistors. A typical current switch cell for such a DAC (the AD1861 18-bit audio DAC) is shown in Figure 8.111. The outputs of CMOS latches are level shifted by the two FETs and converted into a low-level ±0.8V differential drive for the NPN differential pair.

CURRENT-STEERING CMOS DAC

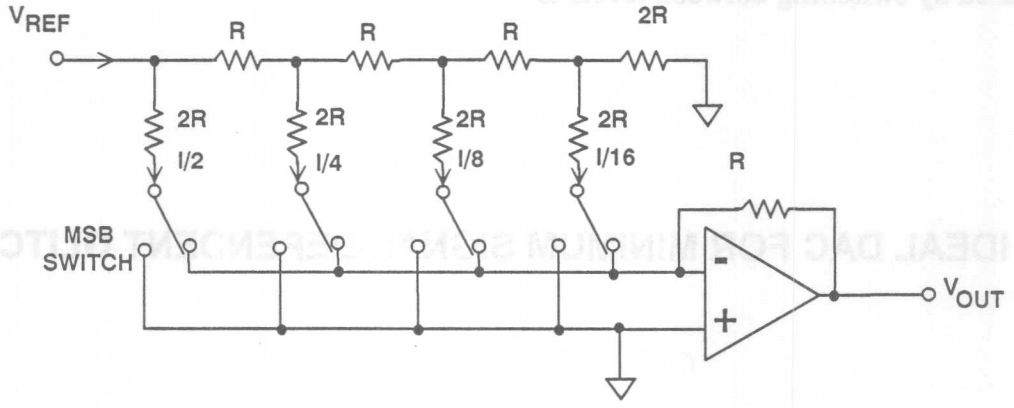


Figure 8.110

BiMOS CURRENT SWITCH

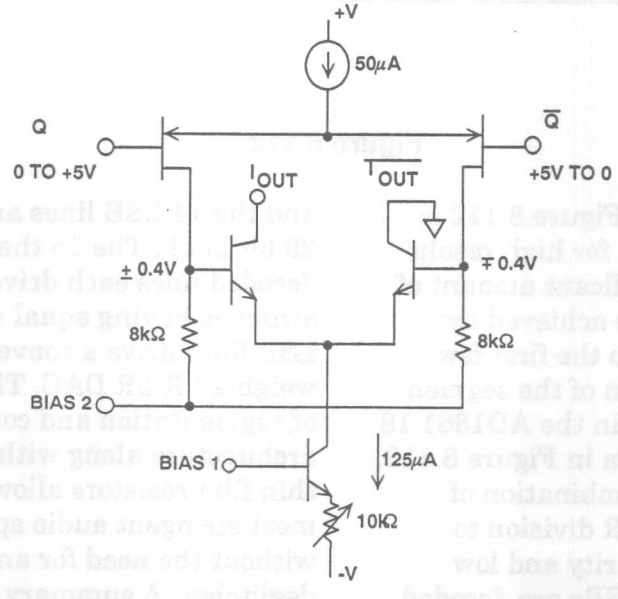


Figure 8.111

GLITCH REDUCTION BY SEGMENTATION

If real estate, cost, power, and capacitance were of no consideration, the ideal "glitchless" DAC would consist of $2^N - 1$ equally weighted current switches preceded by latches and decoding logic as shown in Figure 8.112. The glitch produced by switching between levels is code-independent and, therefore, does not generate harmonics of the sinewave being reconstructed. A set of latches is required after the binary decoding logic in order to equalize the delays to the actual switches themselves.

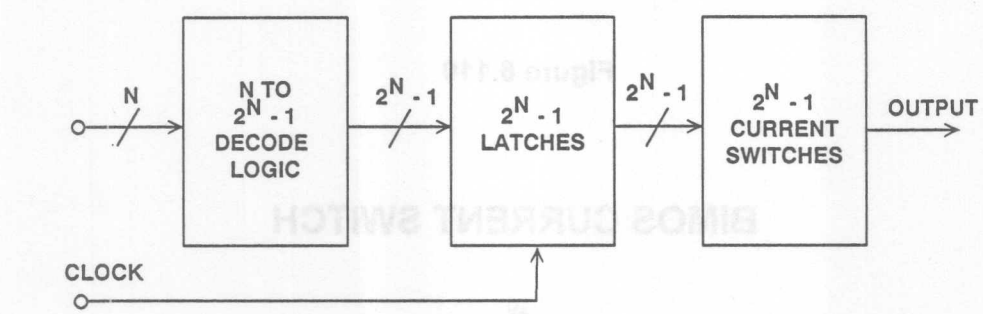


Figure 8.112

The scheme shown in Figure 8.112 is obviously not practical for high resolution DACs, but a significant amount of glitch reduction can be achieved by applying the concept to the first few MSBs. A block diagram of the segmentation technique used in the AD1861 18 bit audio DAC is shown in Figure 8.113. The AD1861 uses a combination of segmentation and R-2R division to achieve excellent linearity and low distortion. The four MSBs are decoded into a 15 bit "thermometer" code after the serial-to-parallel conversion. The 15 decoded lines (representing the 4 MSBs) and the 14 LSB lines are then fed to a 29 bit latch. The 15 thermometer decoded lines each drive current switches having equal weights. The 14 LSB lines drive a conventional binary-weighted R-2R DAC. This combination of segmentation and conventional R-2R architecture along with laser trimmed thin film resistors allows the AD1861 to meet stringent audio specifications without the need for an external SHA deglitcher. A summary of key performance specifications for the AD1861 is given in Figure 8.114.

SEGMENTATION IN THE AD1861 18-BIT AUDIO DAC

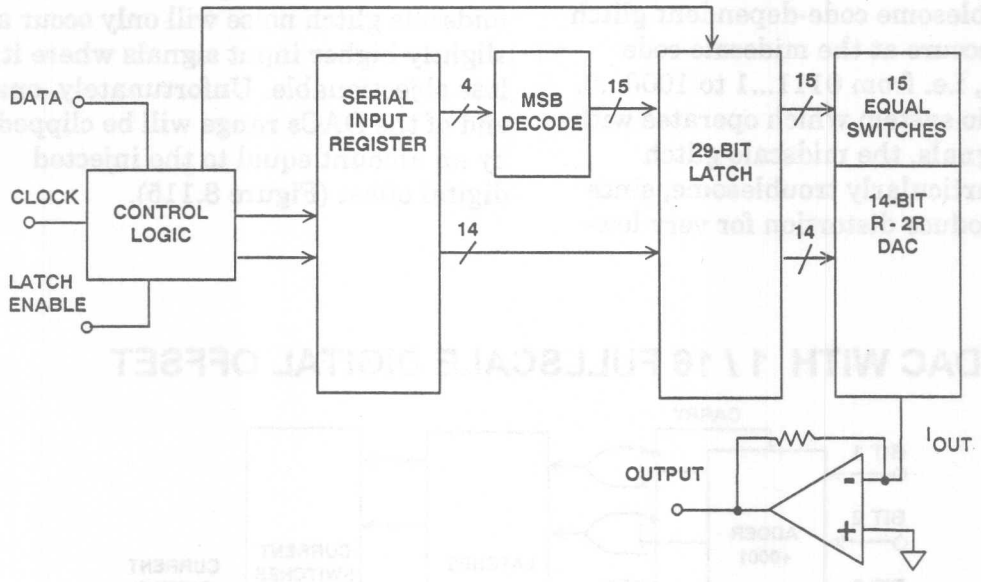


Figure 8.113

AD1861 18-BIT AUDIO DAC KEY SPECIFICATIONS

- 108dB SNR
- 0.002% THD + N @ 0dB Signal Amplitude
- Up to 16x Oversampling Capability (768kSPS)
- ±3V or ±1mA Output Capability
- 110mW Power Dissipation
- 16 Pin DIP Package

Figure 8.114

AUDIO DAC GLITCH REDUCTION USING DIGITAL OFFSET

Regardless of the architecture used to design a high performance DAC, the most troublesome code-dependent glitch typically occurs at the midscale code transition, i.e. from 0111...1 to 1000...0. In an audio system which operates with bipolar signals, the midscale glitch noise is particularly troublesome, since it can introduce distortion for very low-level passages. If a small digital offset is added to the DAC input, then the DAC midscale glitch noise will only occur at slightly higher input signals where it is less objectionable. Unfortunately, one end of the DACs range will be clipped by an amount equal to the injected digital offset (Figure 8.115).

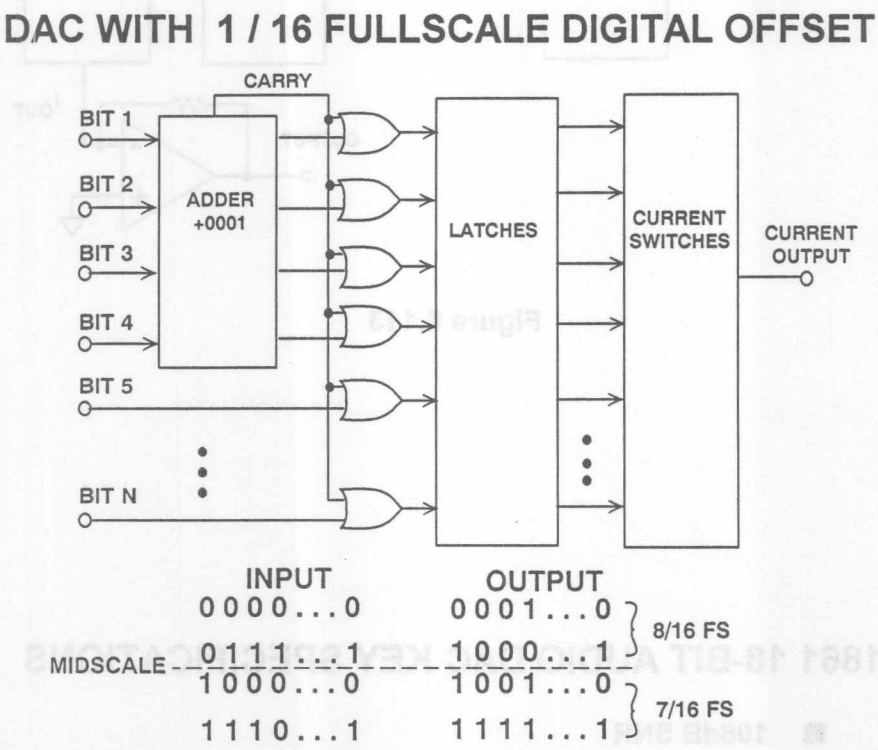


Figure 8.115

The AD1862 20 bit digital audio DAC uses a combination of segmentation and digital offset to achieve a high level of performance. The novel architecture prevents clipping and allows the full range of the 20 bit DAC to be utilized. A block diagram of the AD1862 is shown in Figure 8.116. The digital offset is accomplished by adding 0001 (1/16th fullscale) to the four MSBs. The three MSBs are then segmented into a 7 bit thermometer code output which is latched and then drives seven equal current switches. Bit 4 (after the addition), and bits 5 through 20 are latched and then drive a conventional R-2R DAC. In order to prevent clipping at the positive end of the range, the carry

output of the adder drives an additional current switch having a weight corresponding to bit 4. Finally, an offset current equal to 1/16th fullscale is subtracted from the DAC output to compensate for the constant digital offset. This architecture results in exceptional THD + N performance as shown in Figure 8.117. Key specifications for the AD1862 are summarized in Figure 8.118.

AD1862 20-BIT AUDIO DAC USES DIGITAL OFFSET AND SEGMENTATION

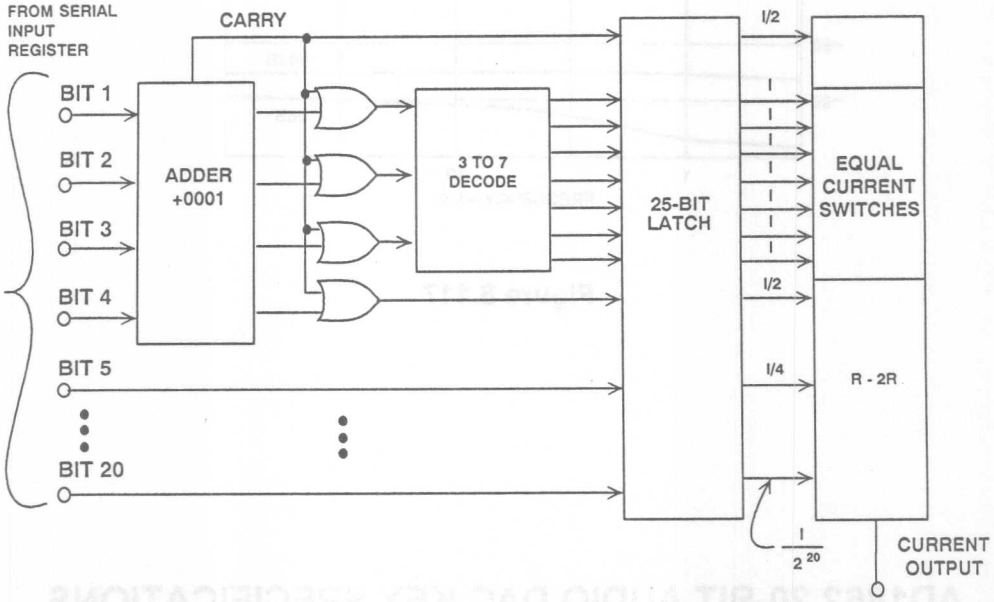


Figure 8.116

THD + N VERSUS INPUT FREQUENCY FOR AD1862 20-BIT AUDIO DAC

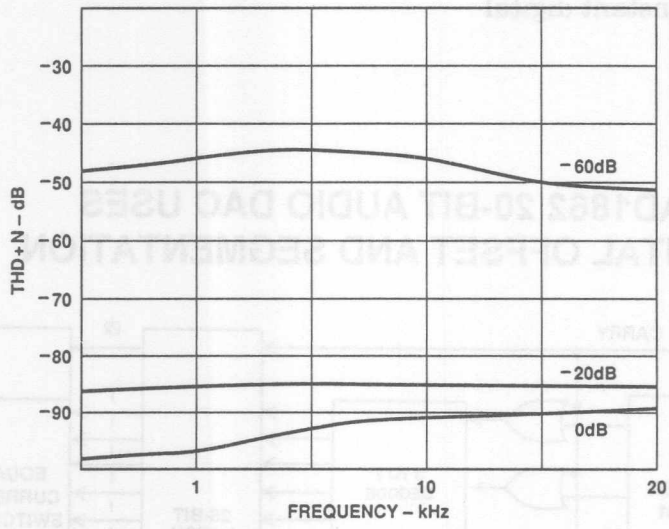


Figure 8.117

AD1862 20-BIT AUDIO DAC KEY SPECIFICATIONS

- 119dB SNR
- 0.0012% THD + N @ 0dB Signal Amplitude
- 16× Oversampling Capability (705.6kSPS)
- ±1dB Gain Linearity @ –90dB Amplitude
- ±1mA Output Current
- 288mW Power Dissipation
- 16 Pin DIP Package

Figure 8.118

STEREO CODECS FOR MULTIMEDIA AND BUSINESS AUDIO APPLICATIONS

David Fair

The AD1848 and AD1849 16-bit SoundPort® Stereo Codecs (coder/decoder) bring "audio system on a chip" integration to computer applications for multimedia sound and business audio. Operating from a single +5V supply, they allow sophisticated digital audio functions to be incorporated on PC or workstation motherboards or add-in boards easily and at low cost.

Both codecs include a stereo sigma-delta ADC and DAC, with their 1-bit, high-sampling-rate analog interface. They achieve a dynamic range of 80dB with total harmonic distortion plus noise of –74dB over the 0-to-20kHz audio band. They are fabricated in a digital CMOS process enhanced with a second layer of polysilicon to facilitate high-performance capacitor formation.

These codecs offer far more than just two pairs of integrated converters. On-chip oscillators provide for software selection of all the key multimedia sample rates from 5,500 samples/second to 48kSPS, via software selection of one of two external crystals and the appropriate division ratio; an external clock may also be supplied. Signal filters are provided on-chip to simplify design and reduce expense and space requirements. The sigma-delta a/d converters incorporate their own digital decimation filters with maximum ±0.1-dB passband ripple. The d/a converters are preceded by an integral interpolation filter in the digital domain and followed by switched-capacitor and continuous-time analog filters to remove Nyquist images. No external references are required; they are included on the SoundPort codec chips.

In addition, both devices allow independent control of left- and right-channel input gain in 1.5dB steps, from 0 to +22.5dB. Microphone inputs have access to an additional +20dB gain block. Left- and right-channel outputs can be attenuated from 0 dB to –94.5dB, in 1.5dB steps, or muted (shut off) entirely. Both codecs support mixing of the a/d converter's output with the d/a converter's input for audio overlay ("karaoke" operation) under software control. The devices support pulse-code-modulated (PCM) 16-bit linear, 8-bit companded μ-law, and 8-bit companded A-law data formats.

The AD1848 and AD1849 SoundPort codecs are basically similar; they differ principally in their digital interface. The AD1848 (Figure 8.119) has a byte-wide *parallel* data/control port that supports a buffered direct connection to the Industry Standard Architecture (ISA) or "PC-AT" bus. This AD1848 was

specified in a joint agreement between Analog Devices, Inc., Compaq Computer Corp., and Microsoft. Its objective was to provide the lowest cost and simplest implementation of digital audio capabilities in an ISA-bus system. Key specifications for the AD1848 and AD1849 are shown in Figure 8.120.

AD1848 PARALLEL-PORT 16-BIT SoundPort® STEREO CODEC

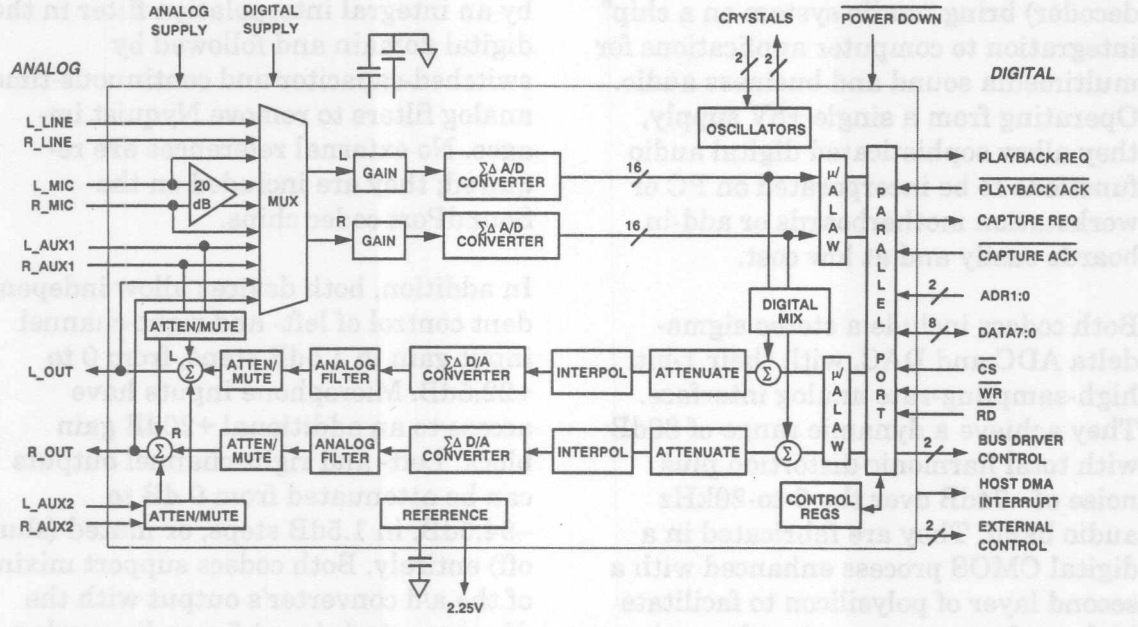


Figure 8.119

AD1848/AD1849 AUDIO CODEC KEY FEATURES

- Single-Chip Integrated Sigma-Delta "Audio System-on-a-Chip"
- Dynamic Range of 80dB, THD + N of -74dB
- 5.5kHz to 48kHz Sampling Rates
- On-chip Signal Filters:
  - Digital decimation and interpolation
  - Analog output lowpass anti-imaging
- Programmable Gain and Attenuation
- 16-bit PCM linear or μ-law / A-law companded data
- On-chip voltage reference and oscillators
- Operation from single +5V supply

Figure 8.120

Compaq uses the AD1848 in the newly announced DESKPRO® computers, and Microsoft uses it in their Windows Sound System® board. Since the precision AD1848 audio system cannot be expected to drive the capacitance of the ISA bus directly, the interface uses an external '245-type digital bus transceiver for current buffering—but under control of the AD1848; it provides the Enable and Direction signals for the transceiver (Figure 8.121).

INTERFACING THE AD1848 CODEC TO THE ISA COMPUTER BUS

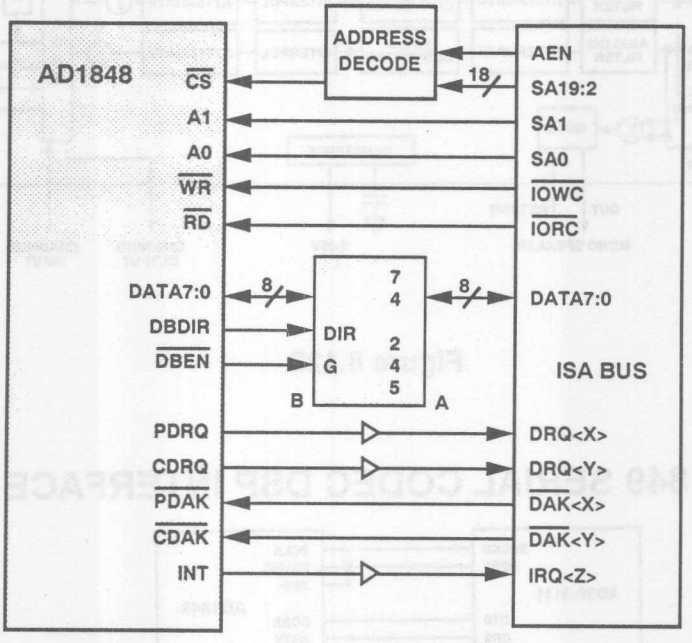


Figure 8.121

In contrast, the AD1849 (Figure 8.122) uses a *serial* interface for data and control information. This SoundPort was developed to meet the needs of Sun Microsystems Corporation's SPARCstation 10 series of UNIX workstations. Sun's original requirement for the serial interface was that it connect with the ISDN bus employed in these new SPARCstations using minimal translation logic. Fortunately, the serial interface is general enough to allow direct or very simple connection to the serial ports of digital signal processors, including popular members of the ADSP-2100 family—as well as DSPs from other vendors as shown in Figure 8.123.

AD1849 SERIAL-PORT 16-BIT SoundPort® STEREO CODEC

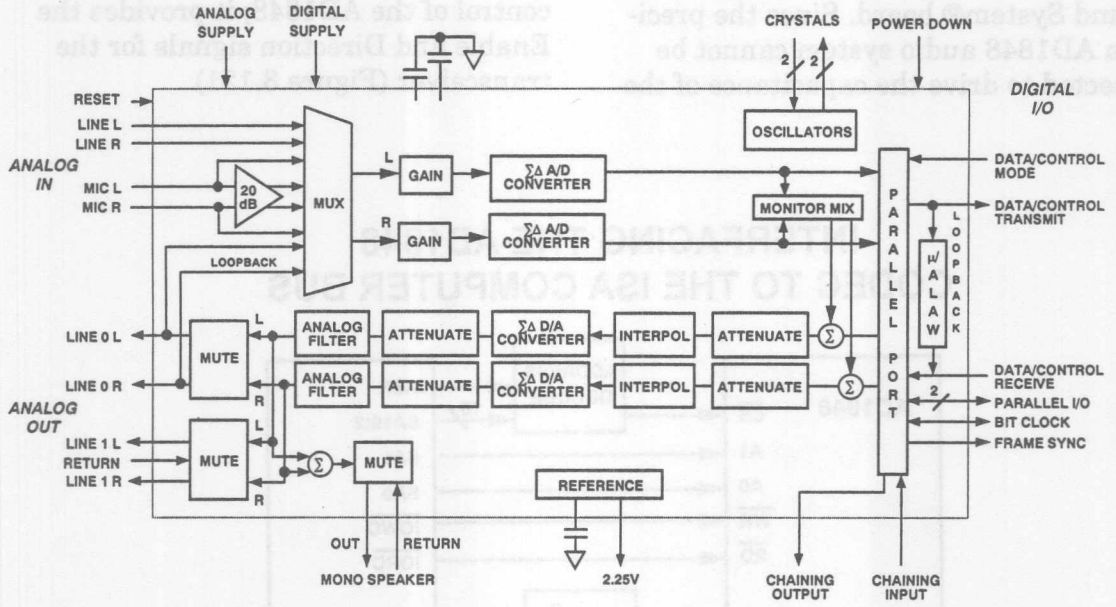


Figure 8.122

AD1849 SERIAL CODEC DSP INTERFACE

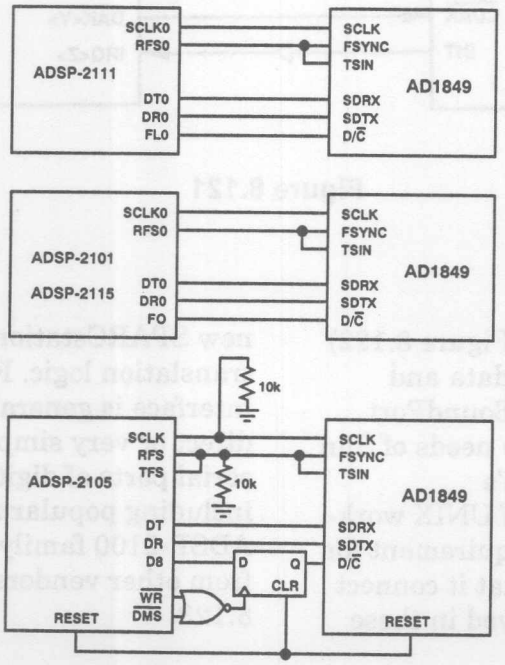


Figure 8.123

The direct connection to DSPs makes it possible to design very cost-effective digital audio "signal-computing" solutions (*Analog Dialogue* 26-2). The DSP can implement a wide range of compression/decompression and audio effects algorithms (such as filtering or equalization) using programs that can be either ROM-resident or downloaded from disk into local RAM.

Additional features of—and differences between—the AD1848 and AD1849 make available solutions for a variety of user needs. For example, the AD1848 parallel-port codec supports both programmed I/O (PIO) and direct memory access (DMA) transfers. In PIO, control information is transferred using the Read and Write strobes. Five registers are directly addressed via the two address pins of the IC. Two of these, used for address and data, indirectly access 16 additional byte-wide control registers, minimizing the number of PLCC package pins (68). Either one or two channels of DMA are supported via the Request and Acknowledge controls. A loadable, 16-bit DMA down-counter generates an external/internal interrupt on underflow.

For multimedia PC (MPC) compatibility, the AD1848 also has two stereo pairs of auxiliary line-level *analog* inputs. Both channels can be independently mixed with the stereo DAC output in the analog domain. As the block diagram shows, this post-mixed analog signal is itself available as an input to the stereo a/d converters. The AD1848 also supports the MPC standard's 8-bit unsigned data format at input and output.

The AD1849 serial-port codec has its own share of unique features. It will accept one of three clock sources: an external crystal, an external clock, or the serial port's bit clock. The serial bus can support up to four devices via time-division multiplexing (TDM). It also has chaining inputs and outputs for sequential word synchronization when one, two, or four devices are "daisy-chained" on a single serial bus. Though more limited than the AD1848 with respect to analog inputs, the AD1849 offers an additional line-level stereo output driven from the stereo d/a converters, and an additional output for a monophonic speaker. The AD1849 is packaged in a 48-lead PLCC.

These two SoundPort codecs provide complete solutions for computer digital-audio applications requiring either parallel or serial interfacing. Though differing in detail, their capabilities are comparable overall.

SIGNAL COMPUTING AUDIO CHIPSETS AND ALGORITHMS

Signal Computing is a technology framework and business model which recognizes that DSP-based signal-processing applications can benefit substantially by combining sets of high-performance processor- and interface chips with powerful, sophisticated algorithms from independent third parties (Independent Algorithm Vendors, or IAVs). Employing open designs and architectures, signal computing is characterized by well-defined levels of standardization that carefully define the hardware and software roles and the layers that make them up. This allows companies—both chip- and software vendors and OEM and system designers—to participate at the level where each brings maximum "value-added" expertise to the application. The chip supplier furnishes standard high-performance, low-cost ICs; the market-oriented algorithm developer provides the standard configurable software that produces the desired electronic performance from the chips; and the OEM designer integrates them into a system specialized to meet the performance needed within his market niche. This environment avoids saddling the designer with the job of recreating all aspects of the overall design.

Low-cost digital signal processing is an "enabling" function, allowing broad expansion of *real-time* signal processing, through the combination of software and hardware defined as "signal computing." Signal computing is characterized by the synchronized execution of algorithms on *real-time* data streams. It is quite distinct from the use of DSP, or any processor, in conventional numerical acceleration, where computations and graphics are simply speeded up—but still occur off-line: images are redrawn "more quickly" on the graphics workstation screen, but even though waiting time is reduced, it is still palpable.

PERSONAL SOUND SYSTEMS USING THE AD20MSP614 AUDIO CHIPSET

The AD20msp614 Audio Chipset is the enabling chipset for Personal Sound System products. the AD20msp614 includes an ADSP-2115KP, AD1848KP, and ESC614. The ESC614 is a gate array designed by Echo Speech Corporation which provides a PC to DSP interface. The personal sound system architecture is illustrated in Figure 8.125.

SIGNAL COMPUTING: A TECHNOLOGY AND BUSINESS MODEL FOR REALTIME SIGNAL PROCESSING SOLUTIONS

- **Hardware Chipsets:**
  Analog I/O (Codecs), DSP Processors, ASIC Interface Chips
- **Software Algorithms: Independent Algorithm Vendors (IAVs)**
- **Manufacturing Design Kits**
- **Typical Applications:**
  Modems, Speech Processing, Music Processing, Digital Mobile Radio, Image Processing, Multimedia

Figure 8.124

PERSONAL SOUND SYSTEM ARCHITECTURE

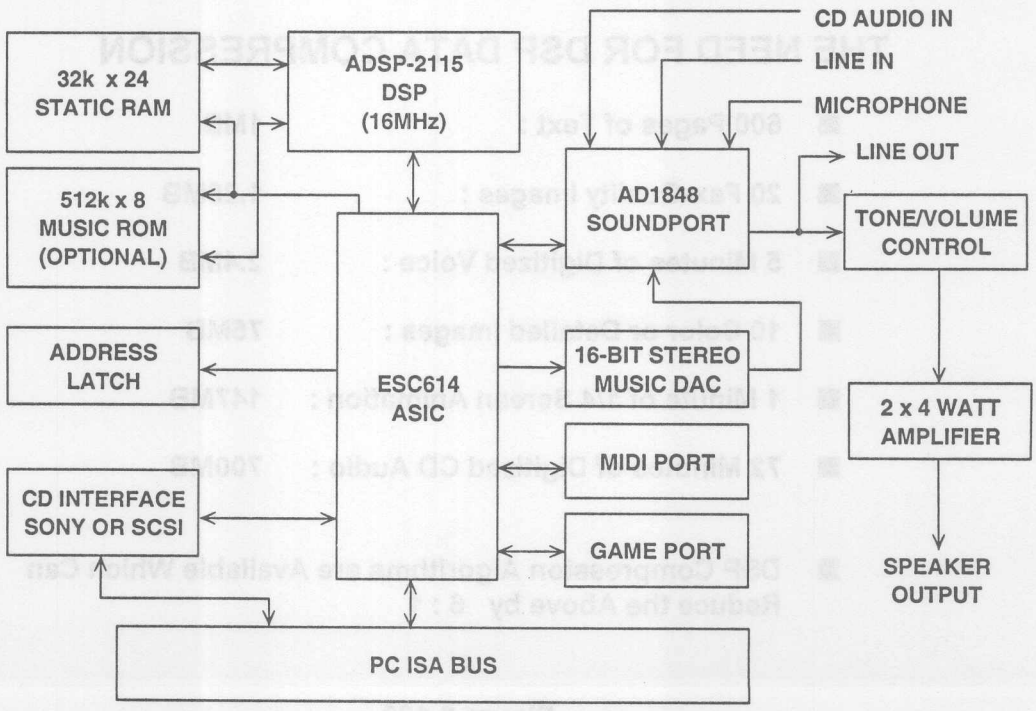


Figure 8.125

The ADMK-610 is a manufacturing kit which allows add-in card OEMs to enter the sound card market with a Personal Sound System product. The kit provides all an OEM needs to manufacture a Personal Sound System which supports Sound Blaster and Windows Sound System applications. The kit includes manufacturing information such as schematics, board layout, and parts lists. DSP algorithm software is included which provides Sound Blaster compatibility. Drivers for WAVE I/O, Musical Instrument Digital Interface (MIDI) MPU-401, and auxiliary functions (mixing, volume, and tone control) are also included in the kit. To complete the solution, Voyetra Multimedia Software, First Byte Monologue text-to-speech, and AudioFile audio application software are also included with the kits. Purchase of separate licenses from the respective software vendors is required for all application software included in the kit. Purchase of the a EuSynth-1 music synthesis license from Analog Devices (ADLU-EUP02/-Q) is required for Sound Blaster compatibility.

Future upgrades to the ADMK-610 will enable Personal Sound System products to be upgraded to future capabilities such as EuSynth-2 wavetable music synthesis and speech and music compression.

The requirement for data compression represents a typical application for signal computing. Figure 8.126 shows the amount of hard disc storage required for various types of data. Notice that 72 minutes of digitized CD-quality audio requires approximately 700MB of storage. This would be impractical in multimedia applications without some type of data compression.

THE NEED FOR DSP DATA COMPRESSION

- 600 Pages of Text : 1MB
- 20 Fax-Quality Images : 1.28MB
- 5 Minutes of Digitized Voice : 2.4MB
- 10 Color or Detailed Images : 75MB
- 1 Minute of 1/4 Screen Animation : 147MB
- 72 Minutes of Digitized CD Audio : 700MB
- DSP Compression Algorithms are Available Which Can Reduce the Above by 6 : 1

Figure 8.126

Various data compression algorithms have been written which can reduce this storage requirement by a factor of 5 to 6. The Dolby AC-2 Toolkit (ADLU-EUP01) is a software toolkit available from Dolby Labs. It includes software developed by EuPhonics which implements the Dolby AC-2 Audio compression/decompression algorithms on the ADSP21XX DSP processor. This algorithm achieves 5.6:1 compression of CD quality audio. It compresses 2 channels of 16-bit audio sampled at 44.1kHz. Both compression and decompression can be done on the ADSP-21XX in real time.

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3. P.F. Ferguson, Jr., A. Ganesan and R. W. Adams, *One Bit Higher Order Sigma-Delta A/D Converters*, **ISCAS PROC. 1990**, Vol. 2, pp. 890-893.

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SECTION 9

INTRODUCTION TO HIGH SPEED SIGNALS AND SYSTEMS

- HIGH SPEED SIGNAL LEVELS, IMPEDANCES, AND NOISE
- DYNAMIC RANGE OF HIGH SPEED SYSTEMS
- DEFINING HIGH SPEED SYSTEM DYNAMIC RANGE

SECTION 9

INTRODUCTION TO HIGH SPEED SIGNALS AND SYSTEMS

Walt Kester

In the first seven sections of this book, we examined systems for processing dc or low-frequency *precision* signals. As we saw, even though the frequency content of the signals is low, the signal processing *components* (amplifiers, multiplexers, ADCs) operate at much higher clock frequencies and have higher bandwidths. This requires close attention to fundamental high speed design techniques as well as the fundamental precision design techniques normally associated with precision measurement systems.

In the previous section (Section 8), we discussed various aspects of *audio* signal processing. Although audio signals generally occupy the bandwidth between 20 and 20kHz, we saw that the bandwidths of the amplifiers, ADCs, and other audio processing components may well extend into the hundreds of MHz. These high bandwidths are necessary to achieve the extremely low levels of distortion required in professional audio applications. For example, high speed amplifiers usually classified as *video* amplifiers, such as the AD811, are often used in audio applications to achieve low levels of distortion.

In this section and those to follow, we will primarily examine the processing of signals which lie above the voice and audio frequency range. These signals are somewhat arbitrarily classified as *high speed* signals, at least for the purposes of differentiation. With a few exceptions, most of the definitions and important characteristics also apply to *voiceband* and *audio frequency* signals, which are referred to in this section as *midband signals*.

TYPICAL HIGH SPEED SYSTEM APPLICATIONS

- Instrumentation: Digital Oscilloscopes and Digital Spectrum Analyzers
- Video: Professional and Consumer
- Medical: Ultrasound and Digital X-Ray
- Radar Receivers
- Communications: Data Transmission, Broadband Receivers
- Direct Digital Synthesis
- Arbitrary Waveform Generation

Figure 9.1

The most important goal in high speed signal processing is to maintain the fidelity of the signal to the required accuracy (ac and dc) throughout the entire signal processing path. A good understanding of each element in the signal chain is therefore required in order to make intelligent design tradeoffs. Different applications (see Figure 9.1) require different levels of accuracy. In this section, we will first examine the key specifications which describe the fidelity of high speed signals. Some of these are applicable to low and mid-frequency applications, while others are commonly used only in high speed systems.

POPULAR MEASURES OF HIGH SPEED SIGNAL FIDELITY

- Bandwidth and Settling Time
- Harmonic Distortion and Total Harmonic Distortion
- Signal-to-Noise Ratio
- Two-Tone Intermodulation Products (IMD)
- Third Order IMD Intercept Point
- Spurious Free Dynamic Range (SFDR)

Figure 9.2

High speed signals may be specified in either the time or the frequency domain, or both. However, all elements in the signal processing path may not be specified in both domains. For instance, ADCs are often specified in terms of effective number of bits (ENOBs) at various input frequencies. However in digital oscilloscope and transient analyzer applications, one is also interested in the accuracy with which pulse edges are digitized. This type of data is usually not explicitly specified on ADC data sheets.

It is therefore important to be able to determine approximate time domain specs when only frequency domain specs are given, and vice versa. This may be done quite easily using the simple relationship between bandwidth and risetime for a first-order system: Bandwidth = 0.35/Risetime. Another useful formula relates the time constant

and the risetime: Risetime = 2.2×Time Constant. It should be emphasized that these relationships should be used with caution when dealing with high speed, high resolution systems, nevertheless, they may be used for first-order approximations.

The pulse response of a single-pole system may be expressed using the well-known exponential relationship: $V_{out}(t) = V_o(1 - e^{-t/\tau})$, where τ is the time constant. The settling time to within ε of the final value may be calculated by solving the expression for t using $t = -\tau \ln(\varepsilon)$. Applying this to systems having 10 or more bits of resolution, however, will probably give erroneous results due to second-order effects.

USEFUL RELATIONSHIPS BETWEEN PULSE AND FREQUENCY RESPONSE FOR FIRST-ORDER SYSTEM

- Bandwidth = 0.35 / Risetime
- Risetime = 2.2 × Time Constant
- Settling Time to Within ε of Final Value
  = – Time Constant × ln(ε)
- Use These Approximations With Caution at High Speeds and / or High Resolutions Due to Second-Order Effects

Figure 9.3

HIGH SPEED SIGNAL LEVELS, IMPEDANCES, AND NOISE

High speed signal levels and impedances are typically lower than those encountered in mid- and low frequency applications. The low impedances (usually less than 1000Ω) are required in order to maintain sufficient bandwidth in the presence of stray capacitance. Transmission line effects require the use of terminated cables and microstrip printed circuit board techniques in order to minimize reflections. The lower impedances (typical cable impedances of 50, 75, and 93Ω) require proportionally larger drive currents in

order to maintain reasonable signal amplitudes. While 10V signals at impedance levels of 600Ω or greater are common at low- and audio frequencies, high speed signal amplitudes tend to be limited to a few volts peak-to-peak. Filtering is critical in all signal processing systems. At high speeds, analog filters (usually passive) are generally designed to operate at standard impedance levels of 50, 75, or 93Ω.

There is an inherent tradeoff between signal amplitude and signal-to-noise ratio. The lower signal amplitudes associated with high speed signals, coupled with the wide bandwidths, increase the susceptibility of circuits to noise. Even though lower impedance levels imply lower resistor Johnson noise (a 100Ω resistor generates 1.29nV/√Hz voltage noise), this is somewhat offset by the wider bandwidths associated with high speed systems (thermal noise voltage is proportional to the square root of the bandwidth).

Another challenge associated with high speed systems is maintaining low levels of signal distortion at high frequencies. Many applications such as digital spectral analysis require that high speed signals be processed with minimal distortion. It is not uncommon for systems to require distortion levels compatible with 14 bits of resolution (84dB) at frequencies of 5 to 10MHz. This places severe constraints on any component in the signal processing chain.

A FEW OF THE MANY HIGH SPEED SYSTEM DESIGN CHALLENGES

- Impedance Levels are Low, Therefore Thermal Noise is Reduced

  BUT

- Signal Levels are Lower
- Bandwidths are High, and

  Thermal Noise = $\sqrt{4kTR \times Bandwidth}$

- Many Applications Require Low Levels of Distortion (>80dBc)

Figure 9.4

To illustrate the importance of low impedances for reduced thermal noise, consider the case of the AD9014 ADC which has 14 bits of resolution and a maximum sampling rate of 10MSPS. The input bandwidth is 60MHz, and the input signal range is 2V p-p, or 0.707V rms. The weight of the least significant bit (LSB) is 2V/16,384 = 125μV. This ADC has an input termination resistance of 75Ω. The thermal noise of a 75Ω resistor in the 60MHz bandwidth is approximately 9μV rms. The corresponding fullscale rms signal to rms noise ratio is 98dB (due to the resistor noise alone). If the input resistance were increased to 1000Ω, however, the rms noise over the same bandwidth would be 33μVrms, and the SNR (due to the resistor noise) would drop to 87dB. (Compare this to the theoretical 14 bit SNR of 86dB). For this reason, among others, optimum SNR performance with high speed devices is generally achieved at low impedance levels.

WHY IMPEDANCE LEVELS IN HIGH SPEED SYSTEMS ARE USUALLY LESS THAN 1000Ω

- Consider the AD9014 14bit, 10MSPS ADC:
  - Input Impedance = 75Ω
  - Input Signal = 2V peak-to-peak
  - Least Significant Bit = 125μV
  - Input Bandwidth = 60MHz
- A 75Ω Input Resistor Generates 9μV rms noise over 60MHz, Yielding SNR = 98dB
- A 1000Ω Input Resistor Generates 33μV rms over 60MHz, Yielding SNR = 87dB
- A Perfect 14 bit ADC has an SNR of 86dB

Figure 9.5

DYNAMIC RANGE OF HIGH SPEED SYSTEMS

Dynamic range requirements in high speed systems have increased dramatically over the last several years. Digital Signal Processing techniques are replacing traditional analog techniques. The need for large signal-to-noise ratios and low distortion have made the selection of appropriate amplifiers and ADCs a challenge.

HIGH SPEED SIGNAL PROCESSING DYNAMIC RANGE REQUIREMENTS (APPROXIMATE)

APPLICATION	SIGNAL BANDWIDTH	HARMONIC DISTORTION, SFDR	SIGNAL-TO-NOISE RATIO
Professional Video (HDTV)	6 to 30MHz	–50 to –60dBc	50 to 60dB
Medical Ultrasound Imaging	2 to 15MHz	–50 to –70dBc	45 to 60dB
Digital Ocsilloscopes	dc to 1GHz	–35 to –50dBc	35 to 50dB
Spectrum Analyzers	1 to 10MHz	–70 to –90dBc	60 to 70dB
Broadband Receivers	2 to 30MHz	–40 to –90dB	45 to 70dB

Figure 9.6

Several high speed applications are listed in Figure 9.6 along with approximate bandwidth, distortion, and noise requirements. Note that some applications such as spectral analysis can deal with noise using techniques such as averaging, or narrowing the scanning bandwidth. In these applications, harmonic distortion and spurious free dynamic range are the most important considerations. In other applications, however, both harmonic distortion and noise are important.

DEFINING HIGH SPEED SYSTEM DYNAMIC RANGE

The dynamic range of a high speed system may be defined in several ways. We have already discussed the mid-frequency specifications Harmonic Distortion, Total Harmonic Distortion (THD), and Total Harmonic Distortion Plus Noise (THD + N). These definitions are summarized in Figure 9.7.

COMPARISON BETWEEN DYNAMIC RANGE TERMS FOR MID-FREQUENCY AND HIGH-FREQUENCY SYSTEMS

MID-FREQUENCY	HIGH-FREQUENCY
Harmonic Distortion	Harmonic Distortion
Total Harmonic Distortion THD	Total Harmonic Distortion THD
Total Harmonic Distortion Plus Noise THD + N	Signal-to-Noise Ratio Plus Distortion S/N + D, SNR
Signal-to-Noise Ratio SNR	Signal-to-Noise Ratio Without Harmonics, SNR
Spurious Free Dynamic Range SFDR	Spurious Free Dynamic Range SFDR
----	Intermodulation Distortion IMD
----	Third Order IMD Intercept

Figure 9.7

At high speeds, dynamic range may be defined using slightly different terminology. The spectral output of a signal (including noise components) is used to calculate these terms. The terms Harmonic Distortion and Total Harmonic Distortion have the same meaning at the higher speeds. The term *Signal-to-Noise Plus Distortion (S/N+D)* is often used instead of THD + N. The term *Signal-to-Noise (SNR)* is often used interchangeably with S/N + D. When the SNR measurement is made with the harmonics removed, it is usually referred to as *SNR Without Harmonics*, although in some cases *SNR* may be used. In all cases, careful study of the datasheet definitions will enable you to differentiate between these terms.

The distortion component which makes up Total Harmonic Distortion (THD) is usually calculated by taking the root sum of the squares of the first five or six harmonics of the fundamental. In many practical situations, however, there is negligible error if only the second and third harmonics are included.

DEFINITIONS OF THD AND THD + N

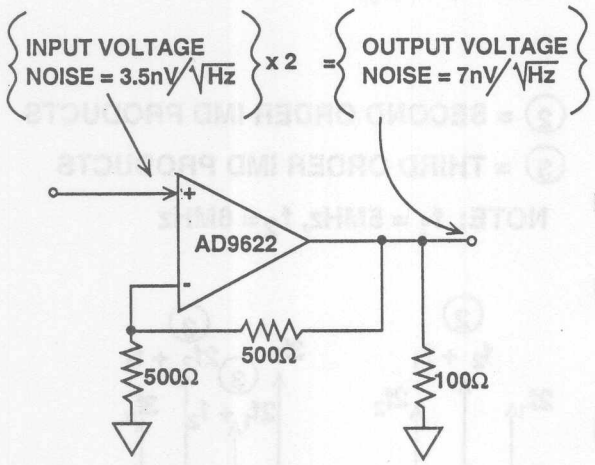
- V_S = Signal Amplitude (rms Volts)
- V_2 = Second Harmonic Amplitude (rms Volts)
- V_n = nth Harmonic Amplitude (rms Volts)
- V_{noise} = rms value of noise over measurement bandwidth
- $$THD + N = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_n^2 + V_{noise}^2}}{V_S}$$
- $$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_n^2}}{V_S}$$

Figure 9.8

It is important to note that the THD measurement does not include noise terms, while THD + N does. The noise in the THD + N measurement must be integrated over the measurement bandwidth. In narrow-band applications, the level of the noise may be reduced by filtering. On the other hand, harmonics and intermodulation products which fall within the measurement bandwidth cannot be filtered, and therefore may limit the system dynamic range.

Consider the example of the simple wideband op amp circuit shown in Figure 9.9. The AD9622 is a high speed low distortion voltage feedback op amp optimized for use in a gain-of-two configuration. The input voltage noise of 3.5nV/√Hz is reflected to the output by multiplying by the noise gain, 2. The 7nV/√Hz is then integrated over the closed loop small signal bandwidth of the op amp, which is approximately 230MHz. This yields a total integrated output noise of 133μV rms. The output noise due to the op amp input current noise and the thermal noise of the resistors is negligible in this example. The corresponding signal-to-noise ratio (neglecting distortion) for a 2V peak-to-peak sinewave output is 74.5dB. Under these conditions, however, the harmonic distortion of the AD9622 is approximately –75dBc at 2MHz. With no filtering, the dynamic range is thus equally limited by the noise and the distortion. If, however, the output of the op amp is filtered, the dynamic range is limited by the distortion.

OUTPUT NOISE AND DISTORTION OF AD9622 WIDEBAND VOLTAGE FEEDBACK OP AMP



- CLOSED LOOP BANDWIDTH = 230 MHz
- RMS OUTPUT NOISE
  $= 7 \times 10^{-9} \sqrt{1.57 \times 230 \times 10^{6}}$
  = 133μV rms
- FOR 2V p-p OUTPUT, SNR = 74.5dB
- HARMONIC DISTORTION = -75dBc @ 2MHz

9

Figure 9.9

Rather than simply examining the THD produced by a single tone sinewave input, it is often useful to look at the distortion products produced by two tones. As shown in Figure 9.10, two tones will produce second and third order intermodulation products. The example shows the second and third order products produced by applying two frequencies, f1 and f2 to a nonlinear device. The second order products located at f2 + f1 and f2 – f1 are located far away from the two tones, and may be removed by filtering. The third order products located at 2f1 + f2 and 2f2 + f1 may likewise be filtered. The third order products located at 2f1 – f2 and 2f2 – f1, however, are close to the original tones, and filtering them is difficult.

needs to be a factor of 10 better than D/A

SECOND AND THIRD-ORDER INTERMODULATION PRODUCTS FOR f_1= 5MHz, f_2 = 6MHz

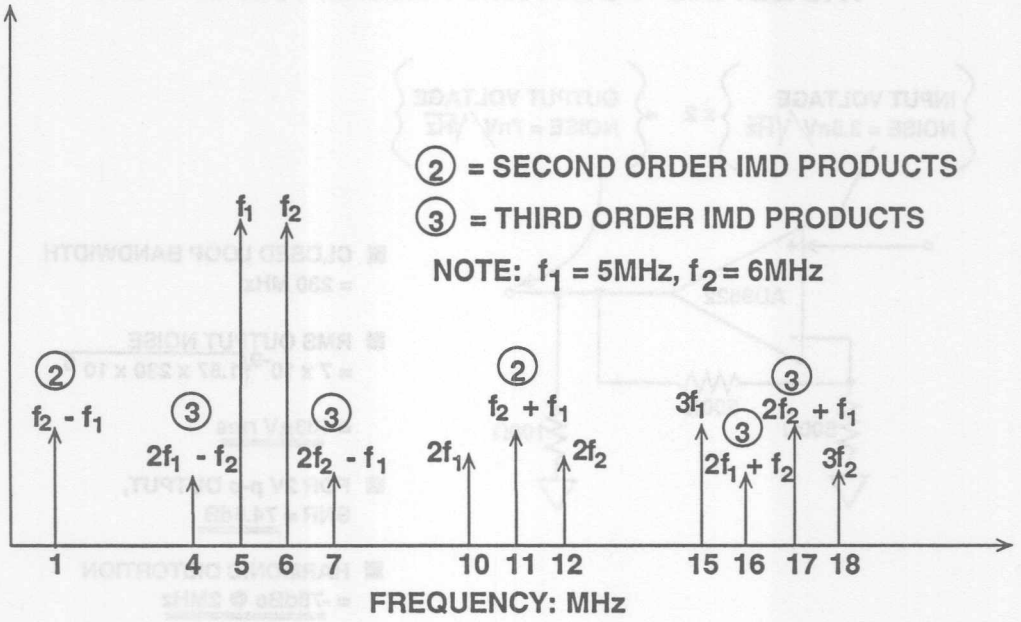


Figure 9.10

Intermodulation distortion products are of special interest in the RF area, and also a major concern in the design of radio receivers. Third-order IMD products can mask out small signals in the presence of larger ones. Third order IMD is often specified in terms of the *third order intercept* point as shown in Figure 9.11. Two spectrally pure tones are applied to the system. The output signal power in a single tone (in dBm) as well as the relative amplitude of the third-order products (referenced to a single tone) is plotted as a function of input signal power. If the system nonlinearity is approximated by a power series expansion, you will find that the second-order IMD amplitudes increase 2dB for every 1dB of signal increase. Similarly, the third-order IMD amplitudes increase 3dB for every 1dB of signal increase. If you start with a low level two-tone input signal, and take a few data points, you can draw the second and third order IMD lines shown in Figure 9.11.

Once the input reaches a certain level, however, the output signal begins to soft-limit, or compress. If you extend the second and third-order intercept lines, they will intersect the extension of the output signal line. These intersections are called the *second-* and *third order intercept points*, respectively. The values are usually referenced to the output power of the device expressed in dBm. Another parameter which may be of interest is the *1dB compression point*. This is the point at which the output signal is compressed by 1dB from the ideal input/output transfer function. This point is also shown in Figure 9.11.

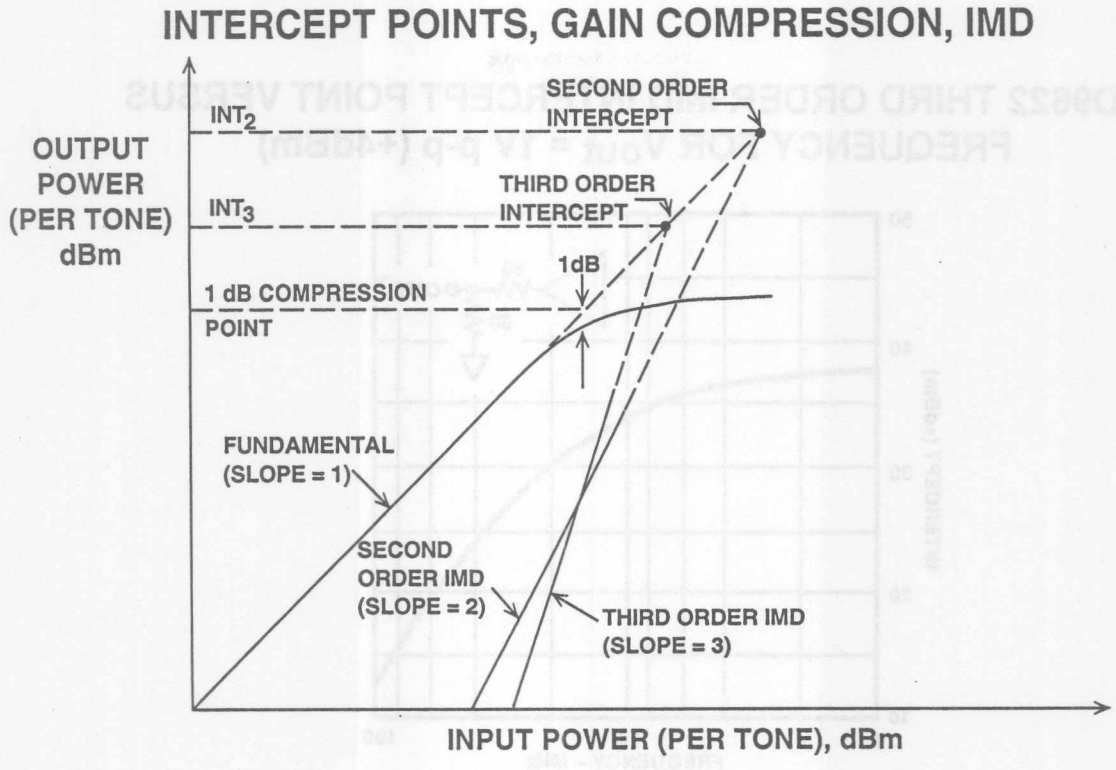


Figure 9.11

Knowing the third order intercept point allows you to calculate the approximate level of the third-order IMD products as a function of output signal level. Figure 9.12 shows the third order intercept value as a function of frequency for the AD9622 voltage feedback amplifier.

Assume the op amp output signal is 10MHz and 2V peak-to-peak into a 100Ω load (50Ω source and load termination). The voltage into the 50Ω load is therefore 1V peak-to-peak, corresponding to +4dBm. The value of the third order intercept at 10MHz is 36dBm. The difference between +36dBm and +4dBm is 32dB. This value is then multiplied by 2 to yield 64dB (the value of the third-order intermodulation products referenced to the power in a single tone). Therefore, the intermodulation products should be –64dBc (dB below carrier frequency), or at a level of –60dBm. Figure 9.13 shows the graphical analysis for this example.

AD9622 THIRD ORDER IMD INTERCEPT POINT VERSUS FREQUENCY FOR V_{out} = 1V p-p (+4dBm)

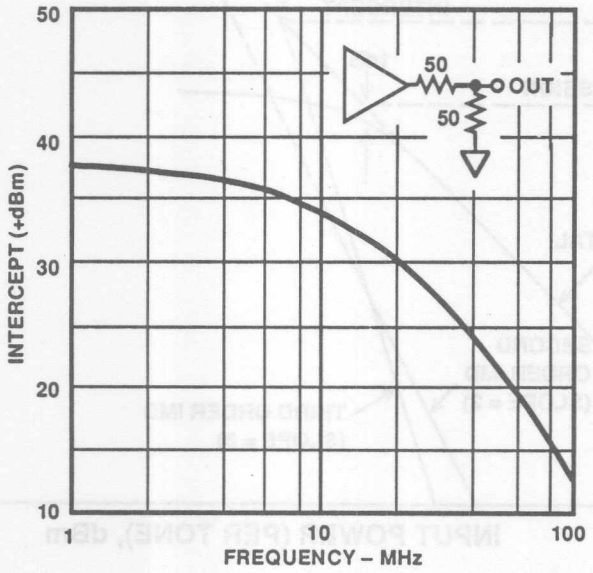


Figure 9.12

USING THE THIRD ORDER INTERCEPT POINT TO CALCULATE IMD PRODUCT FOR THE AD9622 OP AMP

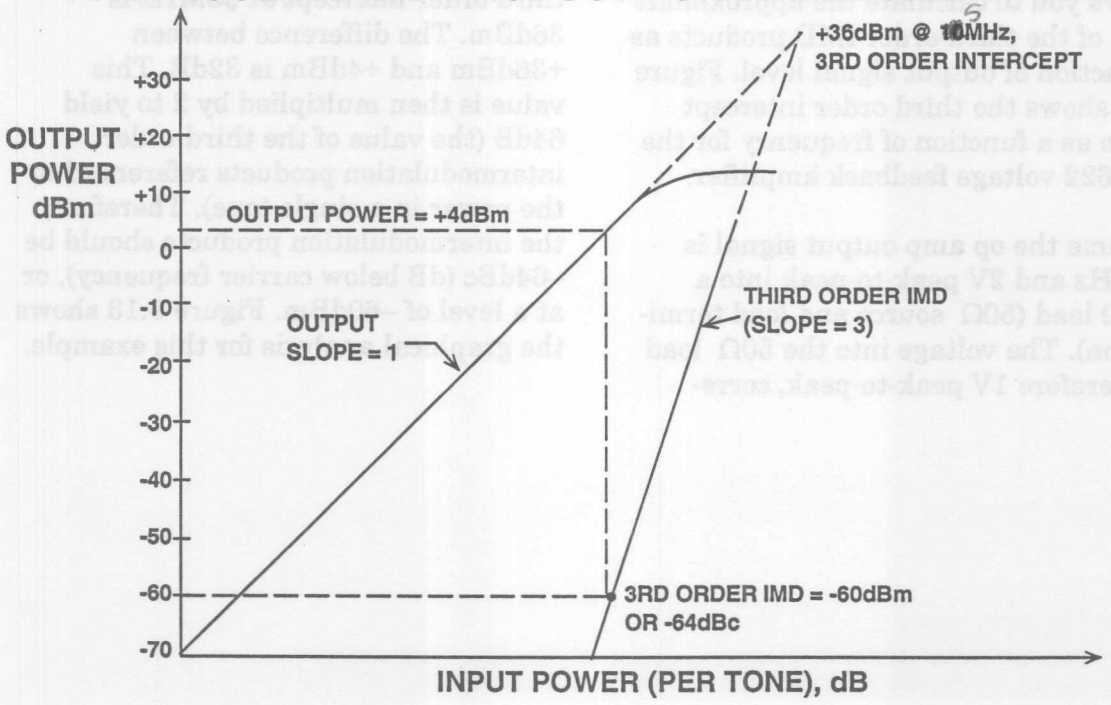


Figure 9.13

Another term often used to characterize the dynamic range of a high speed system is *spurious free dynamic range* (SFDR). The SFDR is defined simply as the difference, in dB, between the rms amplitude of a single-tone signal and the peak spurious signal within the bandwidth of interest. In an amplifier, the level of spurious signals is related to the amplitude of the original signal and is described in terms of harmonic distortion, THD, IMD, or intercept points.

DACs and ADCs, however, generally behave quite differently than amplifiers. In a sampled data system, it is therefore often difficult to examine the output spectrum and distinguish between spurs generated by the *soft* nonlinearity (low-order products) of amplifiers and the *hard* nonlinearity (low and high-order products) caused by quantization and quantization nonlinearity.

AD872 12-BIT, 10MSPS ADC EXHIBITS 73dB SPURIOUS FREE DYNAMIC RANGE FOR 1MHz, –0.5dBFS INPUT

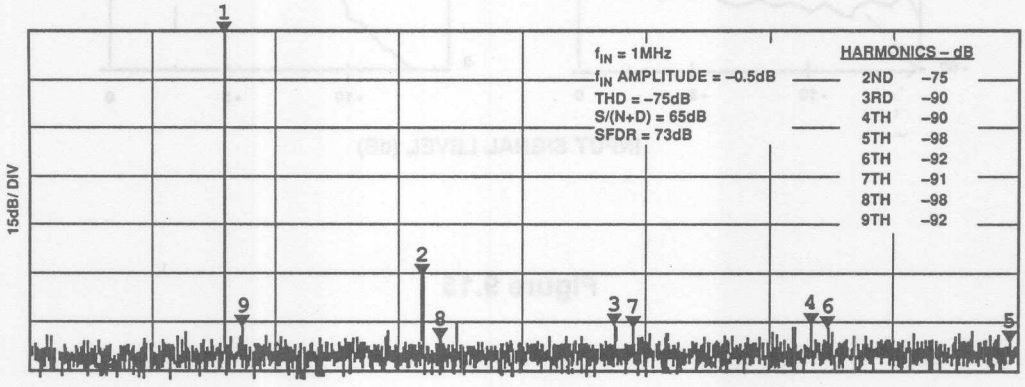


Figure 9.14

Because of this unpredictable nature of the spurs in a sampled data system, the second- and third-order intercepts generally cannot be used to accurately predict IMD performance at various signal levels. If the spurs due to quantization errors were entirely independent of signal amplitude, the point of maximum SFDR would occur for a fullscale input signal. Figure 9.15 shows a typical plot of the maximum spur level versus input signal. Notice that as the signal approaches fullscale, the level of the spurs begins to rise with the signal. This characteristic is typical of many high speed ADCs, especially for high

frequency inputs. The point of maximum SFDR occurs at an input signal amplitude which is a few dB less than fullscale. In some systems, the gain is set such that the nominal signal amplitude into the ADC is equal to this value, thereby ensuring that the ADC provides maximum dynamic range possible.

FOR A TYPICAL ADC, THE MAXIMUM SPURIOUS FREE DYNAMIC RANGE MAY OCCUR WHEN THE INPUT SIGNAL IS SOMEWHAT LESS THAN FULLSCALE

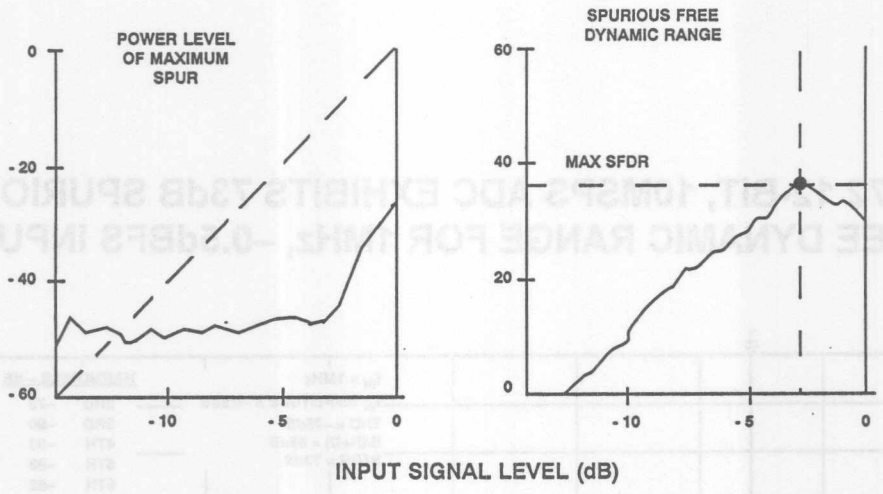


Figure 9.15

In summary, dynamic range in high speed systems is a function of all elements in the signal path and may be limited by distortion, noise, or both. Traditional methods of describing distortion and noise in amplifiers are not always applicable in sampled data systems containing ADCs and DACs. Achieving maximum dynamic range therefore requires a thorough understanding of how each system element contributes to the overall system performance. In the following sections, we will examine each in detail.

REFERENCES

1. Robert A Witte, *Distortion Measurements Using a Spectrum Analyzer*, **RF Design**, September, 1992, pp. 75-84.

2. Walt Kester, *Confused About Amplifier Distortion Specs?*, **Analog Dialogue**, 27-1, 1993, pp. 27-29.

3. **High Speed Design Seminar**, 1990, Norwood, MA: Analog Devices, Inc., Section 5, pp. 13-19.

SECTION 10

HIGH SPEED SIGNAL AMPLIFICATION

- HIGH SPEED AMPLIFIER ARCHITECTURES
- CURRENT FEEDBACK AMPLIFIERS
- COMPARISON BETWEEN VOLTAGE FEEDBACK AND CURRENT FEEDBACK OP AMPS
- HIGH SPEED BUFFER AMPLIFIERS
- HIGH SPEED OP AMP NOISE MODELS
- OP AMP DC MODEL
- LEVEL SHIFTING HIGH SPEED SIGNALS USING OP AMPS

SECTION 10

HIGH SPEED SIGNAL AMPLIFICATION

Walt Kester

The amplification of high speed signals while preserving fidelity presents a significant design challenge. Although there is an overwhelming number of op amps from which to select, only a few satisfy the stringent requirements of high speed signal processing systems. Figure 10.1 lists the selection criteria in the approximate order of decreasing importance. Dynamic range (measured in terms of distortion and noise) and bandwidth are major driving forces in high speed signal processing systems. These parameters are especially important in applications (such as spectral analysis) where the preservation of spectral purity is paramount. Settling time is important in pulse analysis, while video applications require high bandwidths (flat over a wide range of frequencies) and low levels of differential gain and phase.

In the majority of high speed systems, ac performance usually takes priority over dc precision. Nevertheless, modern high speed amplifiers achieve levels of dc accuracy which are usually more than adequate for most applications.

HIGH SPEED AMPLIFIER SELECTION CRITERIA

- Distortion Under Load
- Bandwidth and Bandwidth Flatness
- Broadband Noise
- DC and Capacitive Output Drive Capability
- Settling Time
- Video-Specifications: Differential Gain and Phase
- DC Offset, Drift, and Input Bias Current

Figure 10.1

HIGH SPEED AMPLIFIER ARCHITECTURES

Although it is possible to select high speed amplifiers without much understanding of their internal architectures or circuits, the following discussion will allow the designer to make much more intelligent tradeoffs and perhaps complete the system design in a more timely manner with better performance. In recent years, the differences in amplifier architectures are becoming somewhat overshadowed by the similarities in final performance. For example, *current feedback* op amps (sometimes called *transimpedance* amplifiers) are not necessarily the best choice in all high speed applications. There are a number of applications where optimized fixed-gain *voltage feedback* buffers provide the best solution.

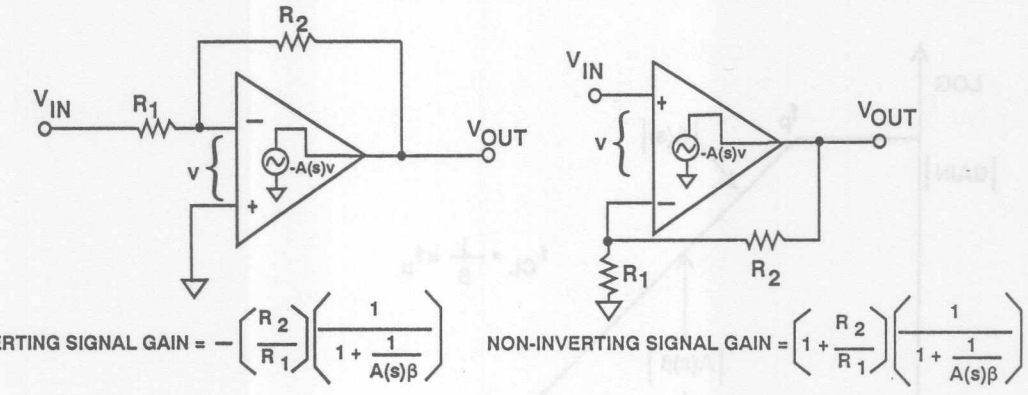
POPULAR HIGH SPEED AMPLIFIER ARCHITECTURES

- Voltage Feedback
- Current Feedback
- Optimized Fixed-Gain Closed-Loop Buffers

Figure 10.2

The equivalent circuit for a typical voltage feedback op amp is shown in Figure 10.3. The input voltage is multiplied by the open loop gain A(s) to yield the output voltage. The feedback attenuation factor is β. The equations which relate the input and output voltage for the inverting and non-inverting mode are also given in Figure 10.3.

VOLTAGE FEEDBACK OP AMP EQUIVALENT CIRCUITS



$$\text{INVERTING SIGNAL GAIN} = -\left(\frac{R_2}{R_1}\right)\left(\frac{1}{1+\frac{1}{A(s)\beta}}\right)$$

$$\text{NON-INVERTING SIGNAL GAIN} = \left(1+\frac{R_2}{R_1}\right)\left(\frac{1}{1+\frac{1}{A(s)\beta}}\right)$$

A(s) = OPEN LOOP VOLTAGE GAIN

$$\beta = \text{FEEDBACK FACTOR} = \frac{R_1}{R_1+R_2}$$

$$\frac{1}{\beta} = \text{NOISE GAIN} = 1+\frac{R_2}{R_1}$$

LOOP GAIN = A(s)β

Figure 10.3

10

The term A(s)β is referred to as the *loop gain*. It is the value of the loop gain at a specified frequency which will determine the overall accuracy of the op amp at that frequency. The so-called *curative* effects of feedback at any frequency are determined by the available amount of loop gain at that frequency. Loop gain affects gain accuracy and stability, linearity, distortion, input impedance, and output impedance. The corresponding Bode plot for a single pole rolloff with fixed compensation is shown in Figure 10.4.

LOG-LOG BODE PLOT FOR VOLTAGE FEEDBACK OP AMP

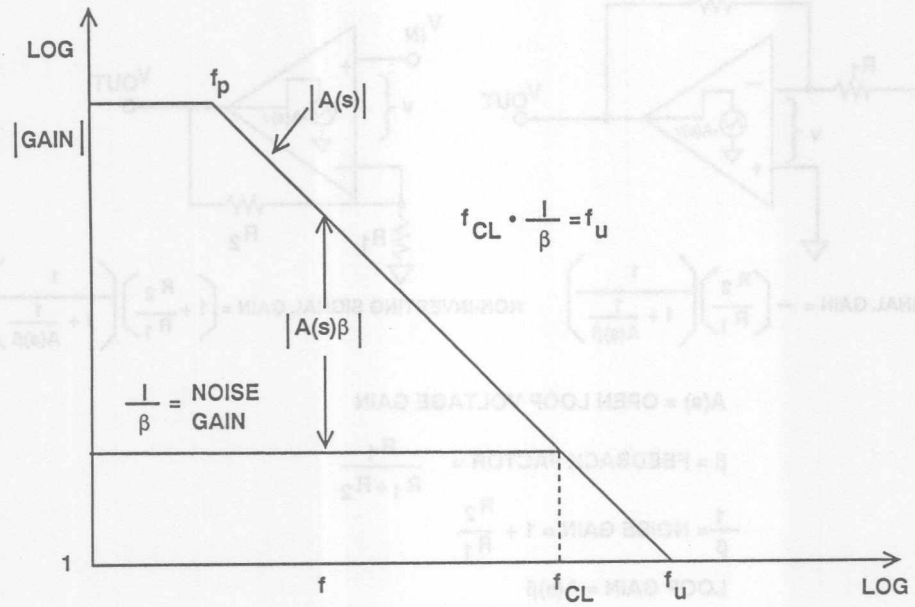


Figure 10.4

The *gain-bandwidth product* of an op amp is simply the product of the closed loop gain and the corresponding bandwidth at a specified frequency. For a voltage feedback amplifier which has a single-pole frequency response, this product is constant over a wide range of frequencies (see Figure 10.4). If the op amp is stable at unity gain, the frequency at which the open loop response crosses unity gain is called the *unity gain bandwidth frequency*. The gain-bandwidth specification may thus be used to calculate the closed-loop bandwidth for various values of closed-loop gain.

A key point often confused in selecting voltage feedback op amps based on bandwidth is that the closed loop gain, A_{cl}, refers to the *noise gain*, $1/\beta$, and not the *signal gain* (see Figure 10.5). For instance, in the non-inverting mode, the dc *signal gain* $(1+R_2/R_1)$ is equal to the dc noise gain. In the inverting mode, however, the noise gain remains $1+R_2/R_1$, but the signal gain is now $-R_2/R_1$. For example, if an op amp has a gain-bandwidth product of 10MHz, the closed loop bandwidth for a non-inverting unity gain configuration is 10MHz, while that of a unity-gain inverter is only 5MHz.

RELATIONSHIP BETWEEN NOISE GAIN, SIGNAL GAIN, AND BANDWIDTH FOR OP AMP WITH UNITY GAIN BW OF 10MHz

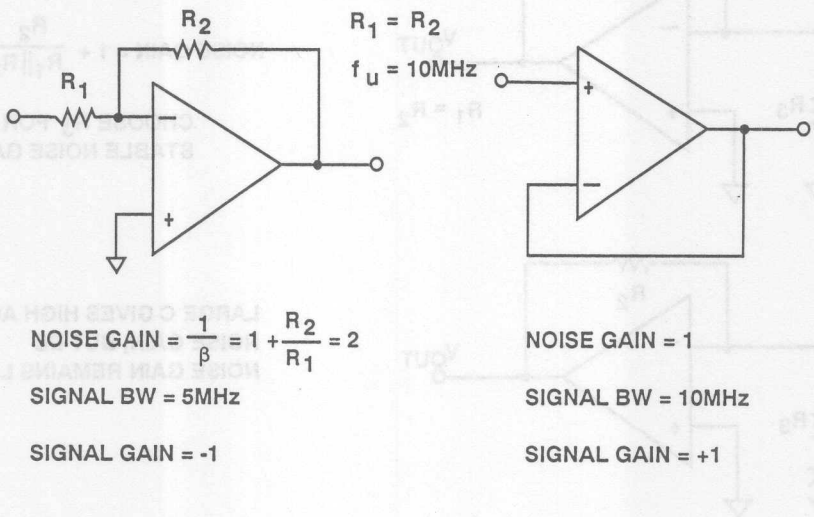


Figure 10.5

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Another important point is that some op amps are optimized to operate at high gains, and are not stable under low- or unity-gain conditions. With these op amps, the gain-bandwidth product is meaningful only over the region of stable closed-loop gains. This type of amplifier can, however, be used at low inverting signal gains by the addition of a shunt resistor to ground as shown in Figure 10.6. The extra resistor is chosen such that the noise gain is greater than the minimum value required for stability. The penalty is increased sensitivity to input offset voltage and input noise voltage as well as lower signal bandwidth. A capacitor may be used in series with the resistor to avoid increasing the dc noise gain.

OPERATING NON-UNITY GAIN STABLE OP AMPS AT UNITY GAIN IN THE INVERTING MODE

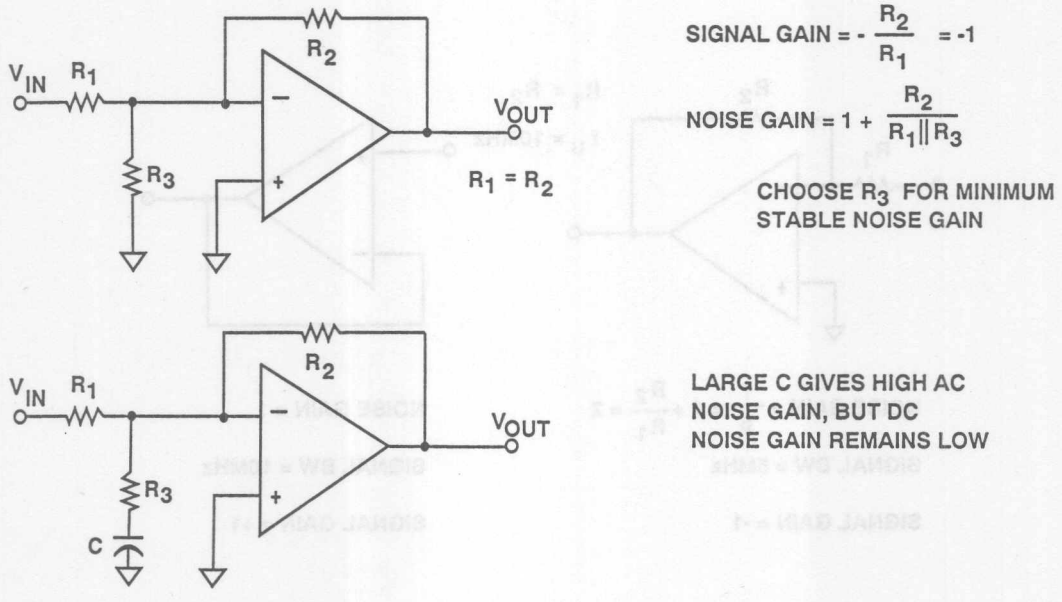
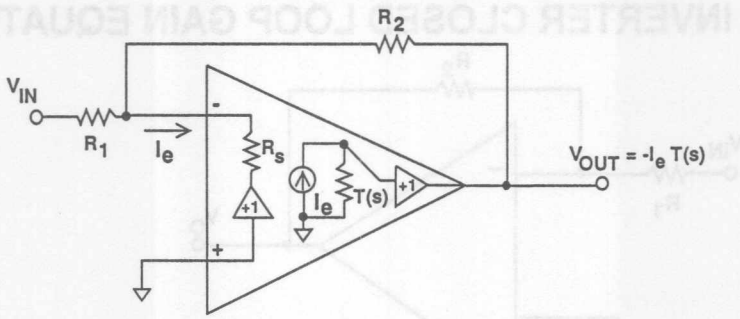


Figure 10.6

CURRENT FEEDBACK AMPLIFIERS

The equivalent circuit for a current feedback amplifier is shown in Figure 10.7. The signal at the non-inverting input is applied to the inverting input through a unity-gain buffer with an output impedance R_S (usually between 10 and 100Ω). The current entering the inverting input is multiplied by the *transimpedance open loop gain*, T(s), to yield the output voltage. The feedback attenuation factor of the current feedback amplifier is different from the voltage feedback amplifier because of the low inverting input impedance, R_S. Solving the feedback equation yields the transfer function shown in Figure 10.7. But although the expression for the current feedback amplifier loop gain is different from a voltage feedback amplifier, it can be used in exactly the same manner in determining the accuracy of the amplifier closed loop gain at any specific frequency.

CURRENT FEEDBACK OP AMP EQUIVALENT CIRCUIT



$$\text{INVERTING SIGNAL GAIN} = -\left(\frac{R_2}{R_1}\right)\left(\frac{1}{1+\frac{1}{LG}}\right) \qquad \text{NON-INVERTING SIGNAL GAIN} = \left(1+\frac{R_2}{R_1}\right)\left(\frac{1}{1+\frac{1}{LG}}\right)$$

T(s) = OPEN LOOP TRANSIMPEDANCE GAIN

$$\beta_{cf} = \text{FEEDBACK FACTOR} = \frac{R_s \| R_1}{R_s \| R_1 + R_2}$$

$$A_{cf}(s) = \text{OPEN LOOP VOLTAGE GAIN} = \frac{T(s)}{R_s}$$

$$\text{LOOP GAIN} = LG = A_{cf}(s)\,\beta_{cf} = \frac{T(s)\{R_s \| R_1\}}{R_s\{R_s \| R_1 + R_2\}}$$

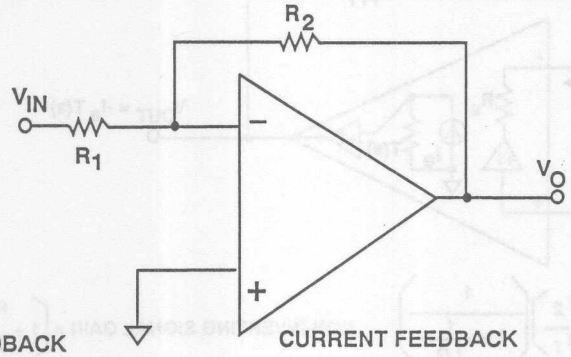
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Figure 10.7

COMPARISON BETWEEN VOLTAGE FEEDBACK AND CURRENT FEEDBACK OP AMPS

The inverting mode transfer functions for the voltage feedback amplifier and the current feedback amplifier are compared in Figure 10.8. Notice that for the voltage feedback amplifier, the frequency-dependent term, 1/A(s), is multiplied by the noise gain, $(1 + R_2/R_1)$. This implies that the closed loop bandwidth is approximately inversely proportional to the noise gain, hence, the product of the noise gain and the closed loop bandwidth is constant.

VOLTAGE FEEDBACK AND CURRENT FEEDBACK INVERTER CLOSED LOOP GAIN EQUATIONS



VOLTAGE FEEDBACK

$$\frac{V_O}{V_{IN}} = \frac{-R_2/R_1}{1 + \frac{1}{A(s)}\left[1 + \frac{R_2}{R_1}\right]}$$

CURRENT FEEDBACK

$$\frac{V_O}{V_{IN}} = \frac{-R_2/R_1}{1 + \frac{R_2}{T(s)}\left[1 + \frac{R_s}{R_1} + \frac{R_s}{R_2}\right]}$$

ASSUME $R_s << R_1$ AND R_2 NOTE: R_2 FIXED

$$\frac{V_O}{V_{IN}} \approx \frac{-R_2/R_1}{1 + \frac{R_2}{T(s)}}$$

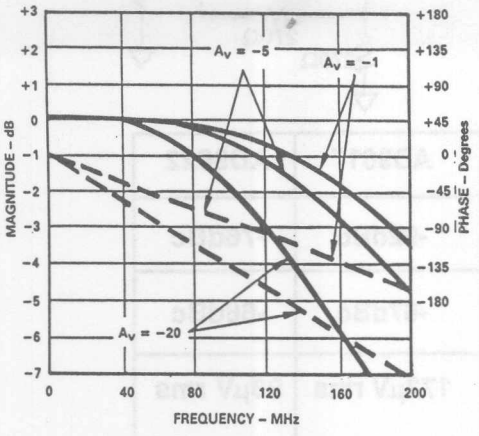
Set BW/R2 GAIN R1

Figure 10.8

In the current feedback amplifier, however, if $R_s << R_1$ and R_2, the closed loop bandwidth is independent of the gain, R_2/R_1, and depends only upon the feedback resistor R_2. Furthermore, most current feedback amplifiers are optimized for maximum bandwidth with a particular value of R_2. This implies that the closed loop bandwidth of a current feedback amplifier will remain fairly constant regardless of closed loop gain, provided the gain is changed by varying only R_1.

Current feedback (or transimpedance) op amps therefore have bandwidths which are relatively independent of closed loop gains (assuming the feedback resistor value remains constant). Therefore, it is inappropriate to refer to the gain-bandwidth product of this type of amplifier. For instance, the signal bandwidth of the AD9617 with a 400Ω feedback resistor is approximately 190MHz for a closed loop signal gain of –1, and approximately 165MHz for a closed loop-signal gain of –5 (see Figure 10.9). In the first case, the so-called gain-bandwidth product would be 190MHz (1 × 190MHz), while in the second case it would be 825MHz (5 × 165MHz). In addition, current feedback amplifiers are usually optimized for a fixed value of feedback resistor. Increasing the feedback resistor lowers the bandwidth proportionally, while decreasing the value may lead to instability. The closed loop signal bandwidth for current feedback amplifiers should therefore be determined from curves on the data sheet.

GAIN AND PHASE RESPONSE FOR AD9617 CURRENT FEEDBACK OP AMP



GAIN	BW	PRODUCT
-1	190MHz	190MHz
-5	165MHz	825MHz

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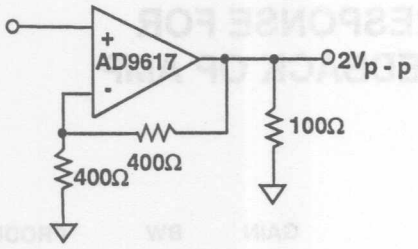
Figure 10.9

The requirement of a fixed, low-value (typically 400Ω to 1000Ω) feedback resistor becomes a significant disadvantage when using a current feedback op amp in the inverting mode at large gains. For example, with the AD9617 optimum feedback resistor of 400Ω, the feedforward resistor must be 40Ω to achieve an inverting gain of 10. Driving the low value feedforward resistor may become a significant problem. Therefore, the non-inverting configuration is generally preferable when using current feedback amplifiers at high gains.

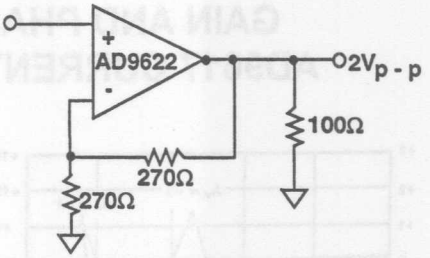
In order to evaluate the performance differences between voltage and current feedback op amps, consider the simple gain-of-2 circuits shown in Figure 10.10.

HIGH SPEED, GAIN-OF-TWO, 200MHz OP AMP BUFFER

CURRENT FEEDBACK



VOLTAGE FEEDBACK



	AD9617	AD9622
DISTORTION AT 1 MHz	-92dBc	-76dBc
DISTORTION AT 20 MHz	-67dBc	-66dBc
RMS OUTPUT NOISE (0.1Hz TO 200MHz)	172μV rms	98μV rms

Figure 10.10

One circuit uses the AD9622 voltage feedback op amp, while the other uses the AD9617 current feedback op amp. Both op amps were designed on the same complementary bipolar (CB) process. Notice that both op amps have a closed loop bandwidth of about 200MHz and 0.1% settling time of about 10ns. The important performance differences relate to noise and distortion. Notice that although the AD9622 op amp distortion is close to that of the AD9617 at 20MHz, it becomes much worse at lower frequencies (see Figure 10.12).

VOLTAGE FEEDBACK VERSUS CURRENT FEEDBACK OP AMP COMPARISON FOR GAIN OF +2 CONFIGURATION

	Current Feedback (AD9617)	Voltage Feedback (AD9622)
Distortion @ 20MHz	– 67dBc	– 66dBc
Distortion @ 1MHz	– 92dBc	– 76dBc
Input Current Noise	29pA / √Hz (– Input)	3.2pA / √Hz (+ and – Input)
Input Voltage Noise	1.2nV / √Hz	3.5nV / √Hz
RMS Output Noise	172μV rms, 0.1 to 200Mhz	98μV rms, 0.1 to 200MHz
Bandwidth (SSBW)	200MHz	220MHz
Slew Rate	1400V/μs	1500V/μs
Settling Time to 0.1%	10ns	8ns
Input Offset Voltage	1mV	2mV

Figure 10.11

DISTORTION OF AD9622 VOLTAGE FEEDBACK OP AMP AND AD9617 CURRENT FEEDBACK OP AMP FOR $R_L = 100\Omega$ AND $V_{OUT} = 2V_{p-p}$, NOISE GAIN = 2, BANDWIDTH = 200MHz

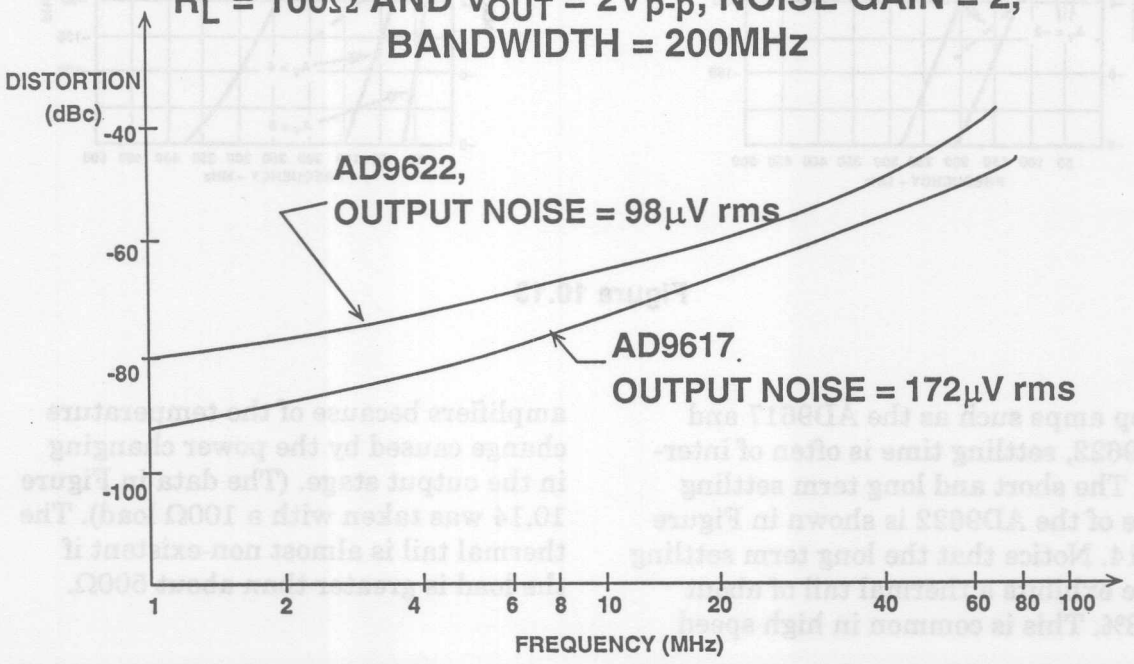


Figure 10.12

The other important difference is that the total output noise of the AD9622 is much less than that of the AD9617. The dominant source of output noise for the AD9622 is the input voltage noise. On the other hand, the AD9617 inverting input current noise (which flows through the feedback resistor) is the dominant contributor to the total output noise. In both circuits, the Johnson noise of the resistors may be neglected.

The inverting and non-inverting frequency response of the AD9622 voltage feedback op amp is shown in Figure 10.13. Note that the bandwidth is approximately inversely proportional to the gain as would be expected for the voltage feedback architecture.

AD9622 VOLTAGE FEEDBACK OP AMP FREQUENCY RESPONSE

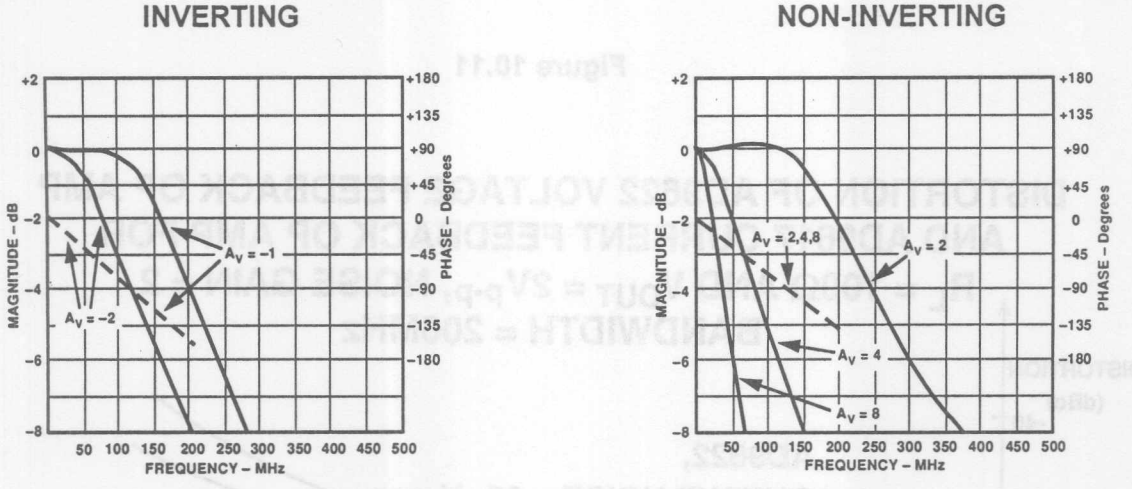


Figure 10.13

In op amps such as the AD9617 and AD9622, settling time is often of interest. The short and long term settling time of the AD9622 is shown in Figure 10.14. Notice that the long term settling time exhibits a thermal tail of about 0.03%. This is common in high speed amplifiers because of the temperature change caused by the power changing in the output stage. (The data in Figure 10.14 was taken with a 100Ω load). The thermal tail is almost non-existent if the load is greater than about 500Ω.

AD9622 OP AMP SHORT AND LONG-TERM SETTLING TIME

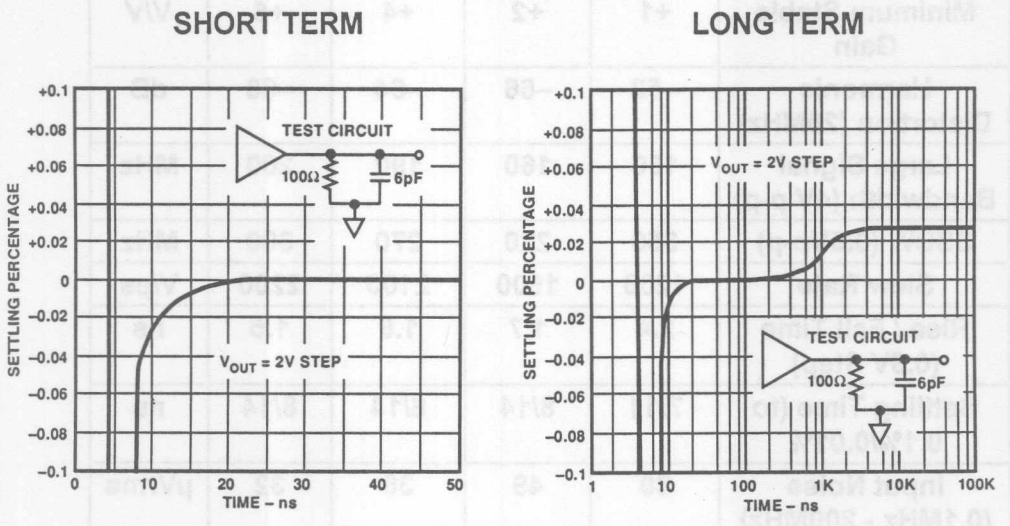


Figure 10.14

From the discussions so far, it should be clear that the differences between voltage and current feedback op amp performance are somewhat more subtle than one would suspect from recent literature. Other than the tradeoffs between noise and distortion discussed above, current feedback amplifiers are uniquely suited to applications where constant bandwidth must be achieved over a fairly wide range of gain settings. (This is true only if the value of the feedback resistor remains constant! If the feedback resistor is increased above the nominal value, the bandwidth is approximately inversely proportional to the resistor increase. Lower than optimum feedback resistors usually cause instability in current feedback op amps).

In order to take advantage of the lower current noise and increased flexibility of voltage feedback amplifiers, the same basic circuit design may be optimized for various gains. This was done in the AD9621, AD9622, AD9623, and AD9624 op amp family. The performance of these amplifiers is summarized in Figure 10.15.

AD9621,AD9622,AD9623,AD9424
VOLTAGE FEEDBACK OP AMPS

Parameter	AD9621	AD9622	AD9623	AD9624	Units
Minimum Stable Gain	+1	+2	+4	+6	V/V
Harmonic Distortion (20MHz)	–52	–66	–64	–66	dB
Large Signal Bandwidth (4V p-p)	130	160	190	200	MHz
SSBW (0.5Vp-p)	350	220	270	300	MHz
Slew Rate	1200	1500	2100	2200	V/µs
Rise / Fall Time (0.5V Step)	2.4	1.7	1.6	1.5	ns
Settling Time (to 0.1%/0.01%	7/11	8/14	8/14	8/14	ns
Input Noise (0.1MHz - 200MHz)	80	49	36	32	µVrms

Figure 10.15

In order to achieve these levels of high speed performance, however, careful attention must be given to good high speed circuit layout, grounding, and decoupling techniques. Figure 10.16 shows the standard inverting and noninverting connections for the AD9622. Notice that since the inputs are symmetrical, the effects of the input bias currents can be minimized by the addition of the proper resistor in series with the noninverting input. The diagrams of Figure 10.16 show a bootstrap capacitor, C_B (normally 0.001µF), which may be added to further enhance settling time. This capacitor connects to the internal high impedance nodes of the amplifier. Using this capacitor will reduce the large signal (4V) step output settling time by 3ns to 5ns for 0.05% or greater accuracy. For settling accuracy less than 0.05% or for smaller step sizes, its effect will be less apparent. Under fast slew conditions, this capacitor forces the internal signal (initial step) amplitude to be controlled by the "on" (slewed) transistor, preventing its complement from completely turning off. This allows for faster settling time of these internal nodes and also the output. In the frequency domain, total (high frequency) distortion will be approximately the same with or without C_B. Typically, the 3rd harmonic will be greater than the 2nd without C_B. This condition will be reversed with C_B in place.

PROPER LAYOUT AND DECOUPLING IS CRITICAL TO HIGH SPEED OP AMP PERFORMANCE

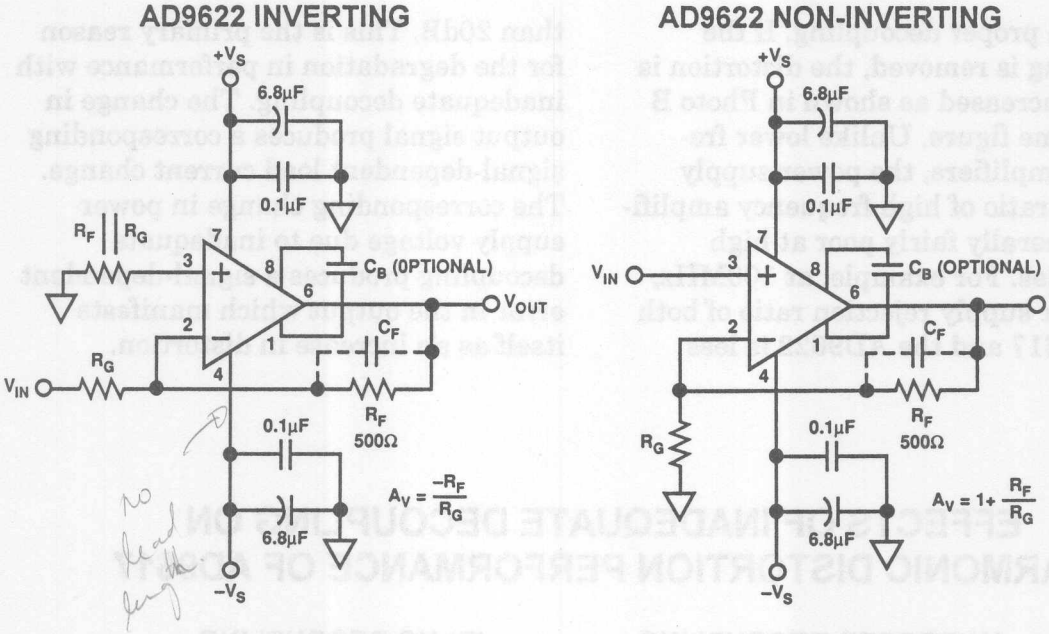


Figure 10.16

As with all wide bandwidth components, good PC board layout is critical to obtain the best dynamic performance with these amplifiers. The ground plane in the area of the op amp and its associated components should cover as much of the component side of the board as possible (or first interior ground layer of a multilayer board).

The ground plane should be removed in the area of the inputs and R_F and R_G to minimize stray capacitance at the input. The same precaution should be used for C_B if it is used. Each power supply trace should be decoupled close to the package with a 0.1µF ceramic (preferably surface mount), plus a 6.8µF tantalum capacitor within 0.5".

All lead lengths for input, output, and feedback resistor should be kept as short as possible. All gain setting resistors should be chosen for low values of parasitic capacitance and inductance, i.e., microwave resistors (buffed metal film rather than laser-trimmed spiral-wound) and/or carbon resistors.

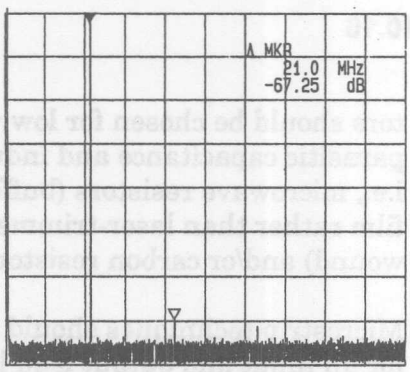
Microstrip techniques should be used for all input and output lead lengths in excess of one inch. Sockets should be avoided if at all possible because of their parasitic capacitance and inductance. If sockets are necessary, individual *pin sockets* such as AMP p/n 6-330808-3 should be used. These contribute far less stray capacitance and inductance than molded socket assemblies.

The effects of inadequate decoupling on harmonic distortion performance are dramatically illustrated in Figure 10.17. Photo A shows the spectral output of the AD9617 driving a 100Ω

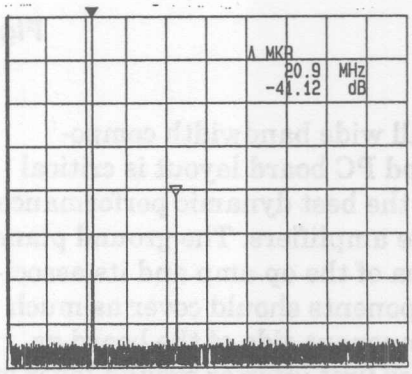
load with proper decoupling. If the decoupling is removed, the distortion is greatly increased as shown in Photo B of the same figure. Unlike lower frequency amplifiers, the power supply rejection ratio of high frequency amplifiers is generally fairly poor at high frequencies. For example, at 100MHz, the power supply rejection ratio of both the AD9617 and the AD9622 is less than 20dB. This is the primary reason for the degradation in performance with inadequate decoupling. The change in output signal produces a corresponding signal-dependent load current change. The corresponding change in power supply voltage due to inadequate decoupling produces a signal-dependent error in the output which manifests itself as an increase in distortion.

EFFECTS OF INADEQUATE DECOUPLING ON HARMONIC DISTORTION PERFORMANCE OF AD9617

(A) PROPER DECOUPLING



(B) NO DECOUPLING



VERTICAL SCALE: 10dB/div.
HORIZONTAL SCALE: 10MHz/div.

Figure 10.17

Inadequate decoupling can also severely affect the pulse response of high speed amplifiers such as the AD9617. Figure 10.19 shows the effects of removing all decoupling capacitors on the AD9717 in its evaluation board. Notice the severe ringing on the pulse response.

AD9617 POWER SUPPLY REJECTION RATIO (PSRR) AND COMMON MODE REJECTION RATIO (CMRR)

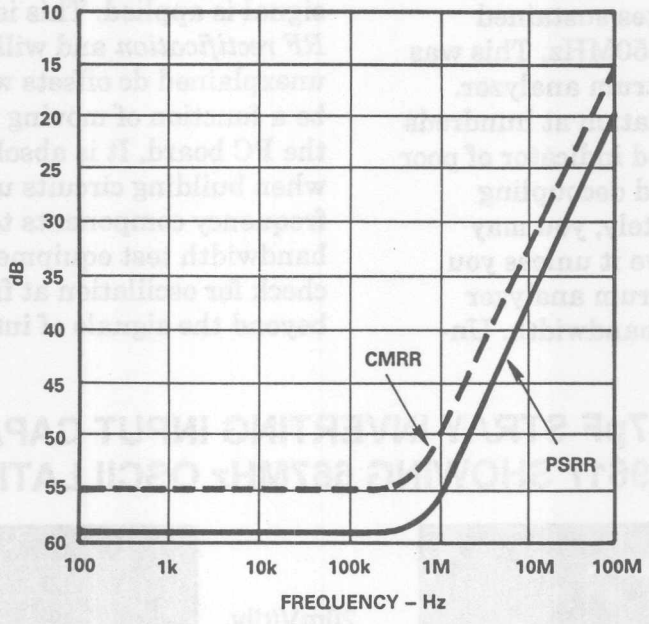
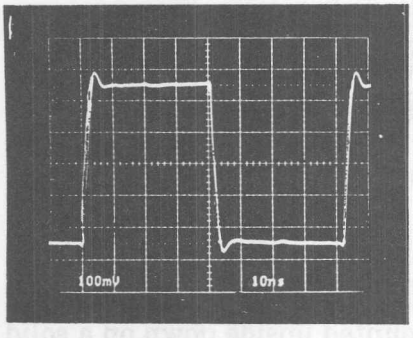


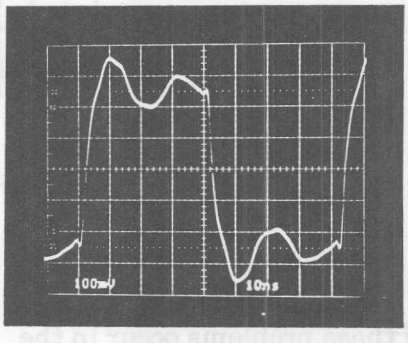
Figure 10.18

EFFECT OF INADEQUATE DECOUPLING ON PULSE RESPONSE OF AD9617 OP AMP

PROPER DECOUPLING



NO DECOUPLING



VERTICAL SCALE: 100mV/div.
HORIZONTAL SCALE: 10ns/div.

Figure 10.19

The effects of stray capacitance on the inverting input of the AD9617 is shown in Figure 10.20. Careful examination of the waveform indicates sustained oscillation at about 650MHz. This was verified using a spectrum analyzer. High frequency oscillation at hundreds of megahertz is a good indicator of poor layout, grounding and decoupling practices. Unfortunately, you may never actually observe it unless you have a scope or spectrum analyzer which has sufficient bandwidth. Unwanted oscillations at RF frequencies will probably be rectified and averaged by devices to which the oscillating signal is applied. This is referred to as *RF rectification* and will create small unexplained dc offsets which may even be a function of moving your hand over the PC board. It is absolutely essential when building circuits using high frequency components to have high bandwidth test equipment and use it to check for oscillation at frequencies well beyond the signals of interest.

EFFECT OF 4.7pF STRAY INVERTING INPUT CAPACITANCE ON AD9617 SHOWING 667MHz OSCILLATION

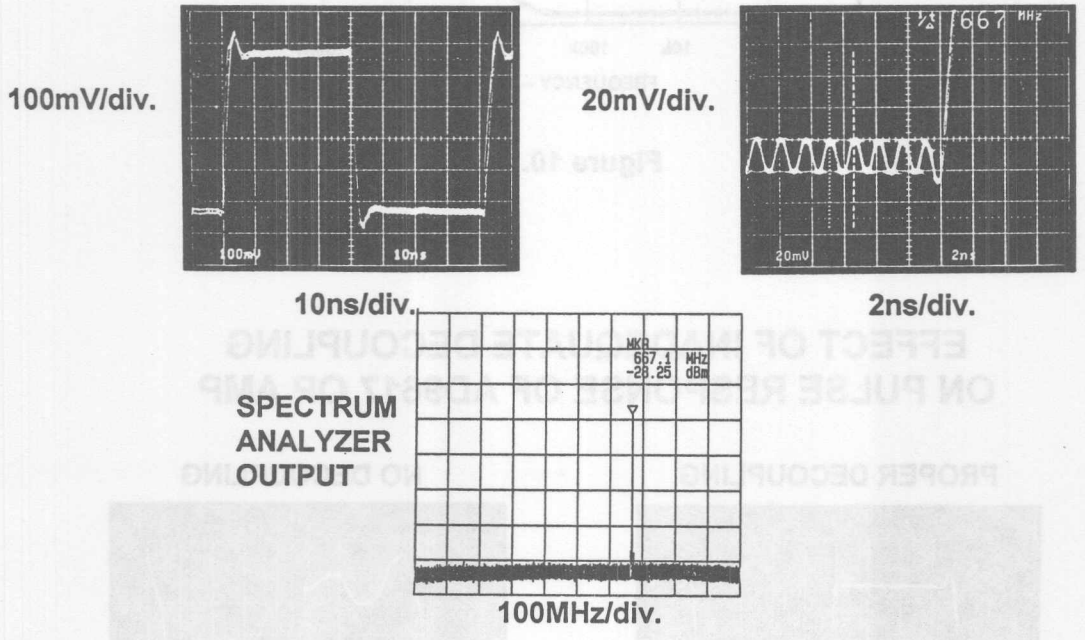


Figure 10.20

Many of these problems occur in the prototype phase due to a disregard for high frequency layout and decoupling techniques. Figure 10.21 shows a hand-wired prototype board which gives excellent performance in spite of its lack of esthetic appeal. The op amp is mounted upside down on a solid copper-clad board with the leads bent back. The signals are connected with short point-to-point wiring. The characteristic impedance of a wire over a ground plane is about 120Ω, although this may vary as much as ±40% depending on the

distance from the plane. The decoupling capacitors are connected directly from the op amp power pins to the copper-clad ground. When working at frequencies of several hundred MHz, it is a good idea to use only one side of the board for ground. Many people drill holes in the board and connect both sides together with short pieces of wire soldered to both sides of the board. If care is not taken, this may result in unexpected ground loops between the two sides of the board, especially at RF frequencies. This approach to prototyping is often called the *deadbug* method because the upside-down ICs look like deceased insects.

PHOTOGRAPH OF A GOOD HIGH SPEED OP AMP PROTOTYPE LAYOUT

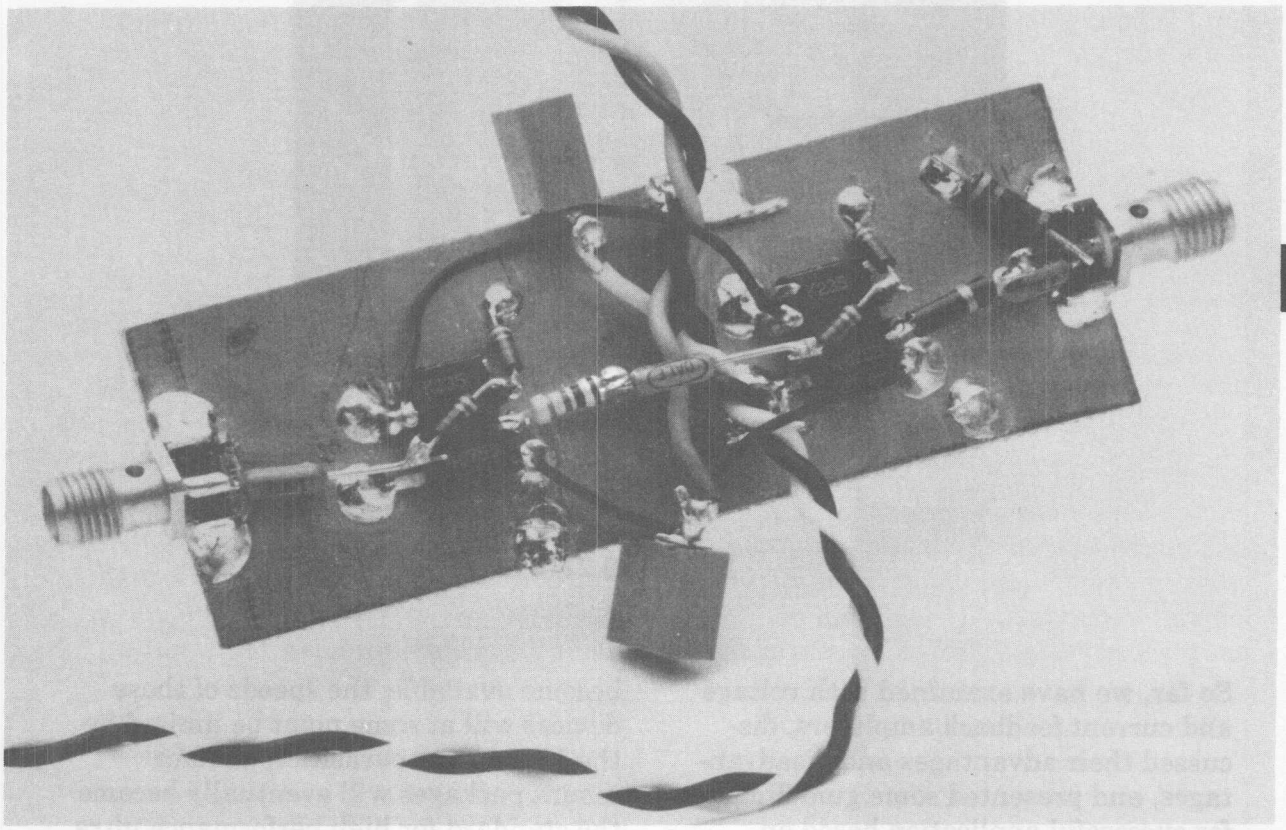


Figure 10.21

In order to properly evaluate the performance of high speed amplifiers, Analog Devices supplies evaluation boards at a nominal charge. The AD9617 evaluation board is shown in Figure 10.22. Use of these boards is encouraged during the initial system design phases.

The actual artwork for the layouts is available free of charge from Analog Devices. In many cases, the artwork appears on the amplifier datasheets, and sometimes PC graphics files are also available

PHOTOGRAPH OF AD9617 OP AMP EVALUATION BOARD

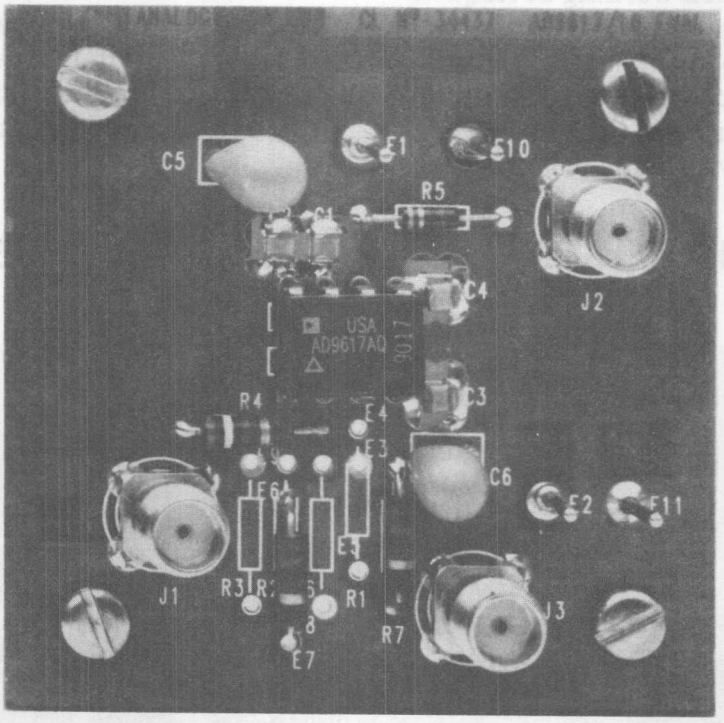


Figure 10.22

So far, we have examined both voltage and current feedback amplifiers, discussed their advantages and disadvantages, and presented some guidelines for successful application based on system requirements. It should be clear that as higher frequency processes become available, the speeds of these devices will at some point be limited by the IC package parasitics. Surface mount packages will eventually become the standard for high performance ultra high speed op amps.

SUMMARY OF HIGH SPEED VOLTAGE FEEDBACK OP AMP CHARACTERISTICS

- Symmetrical Inputs
- Equalization of Source Impedances Generally Reduces Effects of Input Bias Currents
- Largest Noise Source is Input Voltage Noise
- Flexible Feedback Networks Allow Many Tradeoffs
- Constant Gain-Bandwidth Product
- May be Used as Integrators in Active Filters
- Sensitive to Stray Capacitance on Inputs and Outputs
- Proper Layout, Grounding, and Decoupling is Essential to Achieve Specified Performance Levels

Figure 10.23

SUMMARY OF HIGH SPEED CURRENT FEEDBACK OP AMPS CHARACTERISTICS

- Non-Symmetrical Inputs
- Input Bias Current Cancellation Schemes Don't Work
- Inverting Input Current Noise Usually Dominates
- Feedback Network Fixed for Optimum Performance
- Difficult to Use as Integrators in Active Filters
- Bandwidth Remains Relatively Constant for Different Gains
- Sensitive to Stray Capacitance on Inputs and Outputs
- Proper Layout, Grounding, and Decoupling is Essential to Achieve Specified Performance Levels

Figure 10.24

HIGH SPEED BUFFER AMPLIFIERS

In the early days of high speed circuits, simple emitter followers were often used as high speed buffers. The term *buffer* was generally accepted to mean a unity-gain open loop amplifier such as the National LH-0033 hybrid. This device was a complementary emitter follower with an input FET source follower. The schematic of this device and a purely bipolar version is shown in Figure 10.25. Both devices achieved bandwidths of about 100MHz at fairly respectable levels of harmonic distortion. However, they suffered from dc and ac non-linearities when loaded with impedances much less than 500Ω.

EARLY OPEN-LOOP, 100MHz BANDWIDTH HYBRID BUFFERS

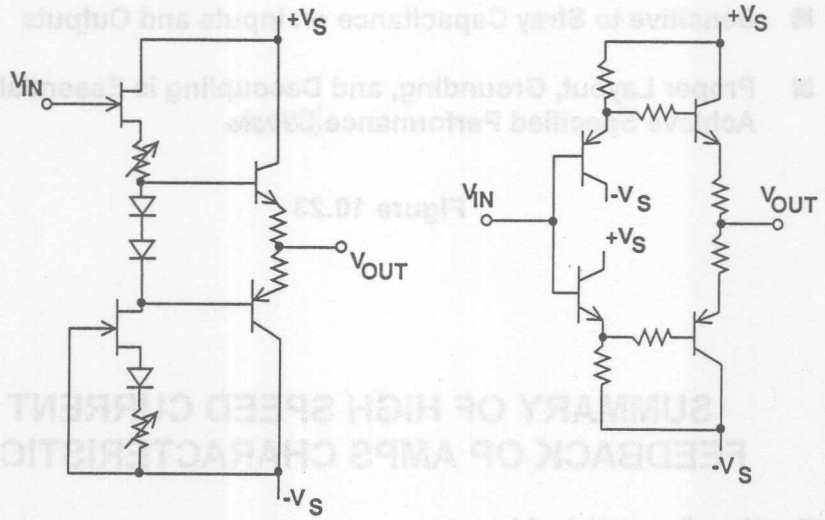


Figure 10.25

An early IC implementation of these functions was the Precision Monolithic, Inc. BUF-03 shown in Figure 10.26. (PMI is now a division of Analog Devices.) This open-loop IC buffer achieves a bandwidth of about 50MHz.

EARLY IC OPEN-LOOP, 50MHz BUFFER, THE BUF-03

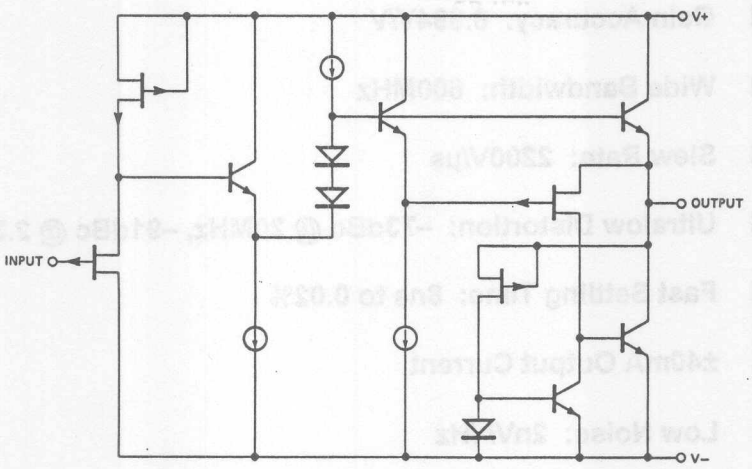


Figure 10.26

One of the problems with open loop buffers is that although high bandwidths may be achieved, these devices cannot take advantage of the "curative" effects of negative feedback. Distortion and DC performance suffers considerably when open loop buffers are loaded with typical video impedance levels of 50, 75, or 100Ω.

As IC processes evolved and high speed general-purpose op amps became available, it became possible to build relatively high speed buffers using op amps as building blocks. Usually, however, the general-purpose op amps are compensated to operate over a wide range of gains and feedback conditions. Therefore, bandwidth suffers somewhat at low gains, especially in the unity-gain non-inverting mode, because of the additional external compensation usually required.

The AD9620 is a 600MHz voltage feedback op amp which is optimized for maximum performance as a unity-gain buffer. The feedback resistor is on chip for minimum parasitic effects. The impressive specifications are summarized in Figure 10.27. Although the open loop dc gain of the AD9620 is only about 2000, the proprietary voltage feedback circuit design of the AD9620 (Patents Pending) insures that this value is relatively constant under a variety of load and frequency conditions. DC endpoint linearity for a 100Ω load is better than 60ppm (85dB) as shown in Figure 10.28. Frequency response and settling time for the AD9620 is shown in Figure 10.29, and harmonic distortion performance in Figure 10.30.

AD9620 ULTRALOW DISTORTION 600MHz BUFFER KEY SPECIFICATIONS

- Gain Accuracy: 0.994V/V
- Wide Bandwidth: 600MHz
- Slew Rate: 2200V/µs
- Ultralow Distortion: –73dBc @ 20MHz, –91dBc @ 2.3MHz
- Fast Settling Time: 8ns to 0.02%
- ±40mA Output Current
- Low Noise: 2nV/√Hz

Figure 10.27

AD9620 BUFFER DC ENDPOINT LINEARITY ERROR FOR 100Ω AND 200Ω LOADS INDICATES GOOD OPEN-LOOP GAIN STABILITY OVER SIGNAL RANGE

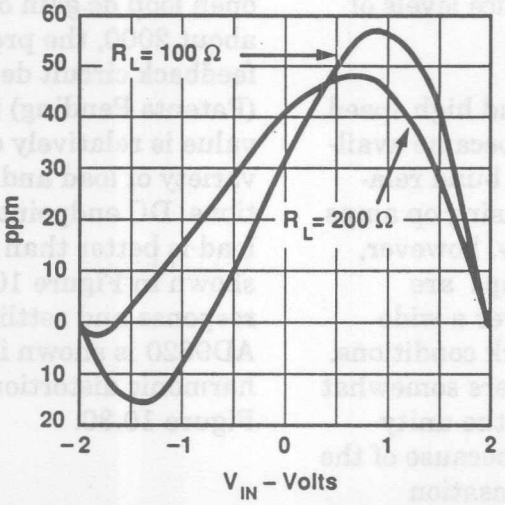


Figure 10.28

AD9620 BUFFER FREQUENCY RESPONSE AND SETTLING TIME

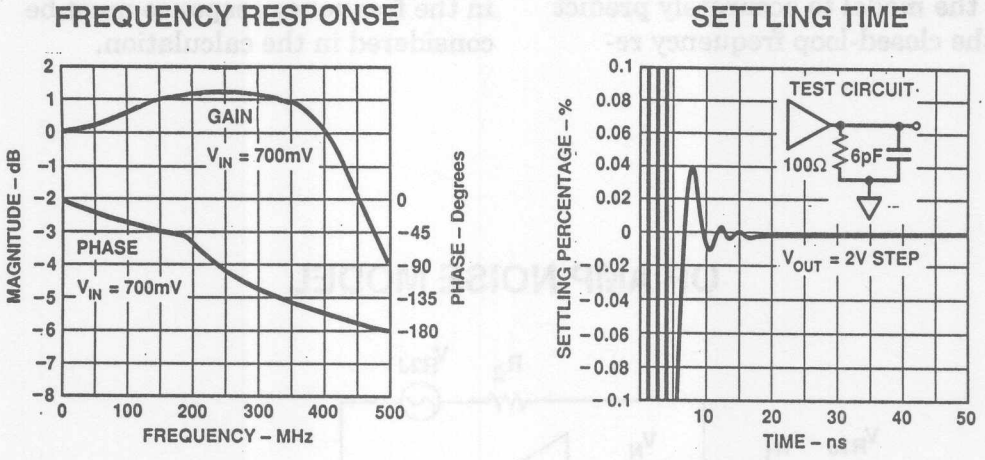


Figure 10.29

AD9620 BUFFER HARMONIC DISTORTION PERFORMANCE

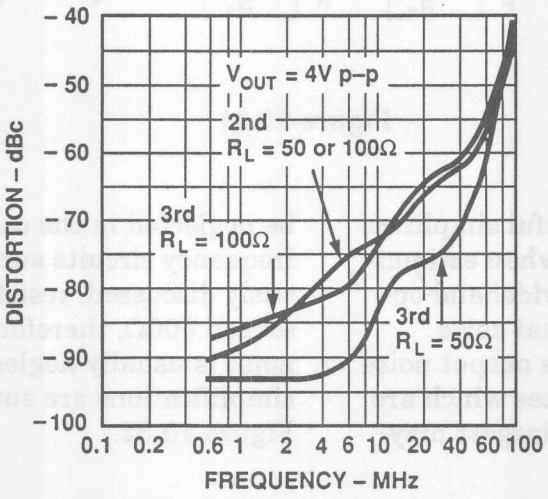
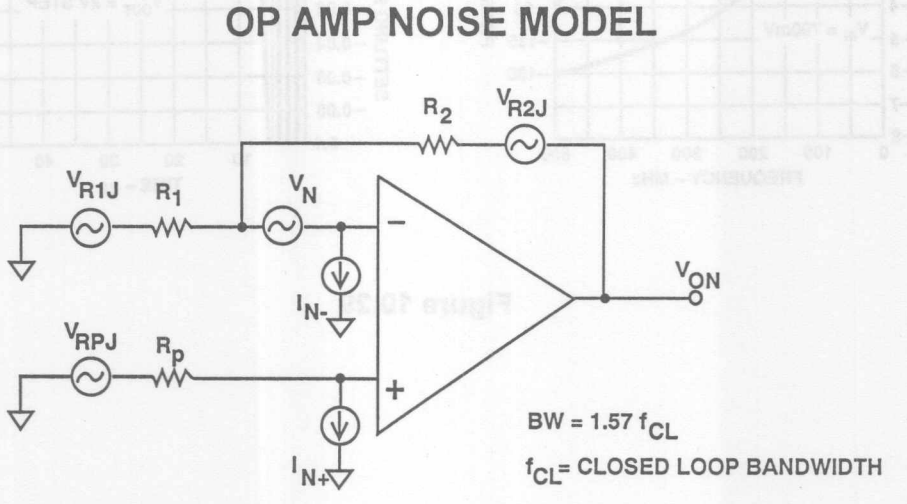


Figure 10.30

HIGH SPEED OP AMP NOISE MODELS

A generalized noise model for an op amp is shown in Figure 10.31. This model is especially suited to high speed op amp circuits where low frequency 1/f noise may usually be neglected. In order for the model to accurately predict results, the closed-loop frequency response should be flat within a few dB up to the closed-loop bandwidth frequency. In calculating the total output rms noise, the high frequency noise will dominate, and any significant peaking in the frequency response must be considered in the calculation.



$$V_{ON} = \sqrt{BW}\sqrt{I_{N-}^2 R_2^2 + I_{N+}^2 R_p^2 \left[1+\frac{R_2}{R_1}\right]^2 + V_N^2 \left[1+\frac{R_2}{R_1}\right]^2 + 4kTR_2 + 4kTR_1\left[\frac{R_2}{R_1}\right]^2 + 4kTR_p\left[1+\frac{R_2}{R_1}\right]^2}$$

Figure 10.31

There are a number of useful simplifications which can be made when estimating the output noise of a wideband op amp. Because the individual noise sources contributing to the output noise add on an rms basis, sources which are 3 to 5 times less than the largest may be neglected in the calculation. In high frequency circuits such as those previously discussed, resistor values seldom exceed 500Ω, therefore resistor Johnson noise is usually neglected. The useful simplifications are summarized in Figure 10.32.

SIMPLIFICATIONS IN ESTIMATING RMS OUTPUT NOISE FOR HIGH SPEED OP AMPS

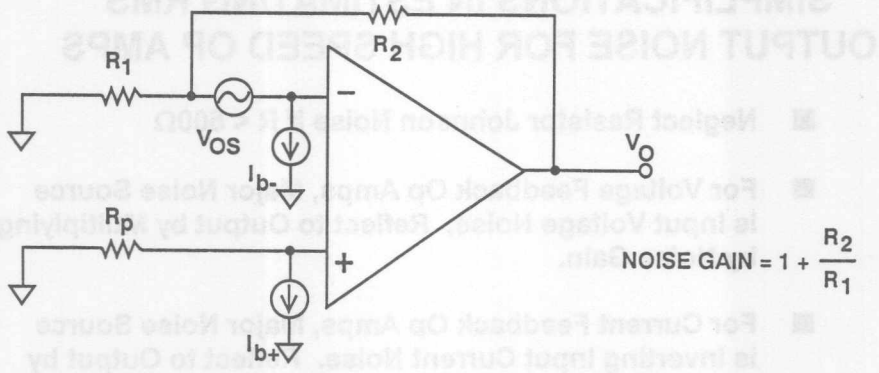
- Neglect Resistor Johnson Noise if R < 500Ω
- For Voltage Feedback Op Amps, Major Noise Source is Input Voltage Noise. Reflect to Output by Multiplying by Noise Gain.
- For Current Feedback Op Amps, Major Noise Source is Inverting Input Current Noise. Reflect to Output by Multiplying by Feedback Resistor Value.
- Use Closed-Loop Small Signal Bandwidth in Calculation

Figure 10.32

OP AMP DC MODEL

A generalized model for calculating the total output offset voltage of an op amp is shown in Figure 10.33. These equations are applicable for either voltage or current feedback op amps. However, the inputs of a voltage feedback op amp are symmetrical; therefore, the input bias currents are approximately equal provided internal bias compensation is not used. Due to the non-symmetrical input structure of the current feedback op amp, however, the bias currents are usually different, and therefore, appropriate values as given in the data sheet must be used for I_{b+} and I_{b-}.

OP AMP OFFSET VOLTAGE MODEL



$$V_O = \pm V_{OS}\left[1 + \frac{R_2}{R_1}\right] \pm I_{b+}R_p\left[1 + \frac{R_2}{R_1}\right] \pm I_{b-}R_2$$

Figure 10.33

Although small dc offset shifts are not a problem in most high frequency applications, significant shifts may produce clipping in an ADC system as shown in Figure 10.34. The output drift of the driving op amp must be summed with the offset drift of the ADC. If the drift is large, the gain must be reduced to prevent clipping, thereby reducing the overall dynamic range of the system.

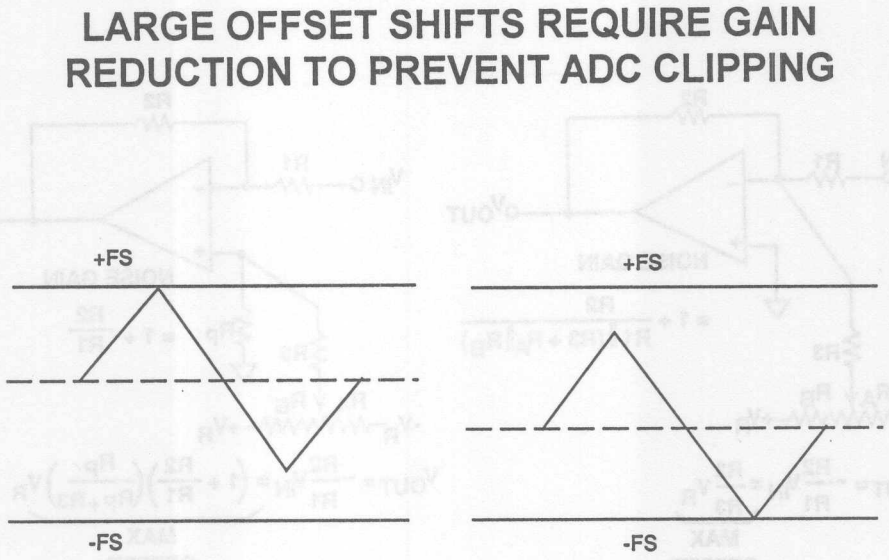


Figure 10.34

LEVEL SHIFTING HIGH SPEED SIGNALS USING OP AMPS

In addition to providing gain, op amps are often used as level shifters in signal processing systems. Figure 10.35 shows two configurations for the inverting mode. Injecting an offset current into the inverting input is probably the simplest method, but the penalty is an increase in noise gain due to R3 and the potentiometer resistance. The resulting increase in noise gain may be reduced by making V_R large enough so that R3 can be made much greater than R1 and R2.

INVERTING OP AMP LEVEL SHIFTERS

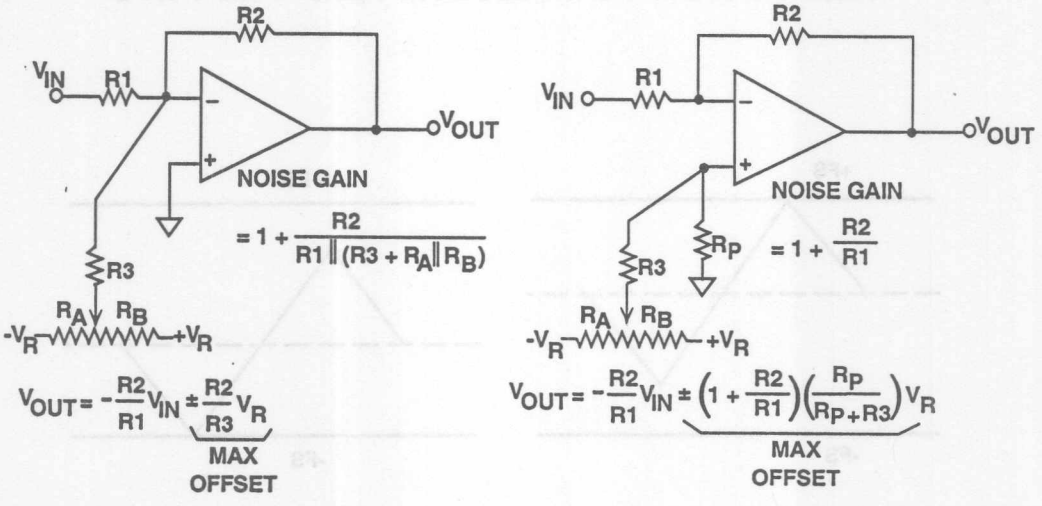


Figure 10.35

The second circuit in Figure 10.35 shows how to create an output offset by injecting the offset current into the non-inverting input. This circuit results in no increase in noise gain, but requires the addition of R_p which may affect the circuit bandwidth if it is not adequately bypassed.

The circuit shown in Figure 10.36 is used to level shift the output when using the op amp in the non-inverting mode. This circuit works well for small offsets where R3 can be made much greater than R1. Otherwise, the signal gain will be affected as the offset potentiometer is adjusted. The gain may be stabilized, however, if R3 is connected to a fixed low impedance reference voltage source.

NON-INVERTING OP AMP LEVEL SHIFTERS

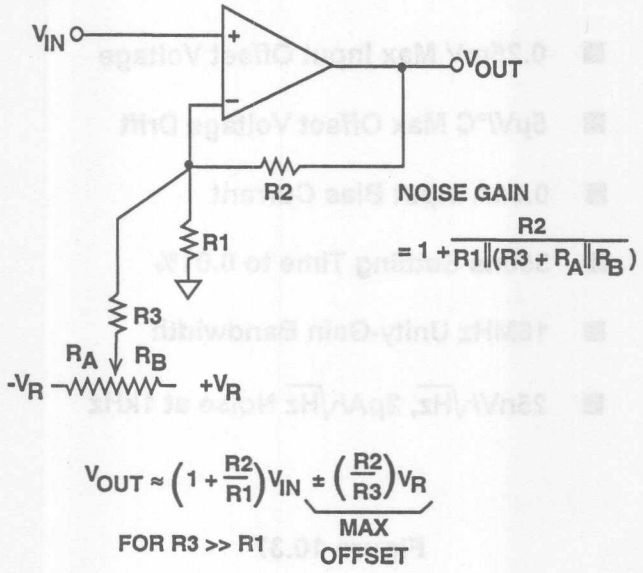


Figure 10.36

Many op amps have offset null pins available for correcting small offsets. The AD845 CBFET op amp is a good example of such an op amp. Key specifications are given in Figure 10.37 and a functional schematic in Figure 10.38. The AD845 is laser trimmed for a maximum offset voltage of 250μV and an offset temperature coefficient of 5μV/°C. The configuration shown in Figure 10.38 may be used to null out this small offset voltage, but the resulting imbalance in the current in the input differential FET pair produces an additional 4μV/°C temperature for every millivolt nulled. Therefore, nulling out 250μV of offset voltage will increase the offset temperature coefficient by approximately 1μV/°C. In no case should the offset null pins be used to correct for large system offsets!

AD845 CBFET KEY SPECIFICATIONS

- 0.25mV Max Input Offset Voltage
- 5μV/°C Max Offset Voltage Drift
- 0.5nA Input Bias Current
- 350ns Settling Time to 0.01%
- 16MHz Unity-Gain Bandwidth
- 25nV/$\sqrt{Hz}$, 2pA/$\sqrt{Hz}$ Noise at 1kHz

Figure 10.37

CAREFUL USE OF OP AMP NULL PINS IS EFFECTIVE IN REDUCING SMALL OFFSET VOLTAGES BUT MAY INCREASE TEMPERATURE COEFFICIENT

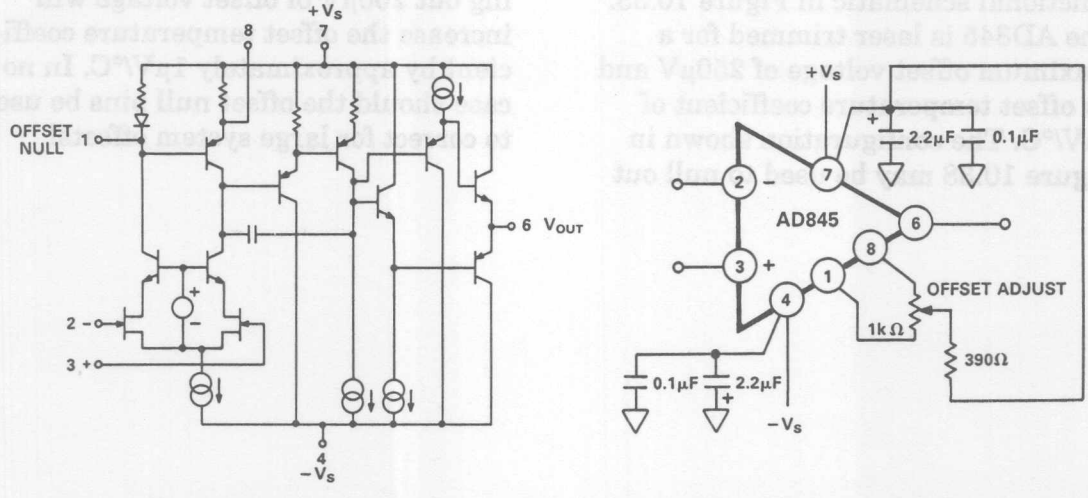


Figure 10.38

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2. Thomas M. Frederiksen, **Intuitive Operational Amplifiers**, McGraw Hill, 1988.

3. D. Stout, M. Kaufman, **Handbook of Operational Amplifier Circuit Design**, New York, McGraw-Hill, 1976.

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5. J. Dostal, Operational Amplifiers, Elsevier Scientific Publishing, New York, 1981.

6. **High Speed Design Seminar Notes**, 1990, Analog Devices.

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8. Walter G. Jung, **IC Op Amp Cookbook, Third Edition**, SAMS (Division of Macmillan, Inc.), 1986.

SECTION 11

VIDEO SIGNAL TRANSMISSION AND PROCESSING

- DRIVING CAPACITIVE LOADS WITH WIDEBAND OP AMPS:
  OUT-OF-LOOP RESISTIVE COMPENSATION FOR DRIVING CAPACITIVE LOADS, IN-THE-LOOP RESISTIVE COMPENSATION FOR DRIVING CAPACITIVE LOADS, USING OP AMPS WITH INTERNAL CAPACITIVE-LOAD COMPENSATION

- CABLE DRIVING AT VIDEO FREQUENCIES

- VIDEO SIGNAL PROCESSING:
  DIFFERENTIAL GAIN AND PHASE SPECIFICATIONS, VIDEO LINE DRIVERS, HIGH SPEED DIFFERENTIAL SIGNAL TRANSMISSION, VIDEO LINE RECEIVERS USING THE AD830 ACTIVE FEEDBACK AMPLIFIER TOPOLOGY, A COMPOSITE VIDEO SYNC TIP DC RESTORER, A VIDEO SYNC STRIPPER CIRCUIT

- MAINTAINING TRANSMISSION LINE IMPEDANCES ON THE PC BOARD

SECTION 11

VIDEO SIGNAL TRANSMISSION AND PROCESSING

Walt Kester, Walt Jung, Dave Whitney

Transmission of high speed analog signals over any distance is difficult for a number of reasons. Even a few pF of stray capacitance on the output of a high speed op amp may cause ringing and perhaps instability. For example, the capacitance of a 10 mil wide PC board trace over a ground plane (G-10 epoxy board, 60mils thick) is approximately 1.3pF/inch. Ground noise between ground planes on different PC boards makes uncorrupted transmission of single-ended signals between them difficult. This section is divided into three major areas: driving capacitive loads, driving coaxial cables, and differential signal transmission techniques.

DRIVING CAPACITIVE LOADS WITH WIDEBAND OP AMPS

Walt Jung, Walt Kester

Capacitive loading should be looked at in any driver-circuit application, however benign. Signal lead capacitance can build up quickly, even for short runs on a single PC board, and can cause high speed op amps to oscillate.

A follower-connected op amp with capacitive load is the classic case of a potential stability disaster (see Figure 11.1). For example, if the op amp has an open-loop phase shift of 135° (corresponding to a phase margin of 45°) near its unity-gain frequency, and if the pole formed by the output impedance of the op amp and the load capacitance produces an additional phase shift of 45°, severe peaking or even oscillation will result. The follower connection tends to maximize this tendency, because it involves 100% feedback.

CAPACITIVE LOADING ON OP AMP GENERALLY REDUCES PHASE MARGIN AND MAY CAUSE INSTABILITY, BUT INCREASING THE NOISE GAIN OF THE CIRCUIT IMPROVES STABILITY

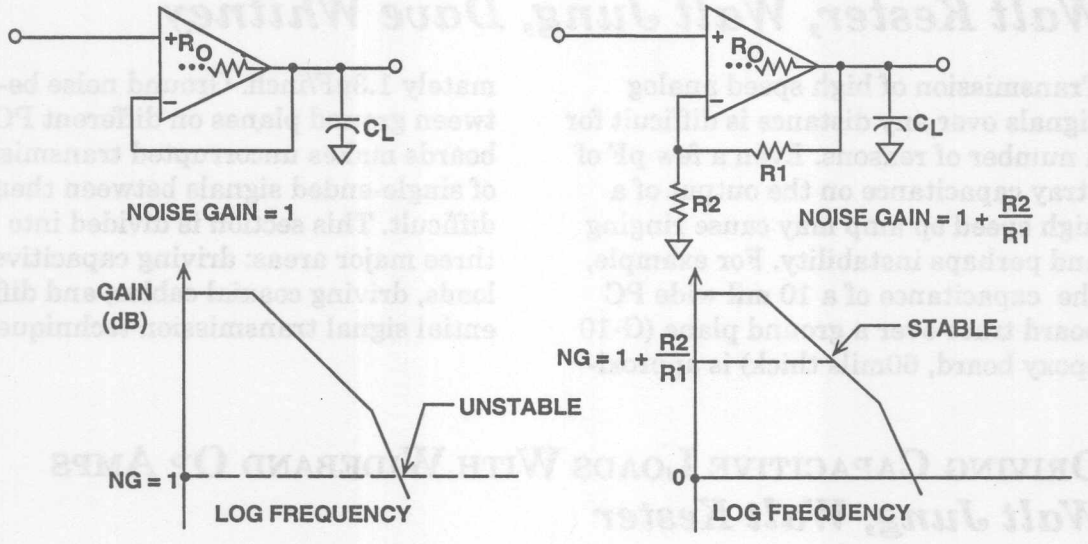


Figure 11.1

Operating at higher noise gains (reduced feedback) will also help stability of a standard voltage feedback op amp, following general feedback theory, because phase lag in generally lower at the lower unity-loop-gain frequencies. Therefore, inverters or higher-gain followers (with attenuated inputs, if necessary) will have less tendency to oscillate or peak.

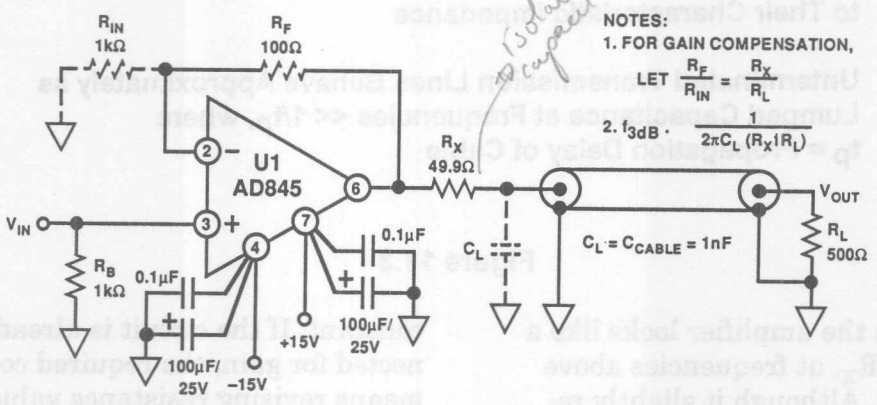
Current feedback op amps, on the other hand, are generally optimized to operate with a fixed value of feedback resistor. The closed-loop bandwidth is relatively constant regardless of the value of closed-loop gain provided this feedback resistor remains unchanged. The bandwidth can be reduced, however, by increasing the value of the feedback resistor, which decreases the sensitivity to capacitive loading.

OUT-OF-LOOP RESISTIVE COMPENSATION FOR DRIVING CAPACITIVE LOADS

Walt Jung

Another method for compensating for capacitive loading is to isolate the amplifier output from the capacitive load, using a series resistor which is outside the feedback loop as shown in Figure 11.2.

OPEN-LOOP SERIES RESISTANCE ISOLATES CAPACITIVE LOAD FOR THE AD845 VOLTAGE FEEDBACK OP AMP (CIRCUIT BANDWIDTH = 3.5MHz)



- Cable: 50Ω, 30 feet, 33pF/ft, 1.6ns/ft
- t_p = 30×1.6 = 48ns
- $1/t_p$ = 20MHz

Figure 11.2

The 30 foot cable has a capacitance of about 30pF/foot yielding an approximate lumped capacitance of about 1nF. The total propagation delay down the cable is about 1.6ns/foot, or 48ns. Since the cable is unterminated (500Ω >> 50Ω), and the circuit bandwidth is only 3.5MHz (as we shall see), the cable can be approximated by a lumped capacitive load of 1nF.

11

CABLE CAPACITANCE

- All Interconnections are Really Transmission Lines Which Have a Characteristic Impedance (Even if Not Controlled)
- The Characteristic Impedance is Equal to $\sqrt{L/C}$, where L and C are the Distributed Inductance and Capacitance
- Correctly Terminated Transmission Lines Have Impedances Equal to Their Characteristic Impedance
- Unterminated Transmission Lines Behave Approximately as Lumped Capacitance at Frequencies << $1/t_p$, where t_p = Propagation Delay of Cable

Figure 11.3

The load on the amplifier looks like a resistance, R_X, at frequencies above $1/(2\pi R_X C_L)$. Although it slightly reduces the amplifier's open-loop gain, it does not introduce additional loop phase lag, and the circuit's stability is less sensitive to C_L. However, the resistance, R_X, causes a voltage drop proportional to load current, and it must be small compared to R_L to minimize low frequency error. R_X is typically 10-100Ω, which, for loads ≥ 1kΩ, produces small (<1dB) dc errors.

For low impedance loads, such as 500Ω for R_L, a series resistance, R_X,) of 50Ω produces a 9% gain error, which often requires correction for unity overall gain, either locally or elsewhere in the system. It can be achieved locally by using feedback resistors in the same ratio, R_X/R_L; accuracy of the overall gain will depend on whether R_L is constant. If the circuit is already connected for gain, the required correction means revising resistance values for a $(1 + R_X/R_L)$ gain increase.

This technique (like almost all others to isolate capacitive loads) also causes a loss of frequency response, a loss likely to be serious with high speed amplifiers. For the example shown in Figure 11.2, the effective bandwidth will be about 3.5MHz, well below the basic 16MHz bandwidth of the AD845 op amp. In essence, the bandwidth will be limited to $1/[2\pi C_L(R_X \| R_L)]$.

In addition to reducing circuit bandwidth, the outside-the-loop series-R_X method can limit the slew rate. In general, the inherent slew rate of the amplifier will be reduced to $I_{o\ max}/C_L$. For example, while the AD845 has a basic slew rate of 100V/μs, the ±50mA

output-current limits cause the circuit slew rate to fall to about 50V/µs with C_L = 1nF. The slew rate is subject to the amplifier's short-circuit current limit, which usually varies inversely with temperature. This general limitation will apply to any capacitively loaded amplifier and is particularly acute in high slew rate devices.

Unlike voltage feedback op amps, current feedback (or transimpedance) op amps require an optimum value of R_F for flat frequency response and maximum bandwidth. For the AD811 at a gain of +1, it is 750Ω as shown in Figure 11.4. For other current feedback op amps, the optimum R_F value may be different. In all cases, the device data sheet should be consulted.

OPEN-LOOP SERIES RESISTANCE ISOLATES CAPACITIVE LOAD FOR AD811 CURRENT FEEDBACK OP AMP (CIRCUIT BANDWIDTH = 13.5MHz)

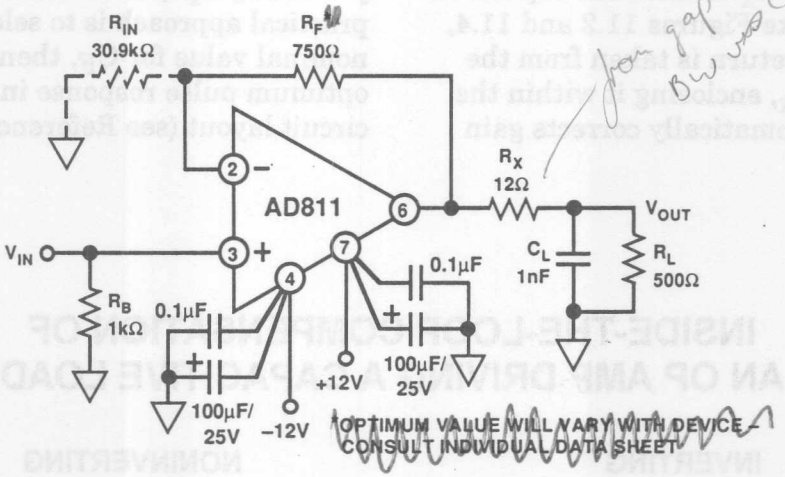


Figure 11.4

The AD811 op amp permits R_F to be increased to improve capacitive load handling for R_X = 0, but with less-flat frequency response. With R_X = 12Ω, as shown, response is optimized into a 1nF load. The AD811 has major benefits in this application, since the bandwidth is 13.5MHz compared to 3.5MHz for the AD845 circuit in Figure 11.2. The ±150mA short-circuit output drive of the AD811 increases the circuit's slew rate to 150V/µs (much less than its unloaded 2500V/µs spec, but much more than that of Figure 11.2. As in the previous example, R_{in} may be added to compensate for the gain loss due the divider action of R_X and R_L.

IN-THE-LOOP RESISTIVE COMPENSATION FOR DRIVING CAPACITIVE LOADS

Walt Jung

In-the-loop resistive compensation is the most flexible and accurate general way to isolate/compensate capacitive loads. It is flexible; in principle, it applies to any unity-gain stable op amp, in inverting or noninverting operation. It is accurate; the isolation resistor is included within a dc feedback loop for excellent low frequency gain accuracy, independent of the load and limited principally by the circuit's gain resistors (assuming adequate op amp gain). Unfortunately, like other techniques discussed thus far, it also reduces bandwidth and slew rate.

Figure 11.5 illustrates the principle. In this circuit, a noninverting gain-of-2 stage, resistor R_X isolates the capacitive load C_L. Unlike Figures 11.2 and 11.4, the feedback return is taken from the *load* side of R_X, enclosing it within the loop. This automatically corrects gain errors caused by loading at the lower frequencies. the gain expression is like that of a standard noninverting op amp stage.

Dynamically, capacitor C_F provides compensation for the additional lag introduces by the R_X-C_L combination. For a given set of values, C_F can be adjusted to cancel much of the destabilizing effect of C_L and provide a well-damped step response, countering the tendency towards overshoot, ringing, or oscillation. Bandwidth is reduced; the closed-loop bandwidth of this stage is a function of R_F and C_F, as well as R_X and C_L. While several references suggest procedures for predicting C_F (see References 3 and 7), a practical approach is to select a close nominal value for C_F, then adjust it for optimum pulse response in the final circuit layout (see Reference 8).

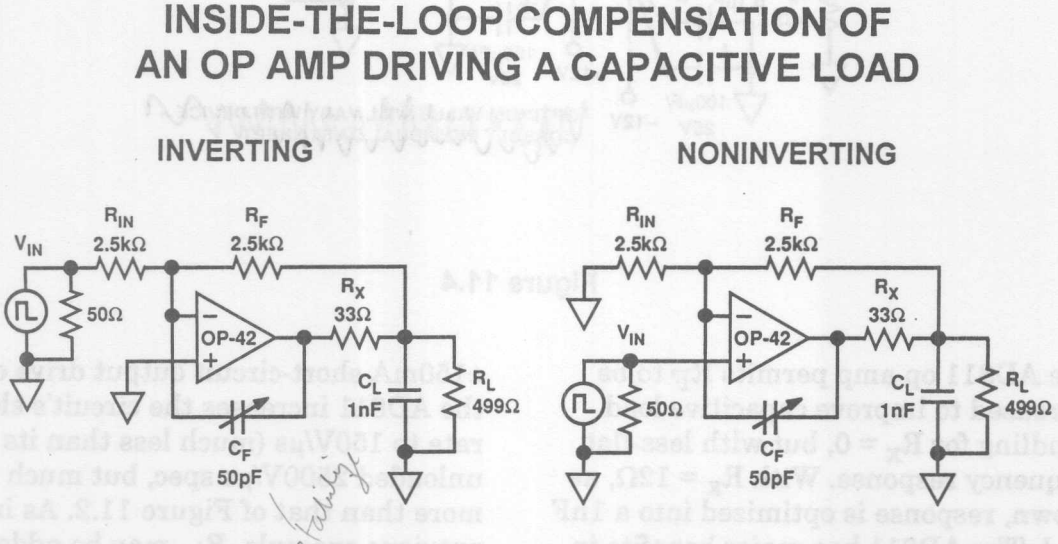


Figure 11.5

USING OP AMPS WITH INTERNAL CAPACITIVE-LOAD COMPENSATION

Walt Jung

Several Analog Devices' op amps have internal compensation for driving capacitive loads. Examples are the AD847, AD848, AD849, AD817, AD818, AD827, AD826, AD828, and the OP-160. The fundamental principle is the same and will be illustrated using the AD817 simplified schematic in Figure 11.6.

AD817 SIMPLIFIED SCHEMATIC ILLUSTRATES INTERNAL COMPENSATION FOR DRIVING CAPACITIVE LOADS

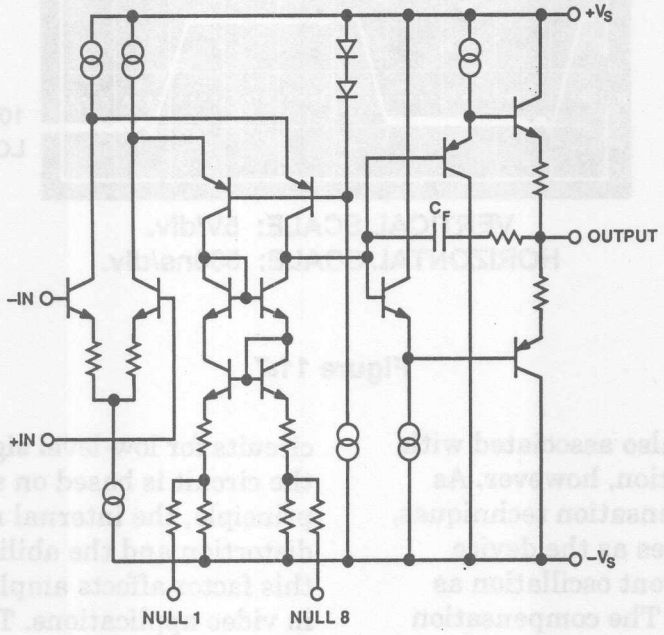
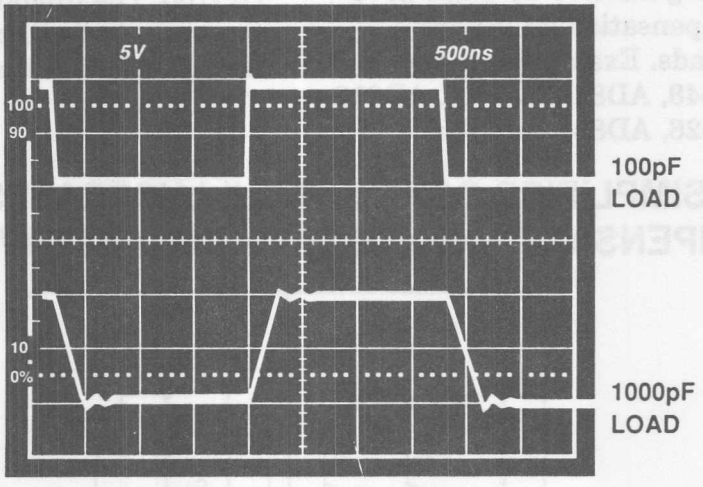


Figure 11.6

The AD817 consists of a degenerated NPN differential pair driving matched PNPs in a folded-cascode gain stage. The output buffer stage employs emitter followers in a class AB amplifier which delivers the necessary current to the load while maintaining low levels of distortion.

The capacitor, C_F, in the output stage mitigates the effect of capacitive loads. At low frequencies, and with low capacitive loads, the gain from the high-impedance compensation node to the output is very close to unity. In this case, C_F is bootstrapped and does not contribute to the overall compensation capacitance of the device. As the capacitive load is increased, a pole is formed with the output impedance of the output stage. This reduces the gain, and therefore, C_F is incompletely bootstrapped. Effectively, some fraction of C_F contributes to the overall compensation capacitance, reducing the unity gain bandwidth. As the load capacitance is further increased, the bandwidth continues to fall, maintaining stability of the amplifier. Figure 11.7 shows the AD817 pulse response for a 100pF load and a 1000pF load.

INTERNAL COMPENSATION MAKES THE AD817 STABLE WHEN DRIVING LARGE CAPACITVE LOADS



VERTICAL SCALE: 5V/div.
HORIZONTAL SCALE: 500ns/div.

Figure 11.7

Some caveats are also associated with internal compensation, however. As with passive compensation techniques, bandwidth decreases as the device slows down to prevent oscillation as load current flows. The compensation network has its greatest effect when enough output current flows to produce voltage across C_F. Conversely, at small signal levels the effect of the network on speed is much less, so greater ringing may actually be possible for some circuits for low-level signals. Because the circuit is based on a nonlinear principle, the internal network affects distortion and the ability to drive loads; this factor affects amplifier performance in video applications. Though it does not by any means make the AD847 or AD817 unusable for video, it does not permit the very lowest levels of distortion and differential gain and phase achieved by otherwise comparable amplifiers.

CABLE DRIVING AT VIDEO FREQUENCIES

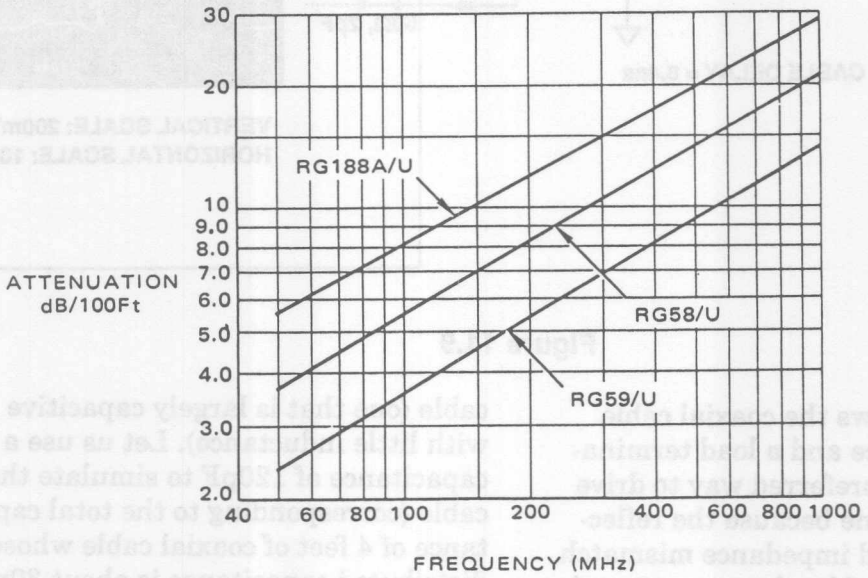
Walt Kester

The capacitive-load compensation techniques described above are hardly a perfect solution to the line-driving problem. Perhaps the best and most foolproof way to drive a long line (which might otherwise present substantial capacitive load) is to use a transmission line. This has been the standard for signal distribution in video and RF systems for years. When properly driven and terminated, bandwidth limitations are greatly reduced.

A transmission line correctly terminated with pure resistance (no reactive component) does not look capacitive. It has a controlled distributed capacitance per foot (C) and a controlled distributed

inductance per foot (L). The characteristic impedance of the line is given by the equation $Z_0 = \sqrt{(L/C)}$. Coaxial cable is the most popular form of single-ended transmission line and comes in characteristic impedances of 50Ω, 75Ω, and 93Ω. Because of skin effect, it exhibits a loss which is a function of frequency as shown in Figure 11.8 for several popular coaxial cables (Reference 4). Skin effect also affects the pulse response of long coaxial cables. The response to a fast pulse will rise sharply for the first 50% of the output swing, then taper off during the remaining portion of the edge. Calculations show that the 10 to 90% waveform risetime is 30 times greater than the 0 to 50% risetime when the cable is skin effect limited (Reference 4).

COAXIAL CABLE ATTENUATION VERSUS FREQUENCY



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Figure 11.8

To illustrate the behavior of a high speed op amp driving a coaxial cable, consider the circuit of Figure 11.9. The AD9617 drives 4 feet of high-quality Belden 9223 50Ω cable which is terminated in the characteristic impedance of 50Ω. The pulse response is also shown on Figure 11.9. The output of the cable was measured by connecting the test fixture directly to the 50Ω input of a 400MHz Tektronix 2465B oscilloscope. The 50Ω resistor termination is actually the input of the scope. The 50Ω load is not a perfect termination (the scope input capacitance is about 2pF), so some of the pulse is reflected back to the source. When the reflection reaches the low impedance source, it is reflected out-of-phase back to the load. The delay of the cable is about 1.6ns/foot, and you can see this small reflection which occurs about 13ns after the leading and trailing edge of the pulse. This is equal to the round-trip delay of the cable. In the frequency domain, the cable mismatch will cause a loss of bandwidth flatness at the load.

PULSE RESPONSE OF AD9617 DRIVING 4 FEET OF LOAD-TERMINATED COAXIAL CABLE

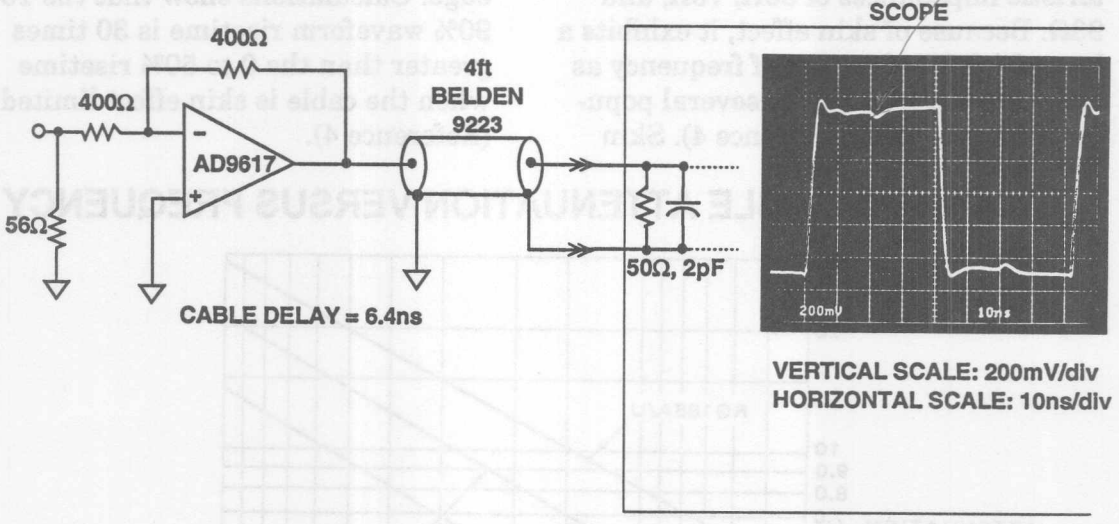


Figure 11.9

Figure 11.10 shows the coaxial cable with both a source and a load termination. This is the preferred way to drive a transmission line because the reflection from the load impedance mismatch is largely absorbed by the source termination resistor. The disadvantage is that there is a 2× gain reduction because of the voltage division between the source and load terminations. But source and load terminations in conjunction with a low-loss cable ensure the best bandwidth flatness.

Now, let us replace the 4feet of coaxial cable with an uncontrolled-impedance cable (one that is largely capacitive with little inductance). Let us use a capacitance of 120pF to simulate the cable (corresponding to the total capacitance of 4 feet of coaxial cable whose distributed capacitance is about 30pF/foot). Figure 11.11 shows the output of the AD9617 driving a lumped 120pF capacitor. Notice the overshoot and ringing on the pulse waveform due to the capacitive loading. This illustrates the need to use good quality controlled-impedance coaxial cable in the transmission of high frequency signals.

PULSE RESPONSE OF AD9617 DRIVING 4 FEET OF SOURCE AND LOAD-TERMINATED COAXIAL CABLE

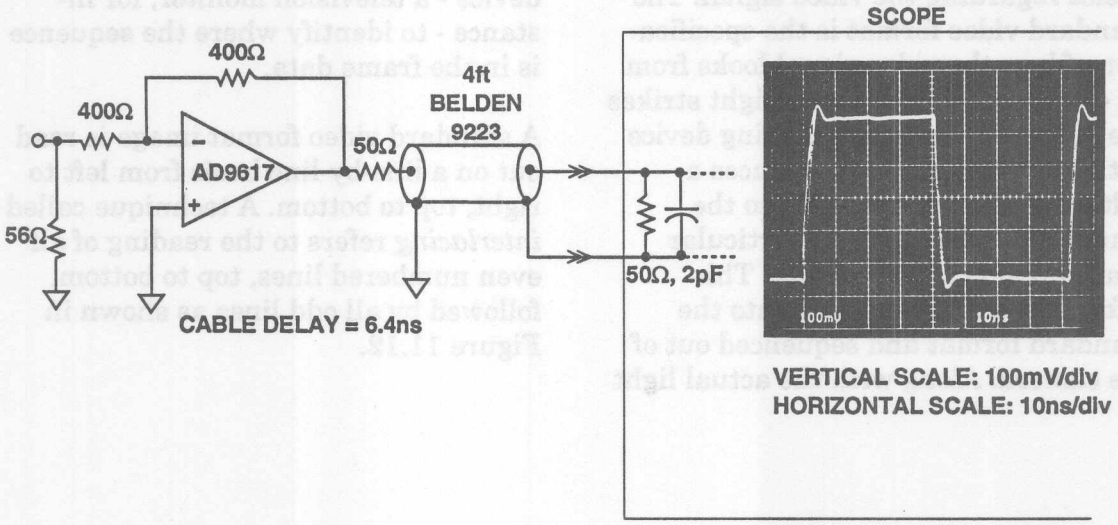


Figure 11.10

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PULSE RESPONSE OF AD9617 DRIVING 120pF ‖ 50Ω LOAD

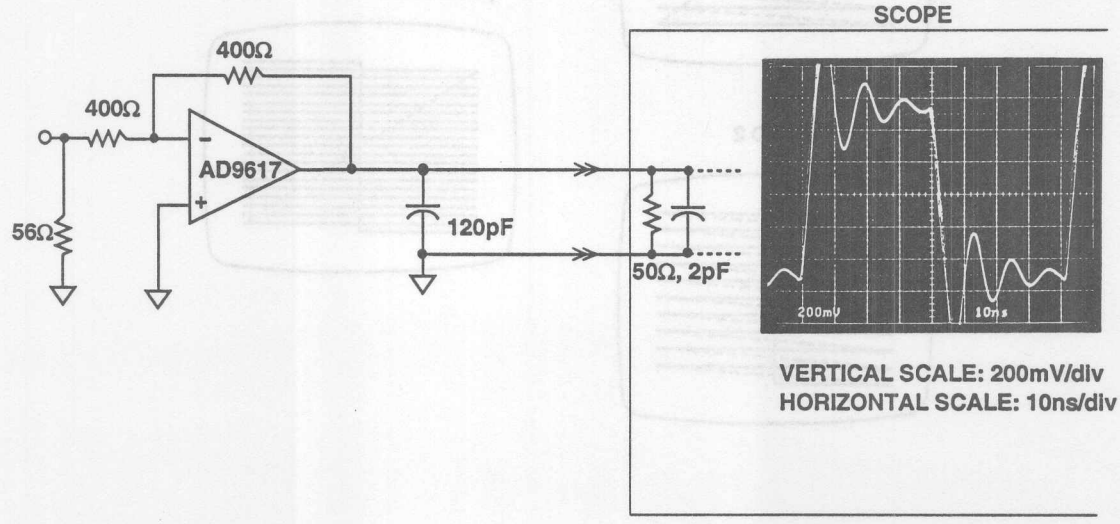


Figure 11.11

VIDEO SIGNAL PROCESSING

Walt Kester, Walt Jung, Dave Whitney

Before discussing a few professional video applications, we will review some basics regarding the video signal. The standard video format is the specification of how the video signal looks from an electrical point of view. Light strikes the surface of an image sensing device within the camera and produces a voltage level corresponding to the amount of light hitting a particular spatial region of the surface. This information is then placed into the standard format and sequenced out of the camera. Along with the actual light and color information, synchronization pulses are added to allow the receiving device - a television monitor, for instance - to identify where the sequence is in the frame data.

A standard video format image is read out on a line-by-line basis from left to right, top to bottom. A technique called *interlacing* refers to the reading of all even numbered lines, top to bottom, followed by all odd lines as shown in Figure 11.12.

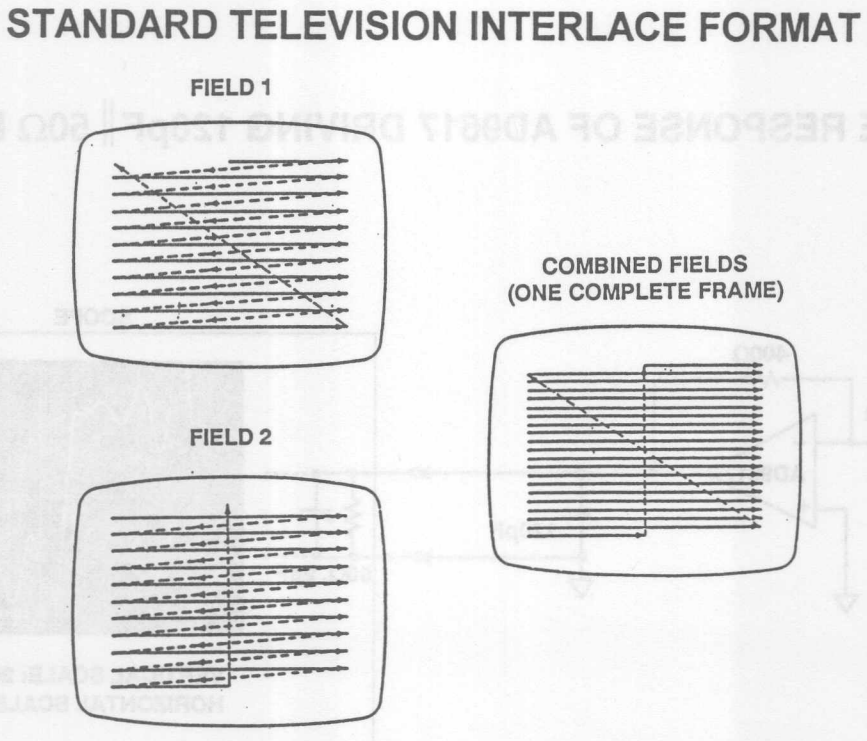


Figure 11.12

The television picture *frame* is thus divided into even and odd *fields*. Interlacing is used to produce an apparent update of the entire frame in half the time that a full update actually occurs. This results in a television image with less apparent flicker. Typical broadcast television frame update rates are 30 and 25 Hz, depending upon the line frequency.

The original black and white, or *monochrome*, television specification in the USA is the EIA RS-170 specification which prescribes all timing and voltage level requirements for standard commercial broadcast video signals. The standard American specification for color signals, NTSC, modifies RS-170 to work with color signals by adding color information to the signal which otherwise contains only brightness information.

A video signal comprises a series of analog television lines. Each line is separated from the next by a synchronization pulse called the *horizontal sync*. The fields of the picture are separated by a longer synchronization pulse called the *vertical sync*. In the case of a monitor receiving the signal, its electron beam scans the face of the display tube with the brightness of the beam controlled by the amplitude of the video signal. Whenever a horizontal sync pulse is detected, the beam is reset to the left side of the screen and moved down to the next line position. A vertical sync pulse, indicated by a horizontal sync pulse of longer duration, resets the beam to the top left point of the screen to a line centered between the first two lines of the previous scan. This allows the current field to be displayed between the previous one. A single line of an NTSC color video signal is shown in Figure 11.13, and the field timing diagram in Figure 11.14.

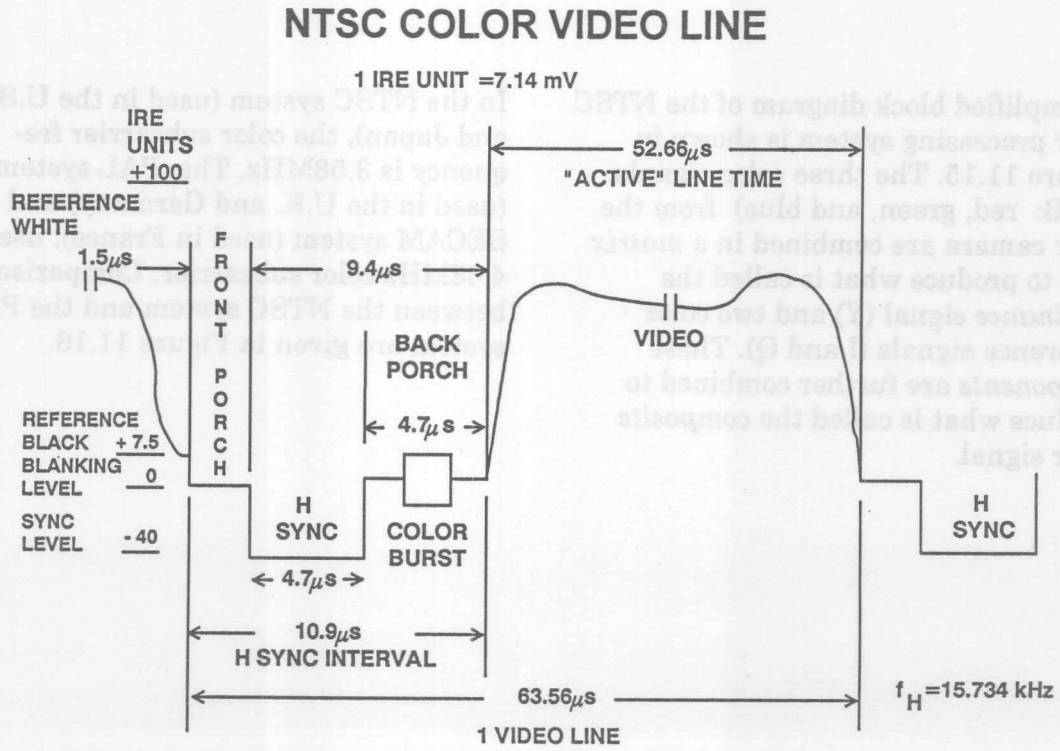


Figure 11.13

NTSC FIELD TIMING DIAGRAM

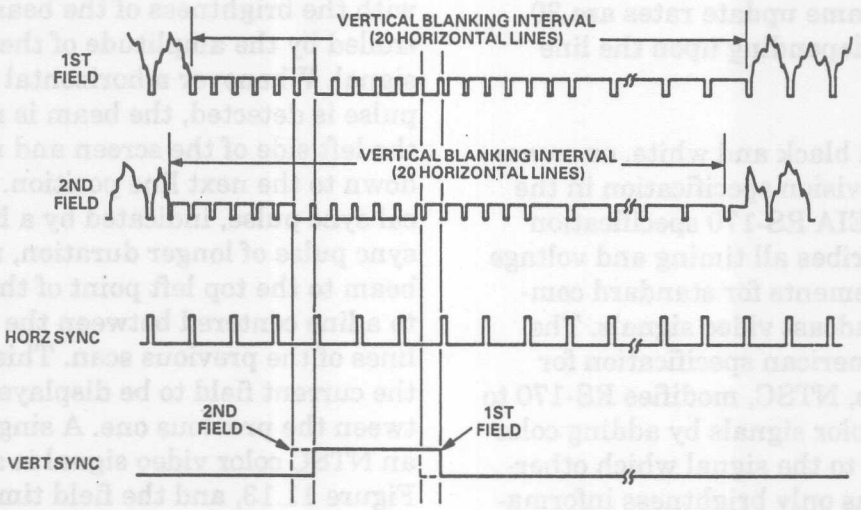


Figure 11.14

A simplified block diagram of the NTSC color processing system is shown in Figure 11.15. The three color signals (RGB: red, green, and blue) from the color camera are combined in a *matrix* unit to produce what is called the *luminance* signal (Y) and two color difference signals (I and Q). These *components* are further combined to produce what is called the *composite* color signal.

In the NTSC system (used in the U.S. and Japan), the color subcarrier frequency is 3.58MHz. The PAL system (used in the U.K. and Germany) and SECAM system (used in France), use a 4.43MHz color subcarrier. Comparisons between the NTSC system and the PAL system are given in Figure 11.16.

GENERATING THE COMPOSITE NTSC COLOR SIGNAL

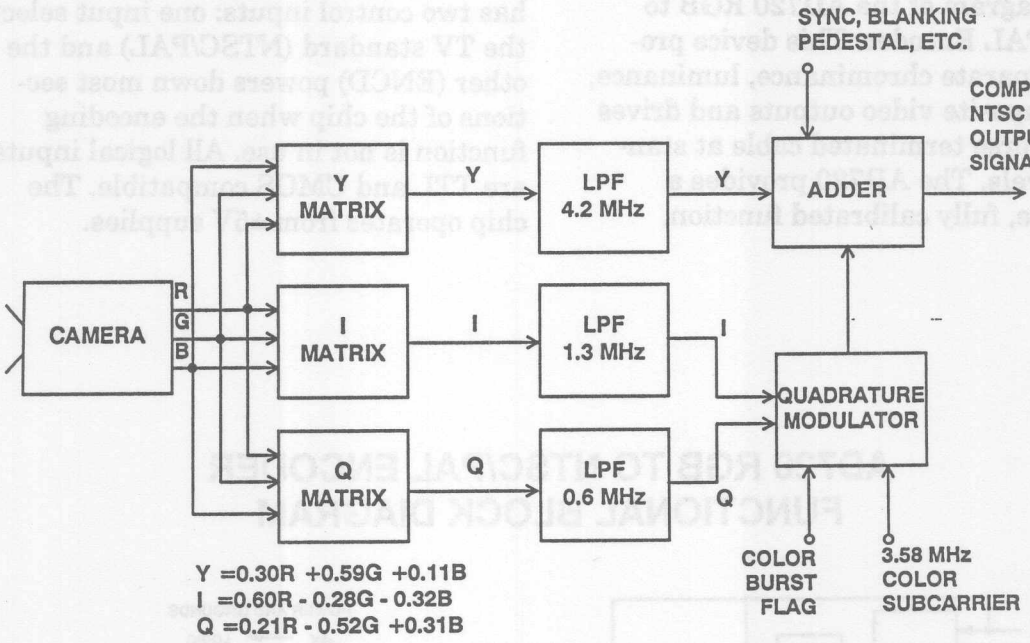


Figure 11.15

11

NTSC AND PAL SIGNAL CHARACTERISTICS

	NTSC	PAL
Horizontal Lines	525	625
Color Subcarrier Frequency	3.58MHz	4.43MHz
Frame Frequency	30Hz	25Hz
Field Frequency	60Hz	50Hz
Horizontal Sync Frequency	15.734kHz	15.625kHz

Figure 11.16

High performance LSI circuits are now available which perform the majority of the complete RGB-to-composite conversion. Figure 11.17 shows a functional block diagram of the AD720 RGB to NTSC/PAL Encoder. This device provides separate chrominance, luminance, and composite video outputs and drives 75Ω reverse terminated cable at standard levels. The AD720 provides a complete, fully calibrated function, requiring only termination resistors, decoupling networks, a clock input at four times the subcarrier frequency, and a composite sync pulse. The AD720 has two control inputs: one input selects the TV standard (NTSC/PAL) and the other (ENCD) powers down most sections of the chip when the encoding function is not in use. All logical inputs are TTL and CMOS compatible. The chip operates from ±5V supplies.

AD720 RGB TO NTSC/PAL ENCODER FUNCTIONAL BLOCK DIAGRAM

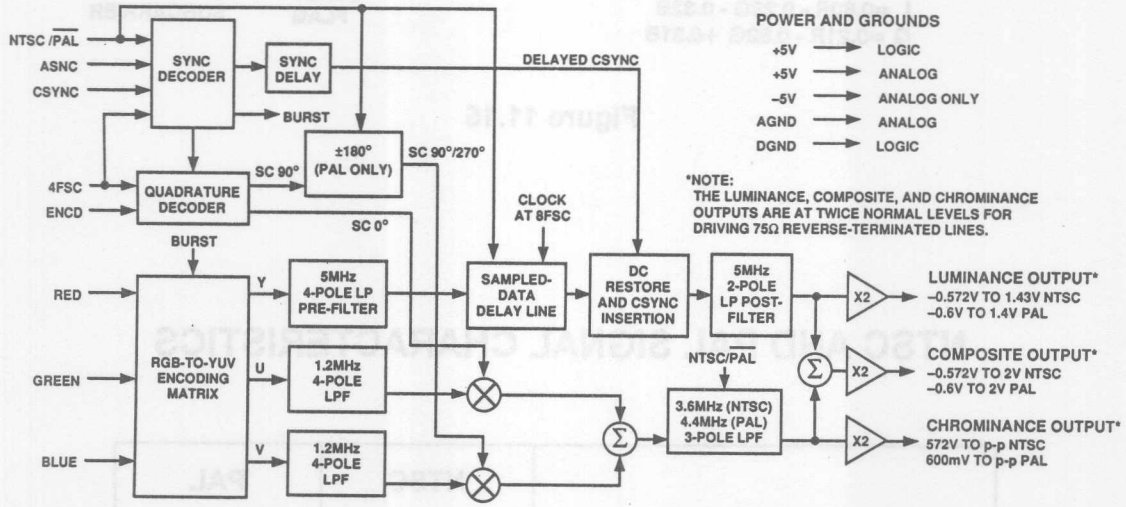


Figure 11.17

All required lowpass filters are on chip. After the input signals pass through a precision RGB to YUV encoding matrix, two on-chip filters limit the bandwidth of the U and V color-difference signals to 1.2MHz prior to quadrature modulation of the color subcarrier; a third lowpass filter at 3.6MHz (NTSC) or 4.4MHz (PAL) follows the modulators to limit the harmonic content of the output. Delays in the U and V chroma filters are matched by an on-chip

sampled-data delay line in the Y signal path; to prevent aliasing, a prefilter at 5MHz is included ahead of the delay line and a postfilter at 5MHz is added after the delay line to suppress harmonics in the output. These lowpass filters are optimized for minimum pulse overshoot. The AD720 is available in a 28 pin PLCC for the 0°C to +70°C commercial temperature range.

DIFFERENTIAL GAIN AND PHASE SPECIFICATIONS
Walt Kester

The color (or *chrominance*) information in the composite video signal is contained in the amplitude and phase of the subcarrier. The *intensity* or *saturation* of the color is determined by the amplitude of the subcarrier signal, and the precise color displayed (i.e. red, green, blue, and combinations) is determined by the phase of the subcarrier signal with respect to the phase of the color burst.

The chrominance signal modulates the luminance signal which determines the relative blackness or whiteness of the color. Therefore, in order to preserve color fidelity, it is important that the amplitude and phase of a constant-amplitude and phase color subcarrier remain constant across the entire range from black to white. Any variation of the *amplitude* of the color subcarrier from black to white levels is called *differential gain* (expressed in %), and any variation in phase with respect to the color subcarrier is called *differential phase* (expressed in degrees). Although several percent differential gain and several degrees differential phase is acceptable for home viewing purposes, individual components in the signal path (such as amplifiers, switches, etc.) must meet much tighter specifications. This is because the signal must pass through many circuits from the camera to the home. Individual professional video systems therefore have stringent requirements for differential gain and phase, usually limiting changes to less than 0.1% and 0.1°. These system specifications mandate even more stringent standards for individual components, with the differential gain and differential phase requirements for op amps approaching 0.01% and 0.01°.

Figure 11.18 shows a high resolution setup that uses a HP3314A waveform generator and a HP8753A network analyzer to measure differential gain and phase to better than 0.01% and 0.01° accuracy. The arbitrary waveform generator generates a staircase that simulates the luminance (picture level) portion of the video waveform. The network analyzer supplies the color subcarrier waveform, in this case a 4.43MHz color subcarrier. The network analyzer also measures the differences in the color subcarrier's phase and gain by comparing the output of the DUT and the reference signal returned by the HP11850 signal splitter. The 4.43MHz color subcarrier and the staircase signal are summed at the input to the op amp. This summing action superimposes the color subcarrier on the staircase, thus generating the standard video test waveform. The differential phase and gain is defined as the maximum difference in the phase or gain between any of the steps in the staircase waveform. Actual measurements taken on an op amp are shown in Figure 11.19.

PRECISION MEASUREMENT OF DIFFERENTIAL GAIN AND PHASE

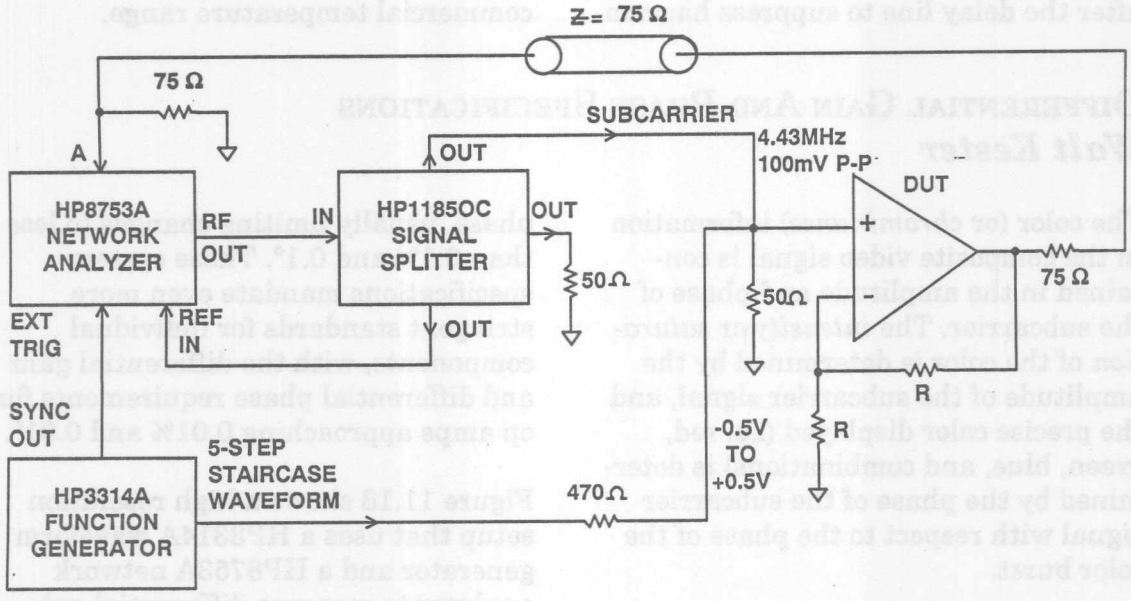


Figure 11.18

DIFFERENTIAL GAIN AND PHASE MEASURED WITH PRECISION TEST SET

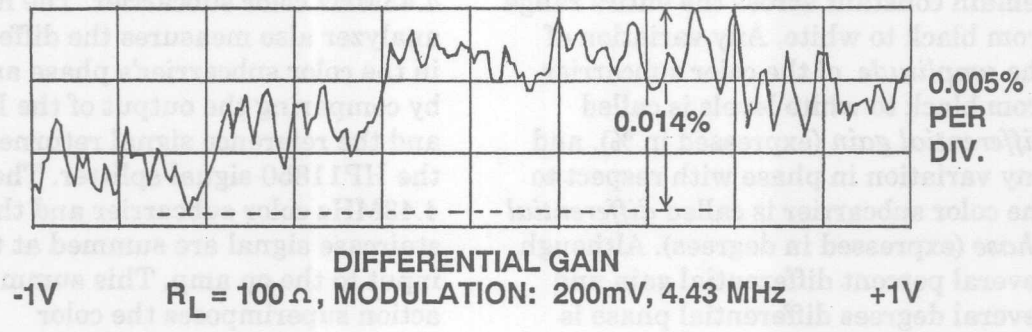


Figure 11.19

The op amp under test is shown connected as a gain-of-two amplifier driving a 75Ω reverse-terminated line. The 75Ω series termination resistor absorbs any reflections from the line termination mismatch. The 75Ω termination resistor and the 75Ω load form a voltage divider, so the net gain from the input to the DUT circuit to the load is unity.

VIDEO LINE DRIVERS
Walt Jung

The basic video line driver circuit of Figure 11.20 utilizes the low cost AD818 voltage feedback op amp. The stage gain is set at 2× by making R_F = R_{IN} = 499Ω. These values are chosen to be fairly low in order to maximize bandwidth. The AD818 is internally compensated for stable operation at a noise gain of 2 or greater, with a maximum bandwidth of over 50MHz. Quiescent current is only 6mA. As shown in Figure 11.20, the AD818 achieves its best differential gain and phase at higher supply voltages.

BASIC (GOOD) VIDEO LINE DRIVER USING THE AD818 OP AMP HAS 50MHz BANDWIDTH

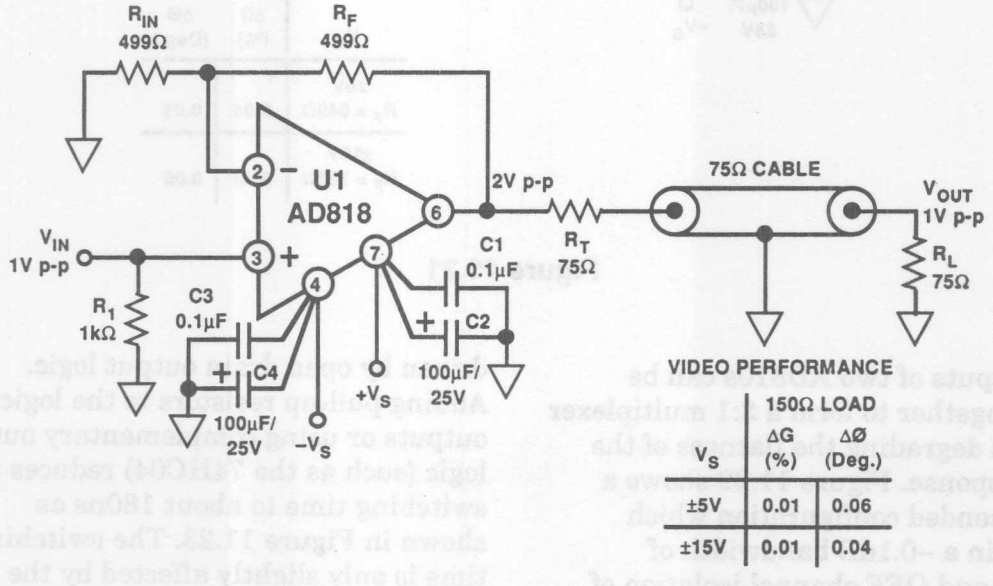
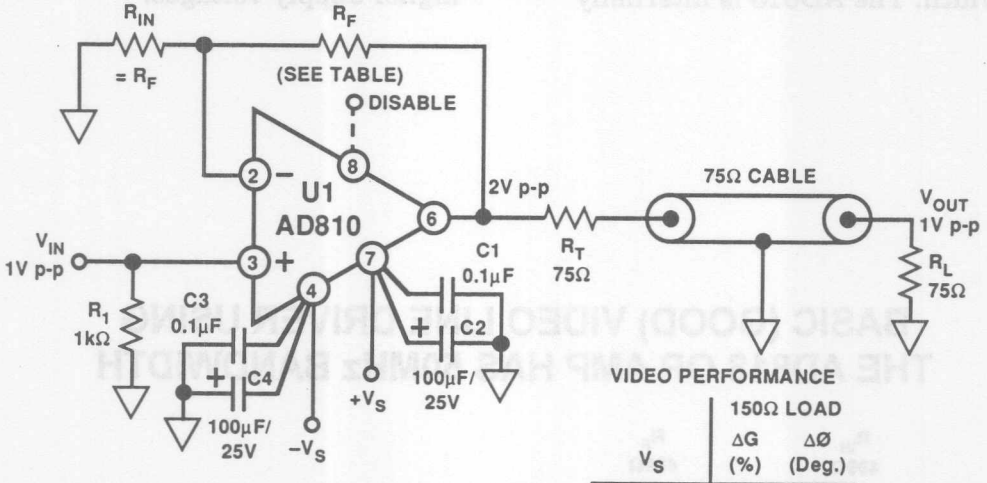


Figure 11.20

Figure 11.21 shows a higher-performance video line driver using the AD810 transimpedance amplifier. This circuit is also inexpensive, but it can perform better than the circuit of Figure 11.20 because of the AD810's appreciably higher slewrate and bandwidth, plus its higher output current. The AD810 has a 3dB bandwidth of 65MHz, and a 0.1dB bandwidth of 20MHz. Quiescent current is only 8mA. A unique feature of the AD810 is its power-down mode. The DISABLE pin is active-low to shut the device down to a standby current drain of 2mA, with 60dB input isolation at 10MHz. This permits on/off control of a single amplifier, or "wire or-ing" the outputs of a number of devices to achieve a multiplexing function.

HIGH PERFORMANCE (BETTER) VIDEO LINE DRIVER USING THE AD810 HAS DISABLE MODE, 65MHz BANDWIDTH (–3dB), AND 20MHz BANDWIDTH (–0.1dB)



VIDEO PERFORMANCE

	150Ω LOAD	
V_S	ΔG (%)	ΔØ (Deg.)
±5V R_F = 649Ω	0.04	0.05
±15V R_F = 750Ω	0.03	0.05

Figure 11.21

The outputs of two AD810s can be wired together to form a 2:1 multiplexer without degrading the flatness of the gain response. Figure 11.22 shows a recommended configuration which results in a –0.1dB bandwidth of 20MHz and OFF channel isolation of 77dB at 10MHz on ±5V supplies. The time to switch between channels is about 750ns when the disable pins are driven by open drain output logic. Adding pull-up resistors to the logic outputs or using complementary output logic (such as the 74HC04) reduces the switching time to about 180ns as shown in Figure 11.23. The switching time is only slightly affected by the signal level. The OFF channel feedthrough of the circuit is also shown in Figure 11.23.

A 2:1 VIDEO MULTIPLEXER USING AD810s HAS –0.1dB BANDWIDTH OF 20MHz AND SWITCHES IN 180ns

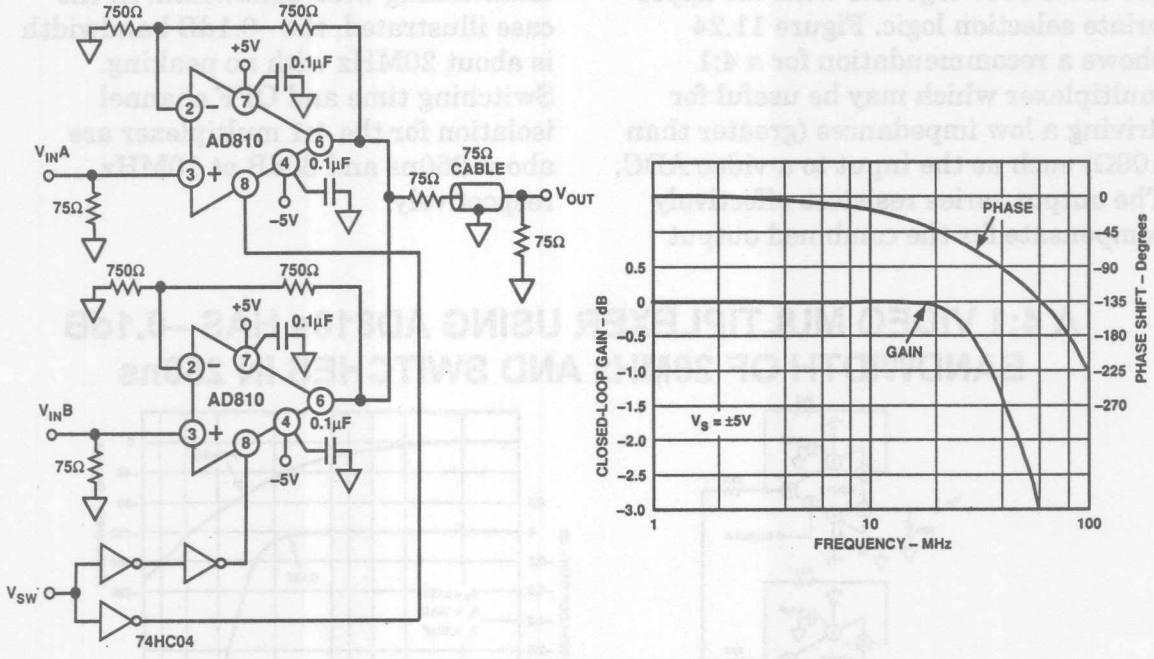


Figure 11.22

11

CHANNEL SWITCHING TIME AND OFF CHANNEL FEEDTHROUGH FOR THE 2:1 VIDEO MULTIPLEXER

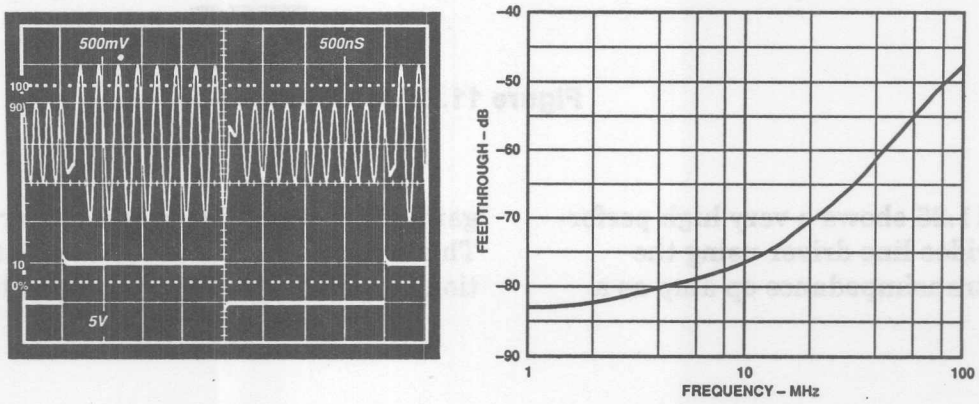


Figure 11.23

A multiplexer of arbitrary size can be formed by combining the desired number of AD810s together with the appropriate selection logic. Figure 11.24 shows a recommendation for a 4:1 multiplexer which may be useful for driving a low impedances (greater than 100Ω) such as the input to a video ADC. The output series resistors effectively compensate for the combined output capacitance of the OFF channels plus the input capacitance of the ADC while maintaining wide bandwidth. In the case illustrated, the –0.1dB bandwidth is about 20MHz with no peaking. Switching time and OFF channel isolation for the 4:1 multiplexer are about 250ns and 60dB at 10MHz, respectively.

A 4:1 VIDEO MULTIPLEXER USING AD810s HAS –0.1dB BANDWIDTH OF 20MHz AND SWITCHES IN 250ns

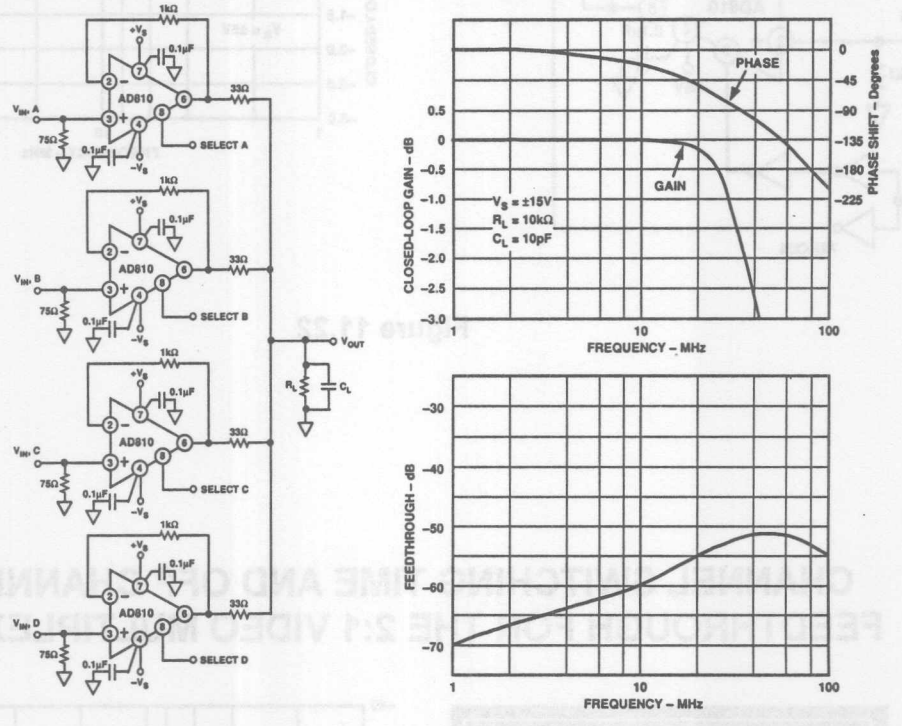


Figure 11.24

Figure 11.25 shows a very high performance video line driver using the AD811 transimpedance op amp as a gain-of-2 video buffer or line driver. This circuit also acts as a video distribution amplifier, driving two output lines.

HIGHER PERFORMANCE (EVEN BETTER) VIDEO LINE DRIVER/DISTRIBUTION AMPLIFIER USING AD811 HAS 120MHz BANDWIDTH (–3dB), AND 35MHz BANDWIDTH (–0.1dB)

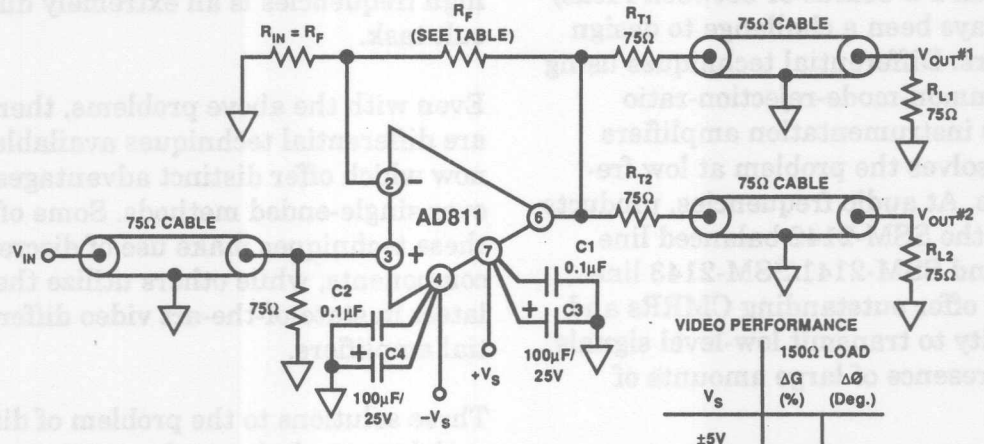


Figure 11.25

Construction of these video circuits should be in accordance with high speed rules. A solid, heavy copper ground plane should be used, and circuit layout should be compact with low capacitance, especially at the inverting input pin. In fact, the ground plane area immediately surrounding the inverting input pins should be etched away to ensure minimum stray capacitance at this critical node. In addition, the power supplies should be well bypassed. As a minimum, local low inductance/low ESR RF ceramic bypass capacitors should be used right at the device supply pins. These are 0.1μF surface mount chips (or other low inductance types). These capacitors should be augmented by local, short lead/large value low ESR electrolytics in the range of 47 to 100μF. These capacitors can be either tantalum, or aluminum types rated for high frequency (i.e., switching supply types).

HIGH SPEED DIFFERENTIAL SIGNAL TRANSMISSION

Walt Kester, Walt Jung

The transmission of high quality signals across noisy interfaces (either between individual PC boards or between racks) has always been a challenge to design engineers. Differential techniques using high common-mode-rejection-ratio (CMRR) instrumentation amplifiers largely solves the problem at low frequencies. At audio frequencies, products such as the SSM-2142 balanced line driver and SSM-2141/SSM-2143 line receiver offer outstanding CMRRs and the ability to transmit low-level signals in the presence of large amounts of noise.

The problem at video frequencies is twofold. First, video signals are generally single-ended and therefore don't adapt easily to balanced transmission line techniques. In addition, shielded twin-conductor coaxial cable with good bandwidth is usually somewhat bulky and expensive. Finally, designing high bandwidth, low distortion differential video amplifiers with high CMRRs at high frequencies is an extremely difficult task.

Even with the above problems, there are differential techniques available now which offer distinct advantages over single-ended methods. Some of these techniques make use of discrete components, while others utilize the latest in state-of-the-art video differential amplifiers.

Three solutions to the problem of differential transmission and reception are shown in Figure 11.26. The first represents the ideal case, where a balanced differential line driver drives a balanced twin-conductor coaxial cable which in turn drives a differential line receiver. This circuit, however, is difficult to implement fully at video frequencies for the reasons previously discussed.

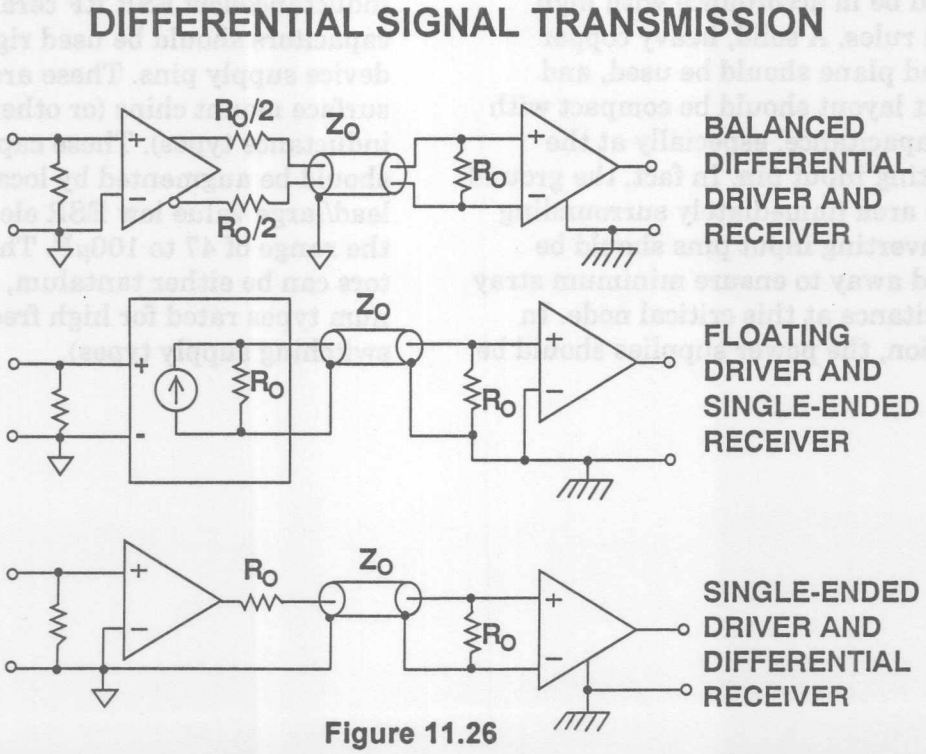


Figure 11.26

The second approach shown in Figure 11.26 uses a floating line driver (represented by the floating current source) to drive a single-conductor coaxial cable which is terminated at the receiving end in its characteristic impedance. Both the shield and the center conductor of the cable are driven by the floating line driver, and the cable is terminated at the receiving end. In this manner, noise between the two ground systems is isolated from the receiver output by the CMRR of the floating line driver.

The third and most often used approach makes use of a single-ended driver which drives a source-terminated coaxial cable. The shield of the coaxial cable is grounded at the transmitting end. At the receiving end, the coaxial cable is terminated in its characteristic impedance, but the shield is left floating. The common mode ground noise is rejected by the CMRR of the differential line receiver. The success of this approach depends upon the characteristics of the line receiver.

Figure 11.27 shows a practical implementation of the third approach in a single-ended 75Ω video transmission system.

SINGLE-ENDED DRIVER AND DIFFERENTIAL RECEIVER

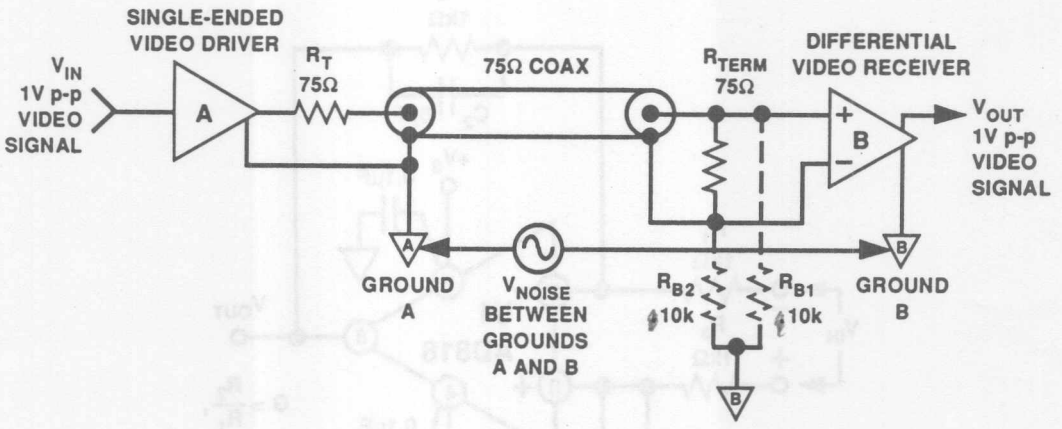


Figure 11.27

The noise between driver and receiver grounds is rejected by the CMRR of the differential video receiver. The coaxial line is terminated in its characteristic impedance at the receiver. Because neither end of the termination is connected directly to ground B, both inputs of receiver B see essentially the same common mode voltage, V_{NOISE}, which is rejected in proportion to B's CMRR. A

typical CMRR goal is 70dB or better for frequencies up to 10MHz. Return resistors, R_{B1} and R_{B2} may be needed to keep I_{bias} from developing excessive common-mode voltage across the amplifier inputs.

A low cost, medium-performance video line receiver, using a high speed op amp in a standard 4-resistor bridge instrumentation amplifier is shown in Figure 11.28. It is implemented using the AD818 op amp and low-resistance ac-trimmed resistors. Resistor matching is critical to good CMRR, so for highest noise rejection, a single-substrate dual-matched-pair thin-film network should be used. Matching of the ratios R1/R2 and R3/R4, to 1% gives a low-frequency CMRR of about 46dB. Above 1MHz, the bridge balance is dominated by ac effects, and C1 - C2 capacitive balance should be trimmed for best performance - a match that is essential for achieving CMRR above 40dB at high frequencies. This circuit, with its two 1kΩ input resistors, does load a 75Ω video line somewhat, and this loading should be taken into account.

SIMPLE VIDEO LINE RECEIVER USING THE AD818 OP AMP

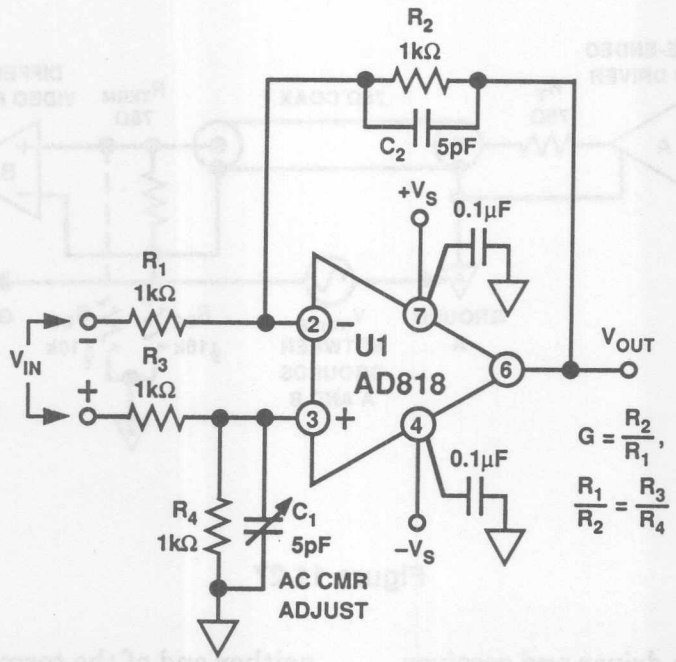


Figure 11.28

VIDEO LINE RECEIVERS USING THE AD830 ACTIVE FEEDBACK AMPLIFIER TOPOLOGY

Walt Kester

Full integration of the video line receiver eliminates the drawbacks of the simple line receiver approach and improves both performance and circuit flexibility. The AD830, shown in the circuit of Figure 11.29, is a two-input IC "active feedback amplifier" designed for this function. The signal from system "A" is received differentially by the AD830 and is reproduced relative to the ground in system "B". Common mode noise is rejected by the excellent CMRR of the AD830 (50dB at 10MHz). Key specifications for the AD830 are shown in Figure 11.30. CMRR and frequency response for the AD830 are shown in Figure 11.31.

DIFFERENTIAL LINE RECEIVER USING THE AD830

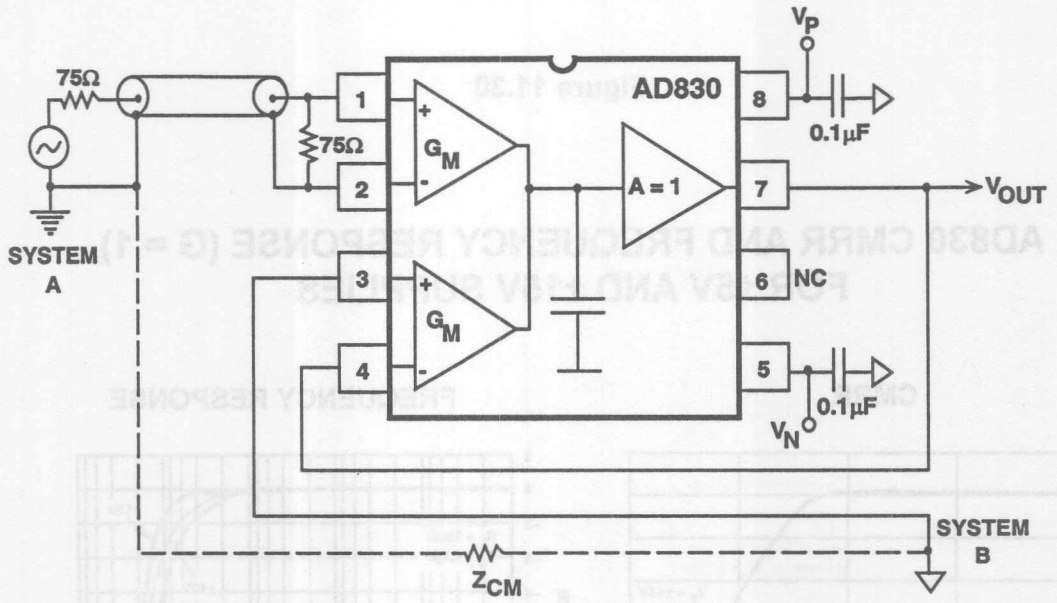


Figure 11.29

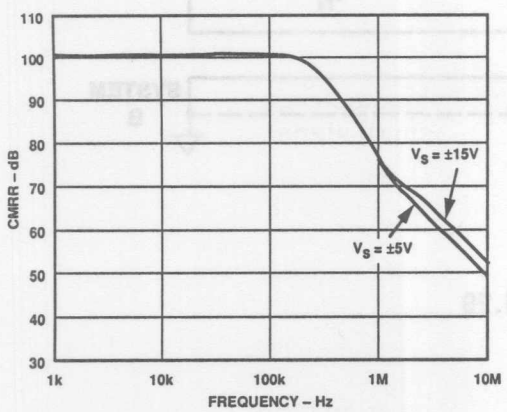
AD830 ACTIVE FEEDBACK VIDEO DIFFERENCE AMPLIFIER KEY SPECIFICATIONS

- Common Mode Voltage Range: ±11.5V
- Differential Voltage Range: ±2V
- CMRR: 60dB @ 4.43MHz, 50dB @ 10MHz
- Bandwidth: 50Mhz
- Distortion: -60dBc @ 4.43Mhz
- Differential Gain: 0.1%, Differential Phase: 0.1°

Figure 11.30

AD830 CMRR AND FREQUENCY RESPONSE (G = 1) FOR ±5V AND ±15V SUPPLIES

CMRR



FREQUENCY RESPONSE

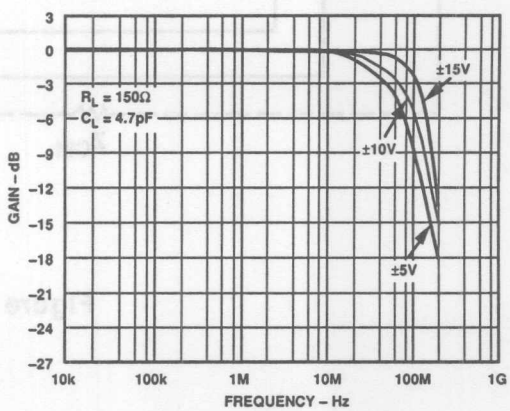


Figure 11.31

The AD830 represents Analog Devices' first amplifier product to embody a powerful new amplifier topology. Referred to as active feedback, the topology used in the AD830 provides inherent advantages in the handling of differential signals, differing system grounds, level shifting and low distortion, high frequency amplification. In addition, it makes possible the implementation of many functions not realizable with single op amp circuits and is often superior to op amp based equivalent circuits. For instance, you can use the AD830 to add or subtract two video signals with no external resistors.

BASIC TOPOLOGY OF THE AD830 ACTIVE FEEDBACK AMPLIFIER

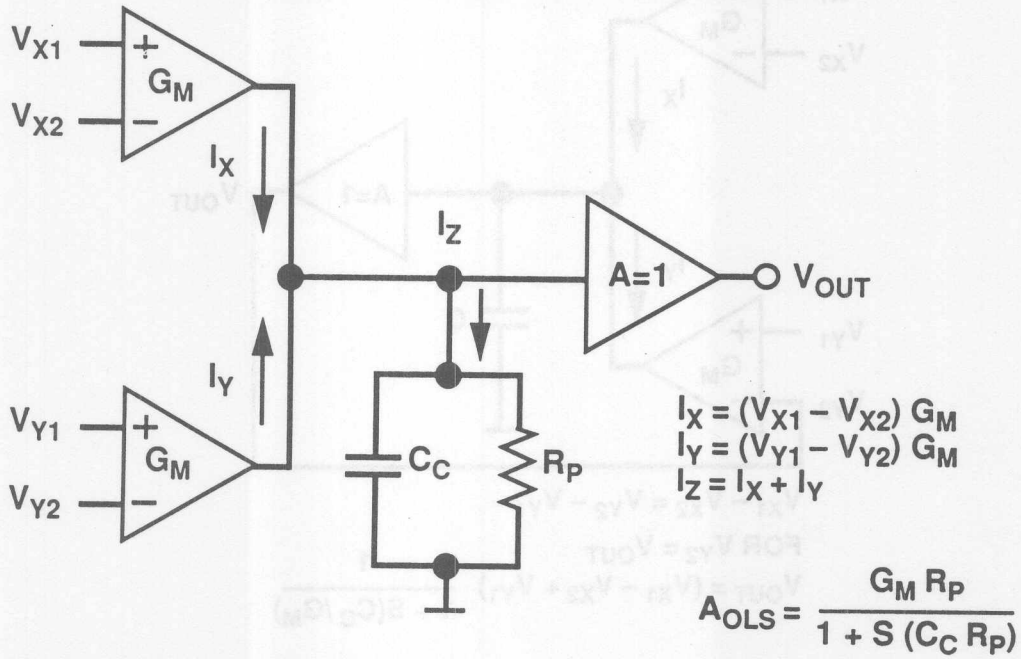
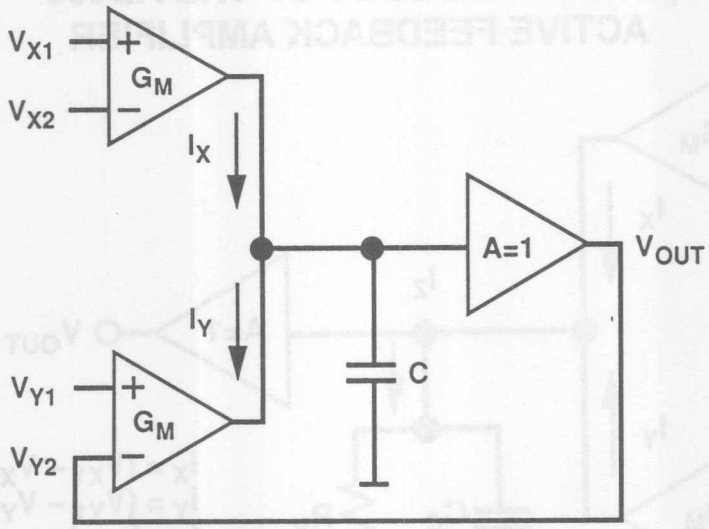


Figure 11.32

The AD830 topology, reduced to its elemental form, is shown in Figure 11.32. Nonideal effects such as nonlinearity, bias currents and limited input range are omitted from this model for simplicity. The key feature of this topology is the use of two, identical voltage-to-current converters, G_M, that make up input and feedback signal interfaces. They are labeled with inputs V_X and V_Y, respectively. These voltage to current converters inputs are fully differential; with high linearity, high input impedance, and wide common mode, small signal voltage range operation. The device can handle ±1V differential input signals in the linear mode. The inputs provide common-mode rejection, low distortion, and negligible loading on the source. The label, G_M, is meant to convey that the transconductance is a large signal quantity, unlike in the front end of most op amps. The two G_M stage current outputs I_X and I_Y, sum together at the high impedance node which is characterized by an equivalent

resistance and capacitance connected to an "ac" ground. A unity voltage gain stage follows the high impedance node to provide buffering from loads. Relative to either input, the open loop gain, A_{OL}, is set by the transconductance, G_M, working into the resistance, R_P, $A_{OL} = G_M \times R_P$. The unity gain frequency ω_{odB} for the open loop gain is established by the transconductance, G_M, working into the capacitance, C_C; $\omega_{odB} = G_M/C_C$.

CLOSED LOOP CONNECTION FOR THE BASIC AD830 TOPOLOGY



$$V_{X1} - V_{X2} = V_{Y2} - V_{Y1}$$

FOR $V_{Y2} = V_{OUT}$

$$V_{OUT} = (V_{X1} - V_{X2} + V_{Y1}) \frac{1}{1 + S(C_C/G_M)}$$

Figure 11.33

Precise amplification is accomplished through closed loop operation of the topology as shown in Figure 11.33. Voltage feedback is implemented via the Y G_M stage where the output is connected to the –Y input for negative feedback. An input signal is applied across the X G_M stage, either fully differentially or single-ended referred to common. It produces a current signal which is summed at the high impedance node with the output current from the Y G_M stage. Negative feedback nulls this sum to a small error current necessary to develop the output voltage at the high impedance node. the error current is usually negligible, so the null condition essentially forces the Y G_M output stage current to exactly equal the X G_M output current. Since the two transconductances are identical, the differential voltage across the Y inputs equals the negative of the differential voltage across the X input; $V_Y = -V_X$ or more precisely, $V_{Y2} - V_{Y1} = V_{X1} - V_{X2}$. This simple relationship provides the

basis to analyze any function possible with the AD830, including any feedback situation.

The bandwidth of the circuit is defined by the G_M and the capacitor C_C. The highly linear G_M stages give the amplifier a single pole response, excluding the output amplifier and loading effects. The bandwidth and general dynamic behavior is symmetrical (identical) for the noninverting and the inverting connections of the AD830. In addition, the input impedance and CMRR are the same for either connection. This is very advantageous and unlike the situation with a voltage or current feedback amplifier, where there is a distinct difference in performance between the inverting and noninverting gain stages. The practical importance of this cannot be overemphasized and is a key feature offered by the AD830 active feedback topology.

The AD830 is a flexible device which may be used in a number of configurations with excellent video performance. Figure 11.34 shows how the AD830 may be configured to provide instrumentation amplifier style amplification. The input signal is connected differentially to the internal V-to-I converter #1. The gain is set via the feedback resistors R2 and R1 in the same manner as a noninverting op amp circuit. The polarity of the gain is established by the relative connections at input pins 1 and 2. Inverting gain is set by reversing the connections to the input. As in a conventional voltage feedback op amp, the bandwidth decreases with increasing gain.

GAIN-OF-N INSTRUMENTATION AMPLIFIER USING THE AD830

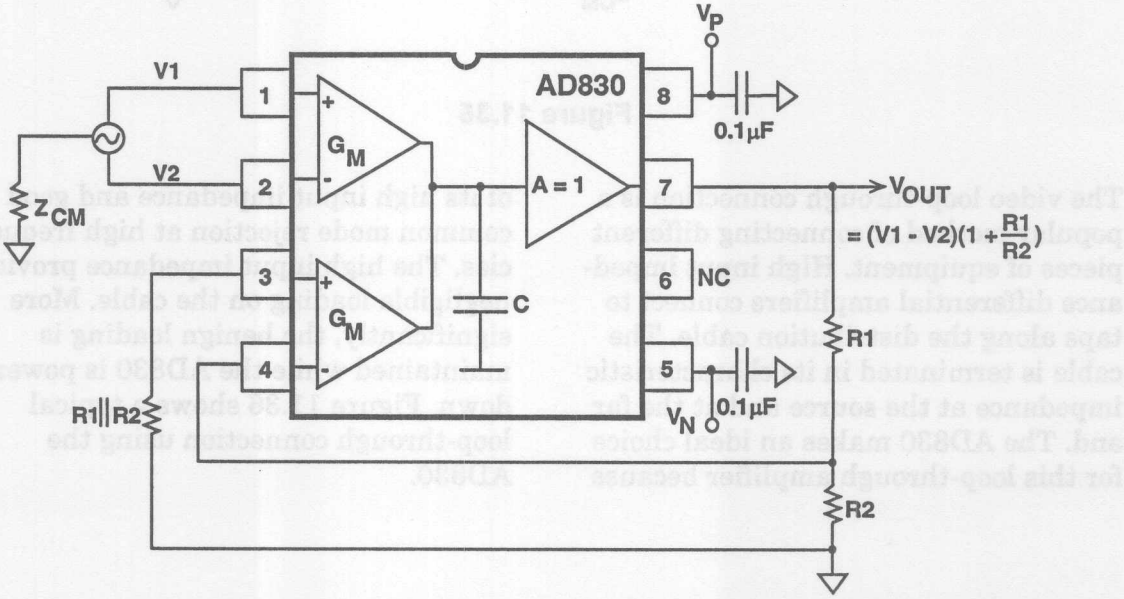


Figure 11.34

The video cable receiver/driver circuit shown in Figure 11.35 not only provides ground noise rejection, but also supplies a gain-of-two so that the AD830 output can drive a source and load terminated 75Ω cable without signal attenuation. The 499Ω resistors set the gain at 2, and the 249Ω resistor between pin 3 and ground cancels the offset due to the input bias currents.

VIDEO CABLE RECEIVER/DRIVER USING THE AD830

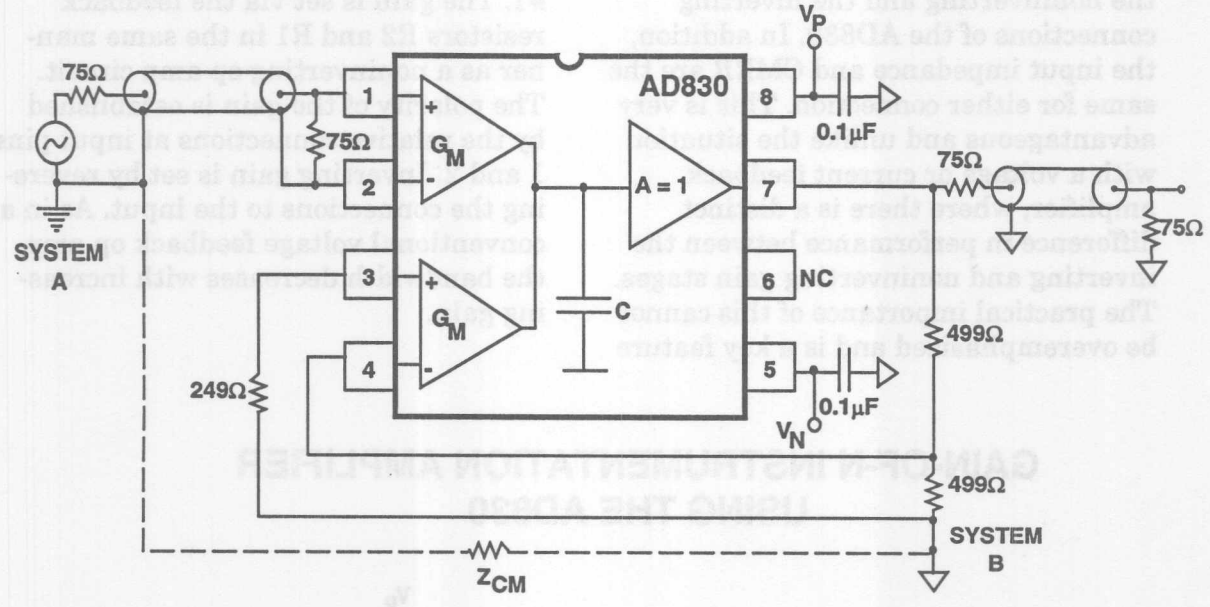


Figure 11.35

The video loop-through connection is a popular method of connecting different pieces of equipment. High input impedance differential amplifiers connect to taps along the distribution cable. The cable is terminated in its characteristic impedance at the source and at the far end. The AD830 makes an ideal choice for this loop-through amplifier because of its high input impedance and good common mode rejection at high frequencies. The high input impedance provides negligible loading on the cable. More significantly, the benign loading is maintained while the AD830 is powered down. Figure 11.36 shows a typical loop-through connection using the AD830.

VIDEO LOOP-THROUGH CONNECTION USING THE AD830

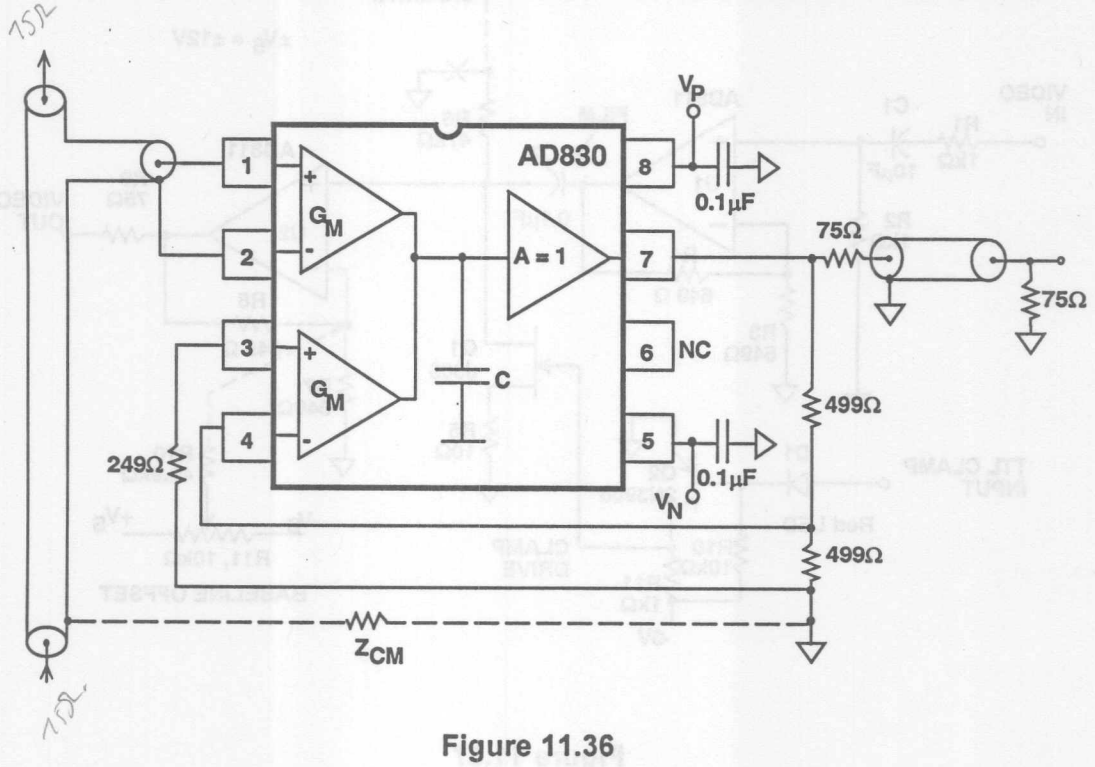


Figure 11.36

A COMPOSITE VIDEO SYNC TIP DC RESTORER

Walt Jung, Dave Whitney

A common video signal processing requirement is DC restoration, or clamping. When used with a composite NTSC video signal, sync tip clamping is commonly used. This fixes the most negative excursion of the signal to a fixed DC level, which is usually ground. With a constant input signal level, note that this operation also fixes the remainder of the signal with respect to ground. The circuit of Figure 11.37 is an example of a sync tip clamper, using 2 op amps and a pair of discrete transistors. With a standard NTSC composite video signal at the input, the circuit restores the signal to a ground reference, and makes the DC restored and buffered version available at the output, source terminated by 75Ω. This circuit is especially useful in driving an ADC, since ac coupling into the ADC requires additional range overhead and a corresponding loss of effective resolution.

SYNC TIP DC RESTORER

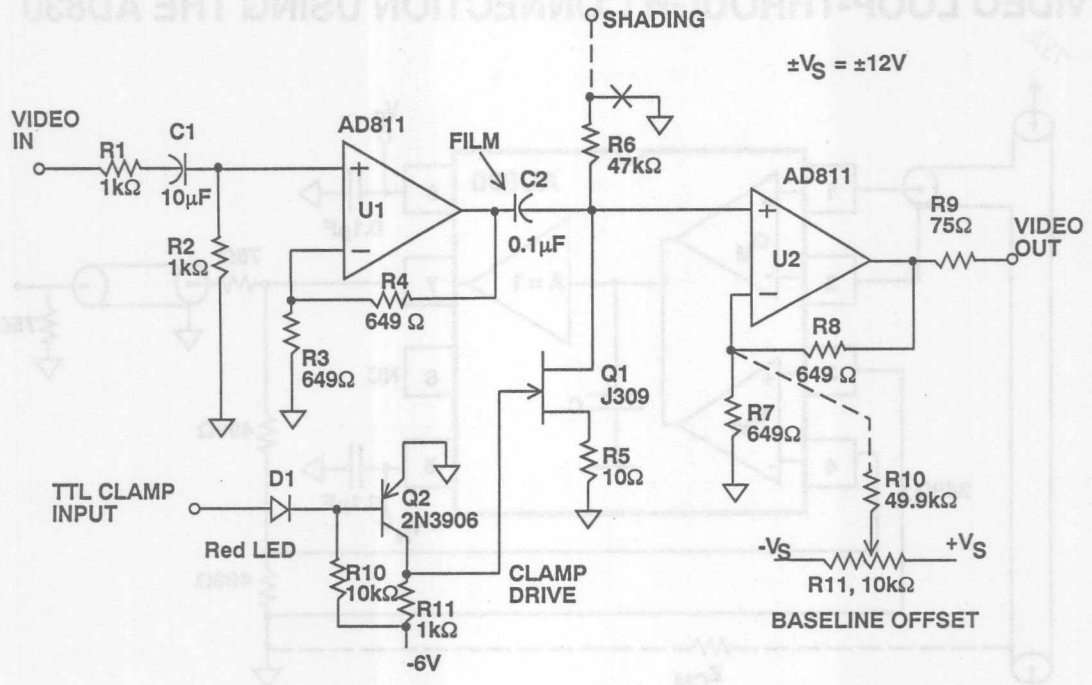


Figure 11.37

In operation, the U1 stage functions as an input line isolator and buffer. The signal at the input is divided by a factor of 2 by R_1 and R_2, and is AC coupled into U1. U1 is an AD811 configured as a wideband noninverting gain-of-two amplifier, by virtue of the R_4-R_3 ratio. With the values shown for R_4-R_3 and the use of ±10V (or more) DC supplies, the 0.1dB bandwidth will be more than 30MHz.

The output of U1 drives Q1, a shunt JFET switch through a film coupling cap, C_2. The N channel JFET is a low capacitance, high transconductance unit, chosen for 50Ω or less of on-resistance. The low capacitance allows it to be easily driven from U1, minimizing potential distortion of the signal. The low on-resistance of Q1 and high output current of the AD811 driver stage allows very fast charging of capacitor C_2 between sync tips, at a rate that will be limited to $I_{max(U1)}/C_2$ V/s. With a ±100mA output from the AD811 and a 0.1µF value for C_2, this allows maximum charging rates on the order of ±1 V/µs, applicable during the interval when switch Q1 is on (the clamp sample period). If this period is for example a 0.1µs time, then the circuit can correct ±100mV of baseline change for each clamp sample.

Since the overall video signal is on the order of 1Vp-p and corrections tend to be longer term, these design limits are conservative in practice. For example, for an interfering 60 Hz hum of 1 volt peak, the clamp circuit will see a maximum rate of change or slew rate of $SR = f \cdot 2\pi \cdot Vpeak$.

For 60Hz and 1V, the rate of change is 376.80V/s. In an NTSC 63.5µs line interval, the maximum change of this

hum signal is 376.80·63.5e-6 = 0.024V, which is correctable.

The clamp sample period drive signal is derived elsewhere, and is presented to this circuit as a TTL signal at D1-Q2. This signal is an active low TTL logic signal, and is timed to occur during the video waveform negative sync tips. The low state signal drives both Q2 and Q1 on, effectively connecting C_2 to ground through Q1-R_5, and so provides the DC reference path to ground described above.

During the remaining time period of a video line time, the switch Q1 is off due to the -6V bias from R_{11}. The bias current of U2 is the main DC load on the C_2-R_6 voltage node during this time, which will tend to ramp ±, slowly charging C_2 with the bias current of U2. Since this current could be as high as 5μA, the baseline ramp error in 50μs time could be (5e-6/0.10e-6)×50e-6 volts, or 2.5mV. However, this is not likely to be a problem, as the typical AD811 bias current is lower, and the video signal is appreciably larger in amplitude.

On the other hand, if an intentional ramp up or down waveform is desired, R_6 can optionally be returned to a variable DC voltage to achieve this effect (by breaking the ground at "X"). This will produce a horizontal shading (a black-to- white or white-to-black background).

Another option possible with the circuit is to introduce a variable DC baseline to the clamped signal, for example to provide a specific bias point for a following stage. The optional bias network consisting of resistor R_{10} and R_{11} can provide this function. The variable DC voltage from R_{11} injects a current through R_{10} which is added in voltage form at the output of U2, effectively allowing signal baseline offset of ±150mV about the DC clamping potential (which otherwise is ground). Note that if this feature is used, the value of R_7 may require some adjustment for exact gain, and that DC voltages ±Vs should be clean.

The output stage U2 is a second wideband AD811, configured as a 75Ω line driver. U2 presents the DC restored video signal to the output, with a level equal to the original input signal.

A VIDEO SYNC STRIPPER CIRCUIT
Walt Jung, Dave Whitney

Another common video signal processing requirement is the function of sync stripping. In a sync stripper, horizontal and vertical timing information is removed from the composite NTSC video signal and converted to logic levels for further processing. The circuit of Figure 11.38 is a self-contained sync stripper, using an AD811 op amp and a pair of discrete transistors. It is driven from an NTSC composite video signal and delivers TTL compatible positive going sync at the output.

SYNC STRIPPER GENERATES COMPOSITE SYNC

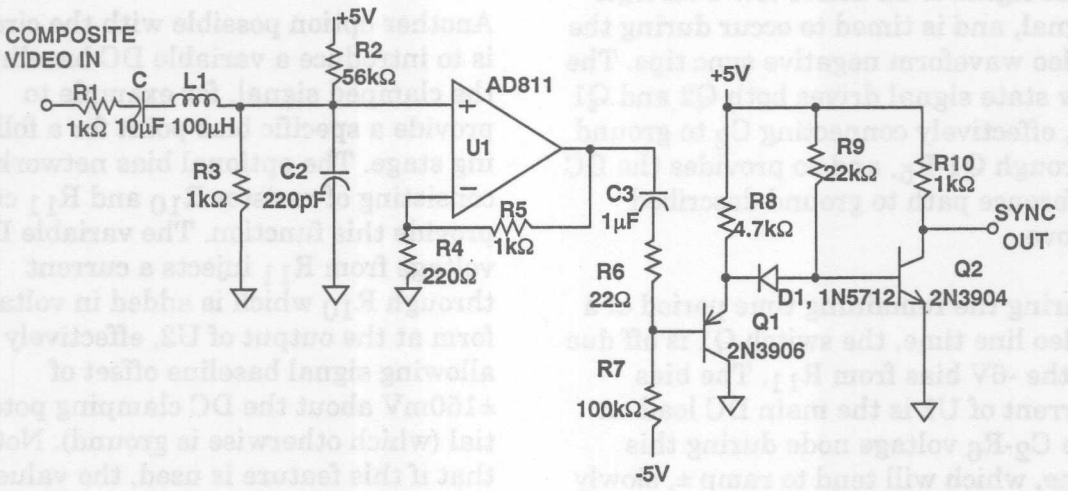


Figure 11.38

In this circuit the U1 stage performs three functions. First, components L_1-C_2 act as a low pass filter, removing the 3.58MHz chrominance components. U1, an AD811, also is an isolator with gain as well as a buffer to drive the following stage, which is a low input impedance sync tip clamp. The input signal is divided by a nominal factor of 2 by R_1 and R_2-R_3, and AC coupled to the input of U1. U1 is configured as a wideband times 6 amplifier, by the R_5-R_4 ratio. This yields an overall luminance signal gain of three times, from the input to C_3. With the gain values shown and ±5V (or more) DC supplies for U1, the stage can handle normal video signals without clipping at the output.

U1's output drives Q1, a PNP shunt clamp in an unusual configuration. In steady-state DC terms, Q1 is held in saturation by the bias current from R_7, where the emitter is close to ground. Since the AC signal driving Q1 through C_3 is a composite video signal with the sync tips the most negative limit, on a dynamic basis Q1 acts as a DC restorer. The negative going video waveform sync tips drive Q1 into hard saturation, and the more positive parts of the waveform bring it out of saturation, where it acts as a linear emitter follower. This action produces a DC restored composite video signal at the emitter of Q1, with the sync tips referred to ground.

The output of Q1 is coupled to the base of NPN switch Q2, through Schottky diode D1. The combination of this diode's forward drop and the V_{BE} of Q2 produce a switching threshold at the base of Q2 which, with consideration of

the signal levels, causes Q2 to switch on/off cleanly at about the sync tip 50% amplitude point.

The output from Q2 consists of clean, noise-free sync timing information, positive going during sync tips. This signal is TTL compatible, by virtue of the +5V supply to Q2 as shown. Practical hints in getting the most from this circuit involve some attention to good decoupling of the U1 stage. The high instantaneous currents during the sync tips can generate power supply and/or ground noise. Local bypassing of U1 with large capacitors to the logic supply ground will help to control this, as will a compact layout and the use of a ground plane.

MAINTAINING TRANSMISSION LINE IMPEDANCES ON THE PC BOARD
Walt Kester

In the previous section, we discussed methods for transmitting high speed signals across interfaces. It is equally important to maintain signal fidelity at the receiving end of the transmission line. In most applications, the actual termination point of the transmission line is on another PC board.

In some cases, it may be possible to bring the high speed analog signal into the PC board through an edge connector. The ground plane of the PC board should be connected to at least 20-30% of the connector pins. The analog signal(s) should be separated from other signals by ground pins.

EDGE CONNECTORS

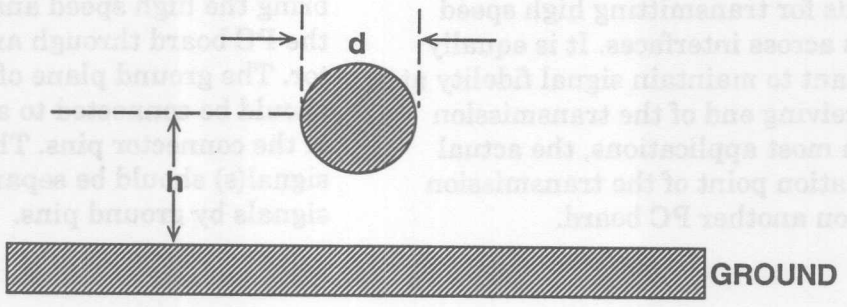
- Separate Sensitive Signals by Ground Pins
- Keep the Ground Impedance Low with Multiple (20-30% of total) Ground Pins
- Have Several Pins for Each Power Line
- Critical Signals May Require a Separate Connector, Possibly Coaxial (BNC, SMA, SMB, SMC)

Figure 11.39

A much better solution is to bring the sensitive analog signal into the PC board via a separate coaxial cable connector. The most popular are the BNC types and the subminiature SMA, SMB, or SMC types. The smaller miniature types offer direct microstrip-to-coaxial interconnects with minimal impedance mismatch. Once the signal is on the PC board, it is a relatively simple matter to match the cable impedance.

Figure 11.40 shows the typical wire-over-ground plane line often used in prototypes. The characteristic impedance of this line is approximately 120Ω, but this may vary by as much as 40% depending upon the actual placement of the wire.

WIRE OVER GROUND PLANE IS USEFUL FOR PROTOTYPES



- $Z_O = \frac{60}{\sqrt{e_r}} \ln\left[\frac{4h}{d}\right]$ ohms
- = 120 ohms ±40%

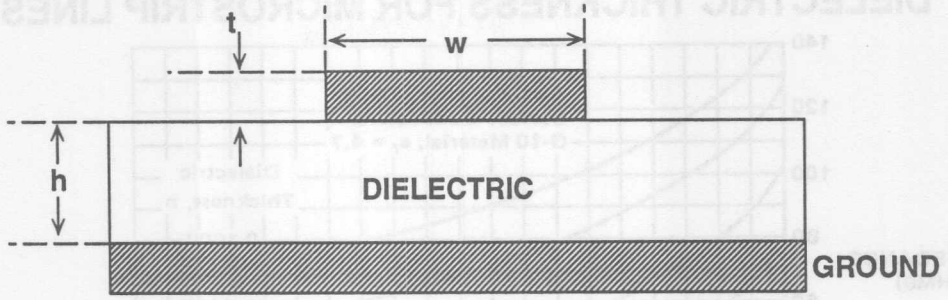
Assume 22 Gauge Teflon Insulated Wire
$e_r = 2$, $d = 0.024"$, $h = 0.1"$

Figure 11.40

Microstrip techniques are easily implemented on a double-sided PC board, where one side of the board is dedicated primarily to ground plane, and the other side to the signal interconnects. The characteristics of typical microstrip lines are given in Figures 11.41, 11.42, 11.43, and 11.44.

In multilayer PC boards, strip line transmission line techniques are required as shown in Figure 11.45. The characteristics of typical strip lines are given in Figures 11.46 and 11.47. It is critically important that if a microstrip line is implemented on a PC board that there is no break in the ground plane underneath the line. Any break renders the whole exercise useless.

MICROSTRIP TRANSMISSION LINE FOR DOUBLE-SIDED PC BOARD

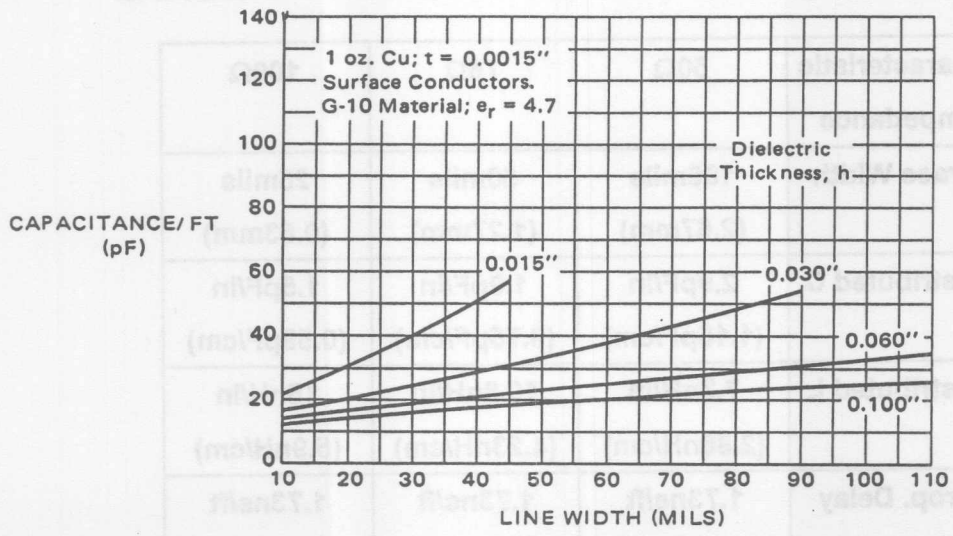


- $Z_O = \frac{87}{\sqrt{e_r + 1.41}} \ln \left[\frac{5.98h}{0.8w + t} \right]$
- $t_{pd} = 1.017\sqrt{0.475e_r + 0.67}$ ns/ft
- $t_{pd} = 1.73$ns/ft for $e_r = 4.7$

Figure 11.41

11

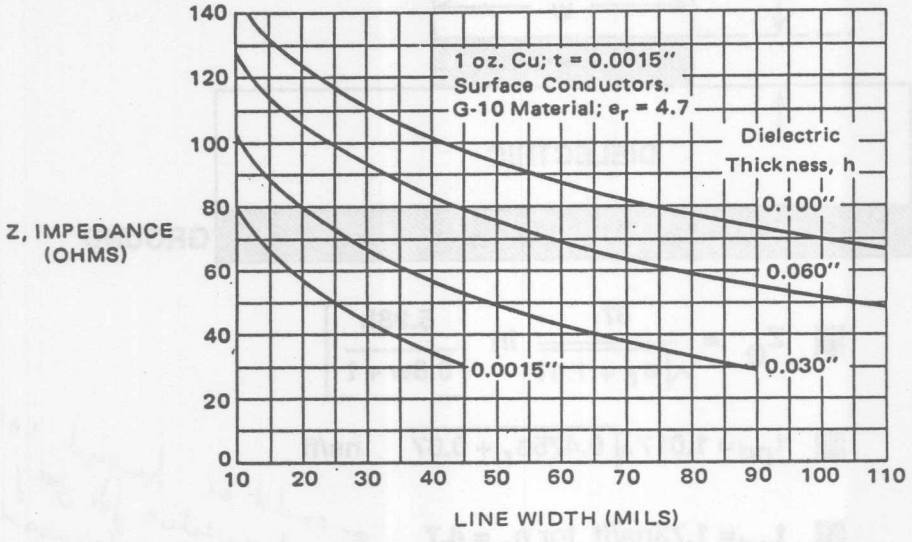
CAPACITANCE VERSUS LINE WIDTH AND DIELECTRIC THICKNESS FOR MICROSTRIP LINES



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Figure 11.42

IMPEDANCE VERSUS LINE WIDTH AND DIELECTRIC THICKNESS FOR MICROSTRIP LINES



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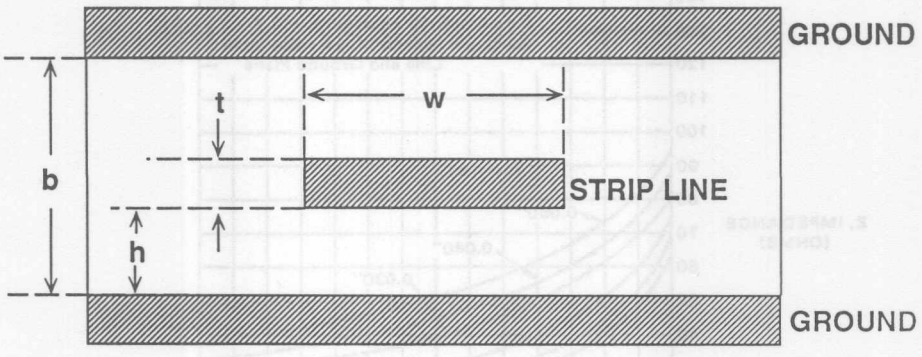
Figure 11.43

CHARACTERISTICS OF 1 OUNCE COPPER MICROSTRIP LINES ON 0.060 INCH THICK G-10 EPOXY PC BOARD

Characteristic Impedance	50Ω	75Ω	100Ω
Trace Width	105mils (2.67mm)	50mils (1.27mm)	25mils (0.63mm)
Distributed C	2.9pF/in (1.15pF/cm)	1.9pF/in (0.75pF/cm)	1.5pF/in (0.59pF/cm)
Distributed L	7.3nH/in (2.86nH/cm)	10.8nH/in (4.23nH/cm)	15nH/in (5.9nH/cm)
Prop. Delay	1.73ns/ft 0.144ns/in (0.057ns/cm)	1.73ns/ft 0.144ns/in (0.057ns/cm)	1.73ns/ft 0.144ns/in (0.057ns/cm)

Figure 11.44

STRIP LINE TRANSMISSION LINE FOR MULTILAYER PC BOARD

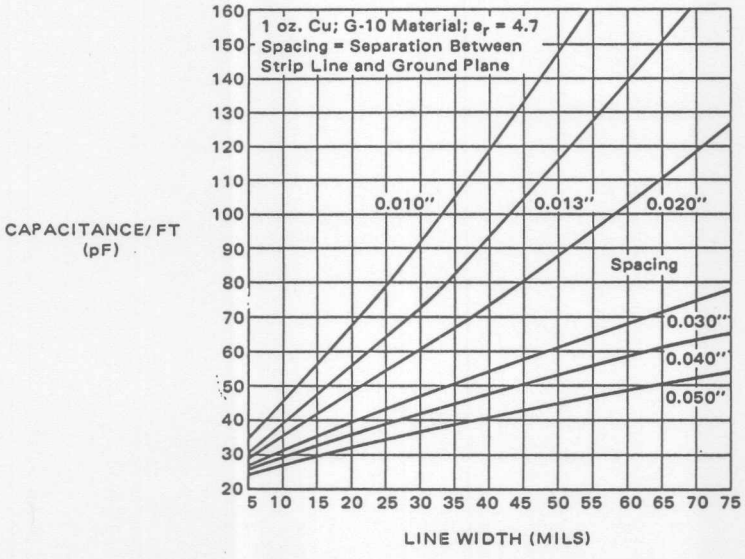


- $Z_O = \frac{60}{\sqrt{e_r}} \ln \left[\frac{4b}{0.67\pi w \left(0.8 + \frac{t}{w} \right)} \right]$
- $t_{pd} = 1.017\sqrt{e_r}$ ns/ft
- $t_{pd} = 2.2$ns/ft for $e_r = 4.7$

Figure 11.45

11

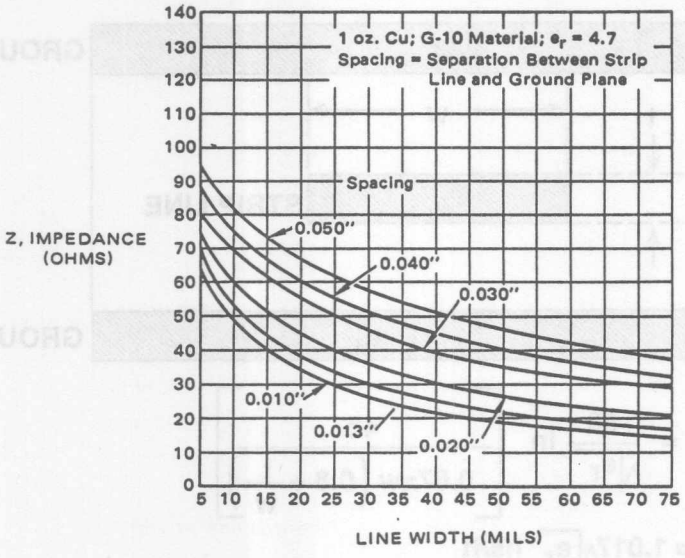
CAPACITANCE VERSUS LINE WIDTH AND SPACING FOR STRIP LINES



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Figure 11.46

IMPEDANCE VERSUS LINE WIDTH AND SPACING FOR STRIP LINES



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Figure 11.47

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10. **High Speed Design Seminar Notes**, 1990, Analog Devices.

SECTION 12

SELECTING THE RIGHT HIGH SPEED ADC

- DISCRETE TIME SAMPLING OF ANALOG SIGNALS
- PROPERLY SPECIFYING THE ADC SAMPLING RATE AND THE ANTIALIASING FILTER
- PROPERLY SPECIFYING THE ADC RESOLUTION AND DYNAMIC RANGE REQUIREMENTS
- HIGH SPEED FLASH CONVERTERS AND ERROR SOURCES
- HIGH SPEED SUBRANGING ADCS AND ERROR SOURCES
- APERTURE DELAY TIME (OR EFFECTIVE APERTURE DELAY TIME)
- ERRORS DUE TO APERTURE JITTER
- TRANSIENT RESPONSE OR SETTLING TIME
- OVERVOLTAGE RECOVERY TIME
- METASTABILITY AND BIT ERROR RATES IN ADCS

SECTION 12

SELECTING THE RIGHT HIGH SPEED ADC

Walt Kester

Determining the ADC requirement in a signal processing system is often a challenge which involves many tradeoffs. We have discussed high speed signal amplification and transmission in detail and explored many of the various options available. When selecting the ADC, you must continue to keep the goal of preserving signal fidelity and dynamic range in mind, while resisting the temptation to overspecify.

Overspecifying the ADC, its antialiasing filter, and other peripheral circuitry is especially dangerous, because it may result in high cost and even unrealizable component requirements. In order to intelligently specify the ADC portion of the system, you must first understand the fundamental concepts of sampling and quantization and their effects on the signal.

KEY ELEMENTS OF A BASEBAND SAMPLED DATA SYSTEM

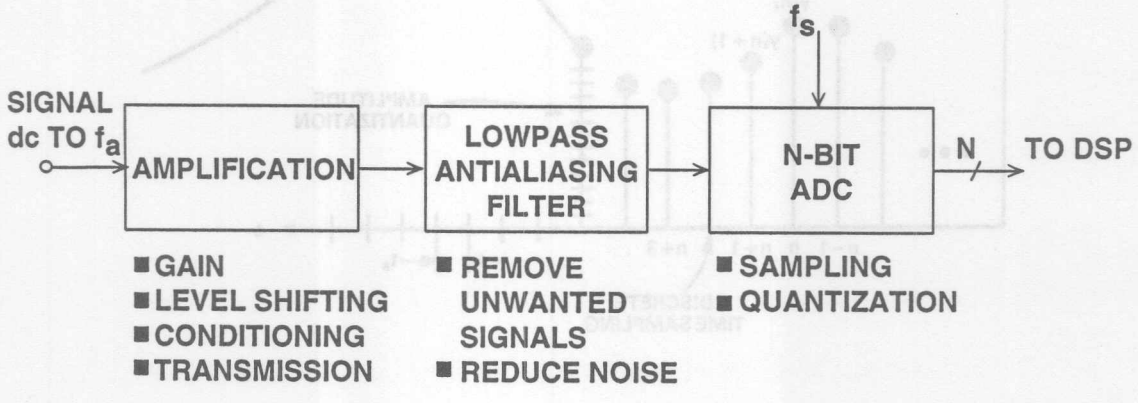


Figure 12.1

In this section, we will consider the traditional problem of sampling and quantizing a baseband signal whose bandwidth lies between dc and an upper frequency of interest, f_a. This is often referred to as *Nyquist, or Sub-Nyquist Sampling*. The topic of *Super-Nyquist* sampling (sometimes called *undersampling*) where the signal of interest falls outside of the Nyquist bandwidth (dc to $f_S/2$) is treated in Section 15.

DISCRETE TIME SAMPLING OF ANALOG SIGNALS

The concept of discrete time and amplitude sampling of an analog signal is shown in Figure 12.2. The continuous analog data must be sampled at discrete intervals, t_S, which must be carefully chosen to insure an accurate representation of the original analog signal. It is clear that the more samples taken (faster sampling rates), the more accurate the digital representation, but if fewer samples are taken (lower sampling rates), a point is reached where critical information about the signal is actually lost. This leads us to the statement of Shannon's Information Theorem and Nyquist's Criteria given in Figure 12.3.

DISCRETE SAMPLING OF AN ANALOG SIGNAL

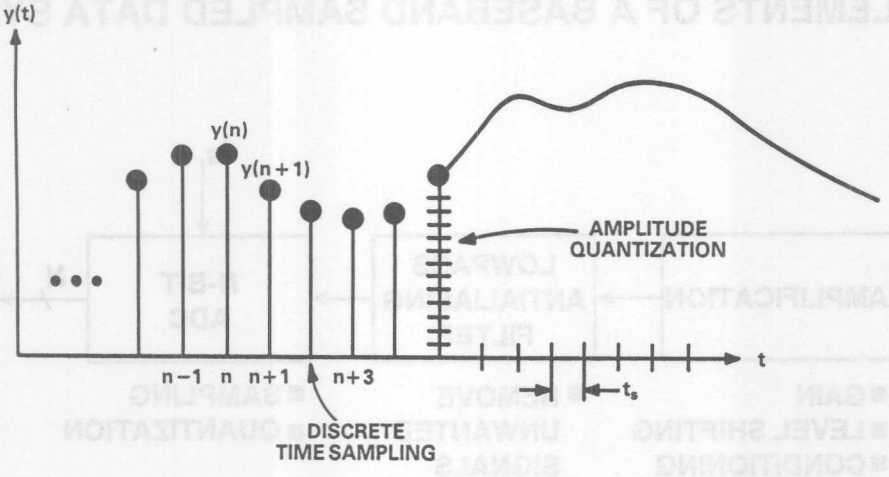


Figure 12.2

SHANNON'S INFORMATION THEOREM AND NYQUIST'S CRITERIA

- **Shannon:**

  An Analog Signal with a *Bandwidth* of f_a Must be Sampled at a Rate $f_s > 2f_a$ in Order to Avoid the Loss of Information.

- **Nyquist:**

  If $f_s < 2f_a$, then a Phenomena Called *Aliasing* Will Occur

Figure 12.3

In order to understand the implications of *aliasing* in both the time and frequency domain, first consider the four cases of a time domain representation of a sampled sinewave signal shown in Figure 12.4. In the Case 1, it is clear that an adequate number of samples have been taken to preserve the information about the sinewave. In Case 2 of the figure, only four samples per cycle are taken; still an adequate number to preserve the information. Case 3 represents the ambiguous limiting condition where $f_s = 2f_a$. If the relationship between the sampling points and the sinewave were such that the sinewave was being sampled at precisely the zero crossings (rather than at the peaks, as shown in the illustration), then all information regarding the sinewave would be lost. Case 4 of Figure 12.4 represents the situation where $f_s < 2f_a$, and the information obtained from the samples indicates a sinewave having a frequency which is lower than $f_s/2$, i.e. the out-of -band signal is *aliased* into the Nyquist bandwidth between dc and $f_s/2$. As the sampling rate is further decreased, and the analog input frequency f_a approaches the sampling frequency f_s, the aliased signal approaches dc in the frequency spectrum.

TIME DOMAIN EFFECTS OF ALIASING

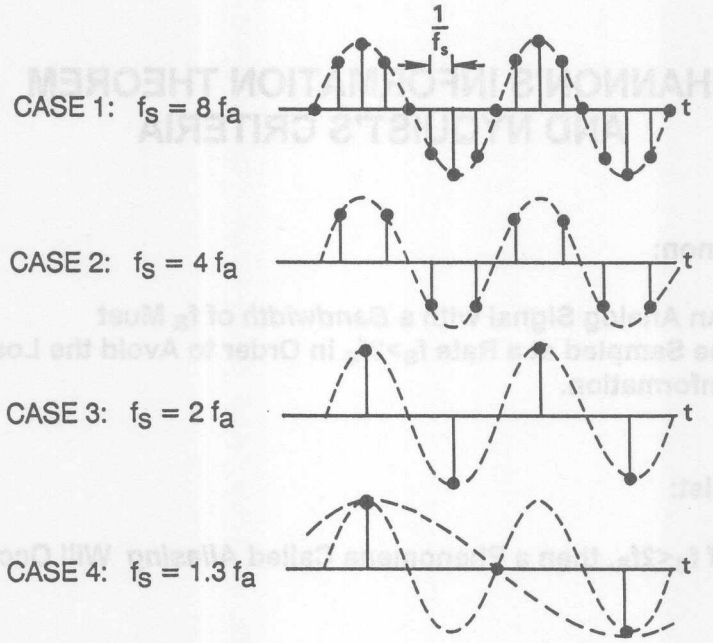


Figure 12.4

The corresponding frequency domain representation of the above scenario is shown in Figure 12.5. Note that sampling the analog signal f_a at a sampling rate f_s actually produces two alias frequency components, one at f_s+f_a, and the other at f_s-f_a. The upper alias, f_s+f_a, seldom presents a problem, since it lies outside the Nyquist bandwidth. It is the lower alias component, f_s-f_a, which causes problems when the input signal exceeds the Nyquist bandwidth, $f_s/2$.

From Figure 12.5, we make the important observation that *regardless* of where the analog signal being sampled happens to lie in the frequency spectrum, the effects of sampling will cause either the actual signal or an aliased component to fall within the Nyquist bandwidth between dc and $f_s/2$. Therefore, any signals which fall outside the bandwidth of interest, whether they be spurious tones or random noise, must be adequately filtered *before* sampling. If unfiltered, the sampling process will alias them back within the Nyquist bandwidth where they will corrupt the signals of interest.

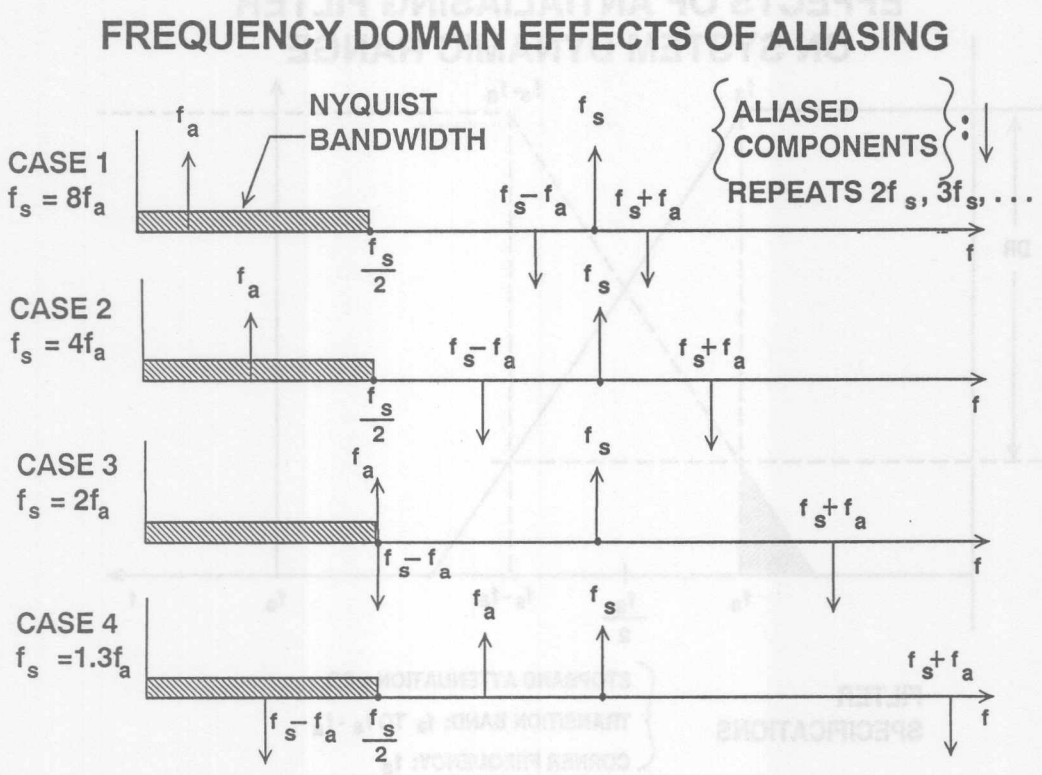


Figure 12.5

PROPERLY SPECIFYING THE ADC SAMPLING RATE AND THE ANTIALIASING FILTER

Properly specifying the ADC sampling rate basically involves trading off higher ADC sampling rates against increased antialiasing filter complexity. The first step is to know the characteristics of the signal being processed. Assume that the highest frequency of interest is f_a. The antialiasing filter passes signals from dc to f_a while attenuating signals above f_a. We have now reached the first decision point, since there is no such thing as a perfect analog lowpass filter.

Assume that the corner frequency of the filter is chosen to be equal to f_a. The effect of the finite transition from minimum to maximum attenuation on system dynamic range is illustrated in Figure 12.6.

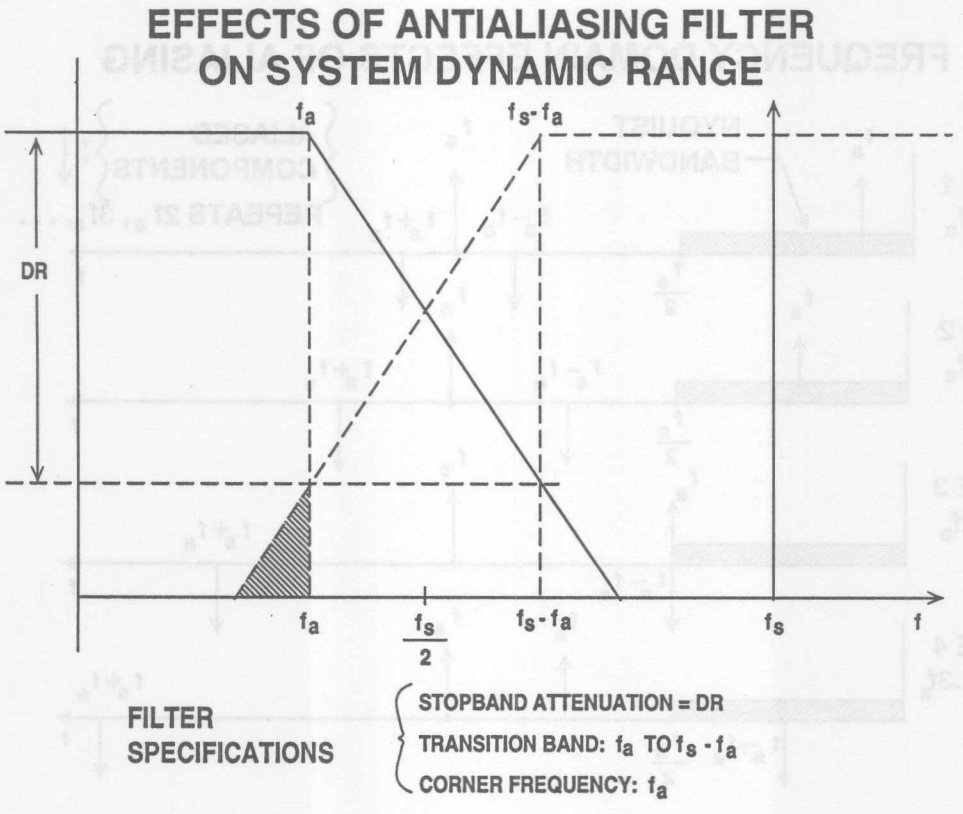


Figure 12.6

Assume that the input signal has fullscale components well above the maximum frequency of interest, f_a. The diagram shows how fullscale frequency components above $f_s - f_a$ are aliased back into the bandwidth dc to f_a. These aliased components are indistinguishable from actual signals and therefore limit the dynamic range to the value on the diagram which is shown as *DR*.

Some texts recommend specifying the antialiasing filter with respect to the Nyquist frequency, $f_s/2$, but this assumes that the signal bandwidth of interest extends from dc to $f_s/2$ which is rarely the case. In the example shown in Figure 12.6, the aliased components between f_a and $f_s/2$ are not of interest and do not limit the dynamic range.

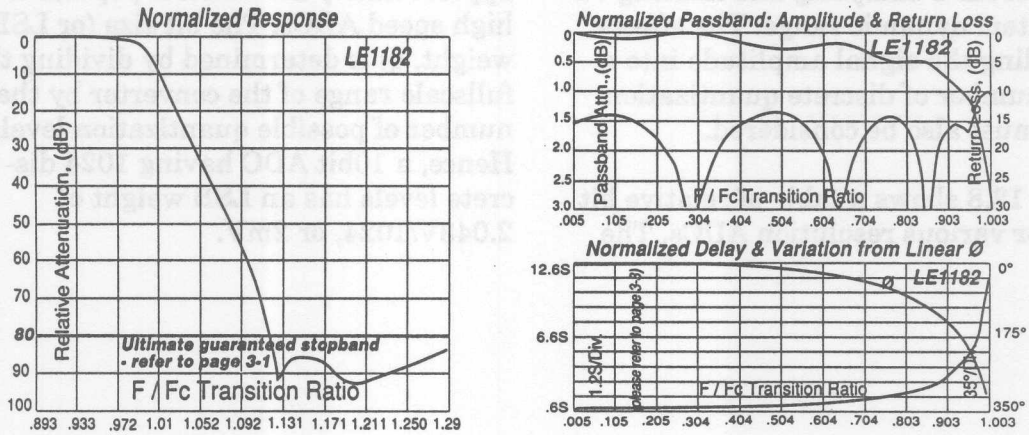
The antialiasing filter transition band is therefore determined by the corner frequency f_a, the stopband frequency $f_s - f_a$, and the stopband attenuation, DR. We choose the required system dynamic range based on our requirement for signal fidelity.

Filters become more complex as the transition band becomes sharper, all other things being equal. For instance, a Butterworth filter design gives 6dB attenuation per octave for each filter pole. Achieving 60dB attenuation in a transition region between 1MHz and 2MHz (1 octave) requires a minimum of 10 poles.

Other filter designs are generally more suited to high speed applications where the requirement for a sharp transition band is combined with requirements on in-band flatness and linear phase response. Elliptic filters are popular choices for high speed antialiasing filters.

There are a number of companies which specialize in designing custom analog filters. As an example, the normalized response of the TTE, Inc., LE1182 11-pole elliptic antialiasing filter is shown in Figure 12.7. Notice that this filter is specified to achieve at least 80dB attenuation between f_c and $1.2f_c$ (Reference 1). The corresponding passband ripple, return loss, delay, and phase response are also shown in Figure 12.7. This custom filter is available in corner frequencies up to 100MHz and in a choice of PC board, BNC, or SMA compatible packages.

CHARACTERISTICS OF TTE, INC., L31182-SERIES 11-POLE ELLIPITICAL FILTER



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Figure 12.7

From this discussion, we can see how the sharpness of the antialiasing transition band can be traded off against the ADC sampling frequency. Choosing a higher sampling rate (oversampling) reduces the requirement on transition band sharpness (hence, the filter complexity) at the expense of using a faster ADC and processing data at a faster rate. Remember that high speed ADCs are not oversampling as in the case of Sigma-Delta converters.

You can begin the above design process by choosing an initial sampling rate of 2 to 4 times f_a. Determine the filter specifications based on the required dynamic range and see if such a filter is realizable within the constraints of the system cost and performance. If not, consider a higher sampling rate and a faster ADC.

You can also relax the antialiasing filter requirements somewhat if you know that you are never going to get a fullscale signal at the stopband frequency $f_s - f_a$. In many applications it is very rare that fullscale signals will occur at this frequency. If you know that your maximum signal at the frequency $f_s - f_a$ will never exceed XdB below fullscale, then the filter stopband attenuation requirement is reduced by

that same amount. The new requirement for stopband attenuation at $f_s - f_a$ based on this knowledge of the signal is now only DR – XdB. When making this type of assumption, be careful to treat any noise signals which may occur above the maximum signal frequency f_a as unwanted signals which will also alias back into the signal bandwidth.

PROPERLY SPECIFYING THE ADC RESOLUTION AND DYNAMIC RANGE REQUIREMENTS

So far, we have discussed only the effects of ADC sampling and aliasing on the system dynamic range. The effects of dividing the signal amplitude into a finite number of discrete quantization levels must also be considered.

Figure 12.8 shows a table of relative bit sizes for various resolution ADCs. The fullscale input range is chosen to be approximately 2V which is popular for high speed ADCs. The bit size (or LSB weight, q) is determined by dividing the fullscale range of the converter by the number of possible quantization levels. Hence, a 10bit ADC having 1024 discrete levels has an LSB weight of 2.048V/1024, or 2mV.

BIT SIZES, THEORETICAL QUANTIZATION NOISE, AND SNR FOR 2.048V FULLSCALE CONVERTERS

Resolution (N Bits)	1 LSB = q	% FS	ppm FS	dB FS (6N)	RMS Quantization Noise, q/√12	Theoretical Fullscale SNR (dB)
6	32mV	1.56	15625	36	9.2mV	37.9
8	8mV	0.39	3906	48	2.3mV	50.0
10	2mV	0.098	977	60	580µV	62.0
12	500µV	0.024	244	72	144µV	74.0
14	125µV	0.0061	61	84	36µV	86.0
16	31µV	0.0015	15	96	13µV	98.1

Figure 12.8

The selection process for determining the ADC resolution should begin by determining the ratio between the largest signal (fullscale) and the smallest signal you wish the ADC to detect. Convert this ratio to dB, and divide by 6. This is your *minimum* ADC resolution requirement for dc signals. You will actually need more resolution to account for extra signal headroom, since ADCs act as hard limiters at both ends of their range. Remember that this computation is for dc or low frequency signals and that the ADC performance will degrade somewhat as the input signal slewrate increases. What will actually occur is that the final ADC resolution will be dictated by dynamic performance at high frequencies. This will lead to the selection of an ADC which probably has more resolution at dc than is actually required.

Also shown in the table of Figure 12.8 is the theoretical rms quantization noise produced by a perfect N-bit ADC. It has been demonstrated that this noise can usually be treated as random noise which is uncorrelated with the input signal. The quantization noise is spread uniformly over the entire Nyquist bandwidth dc to $f_S/2$. The theoretical fullscale rms sinewave signal-to-noise ratio (SNR) may then be calculated using the well known formula, SNR = 6.02N + 1.76dB.

In actual practice, sampling ADCs are evaluated for their dynamic performance by first applying a spectrally pure sinewave input and then performing an FFT on the ADC output data as shown in Figures 12.9 and 12.10. The FFT output can be used to calculate harmonic distortion, THD, and SNR. The actual SNR is then compared to the theoretical SNR. The measured SNR may be substituted in the SNR formula, and the equation solved for N. The resulting value for N is called the *effective number of bits, or ENOBs.*

ADC DYNAMIC TESTING

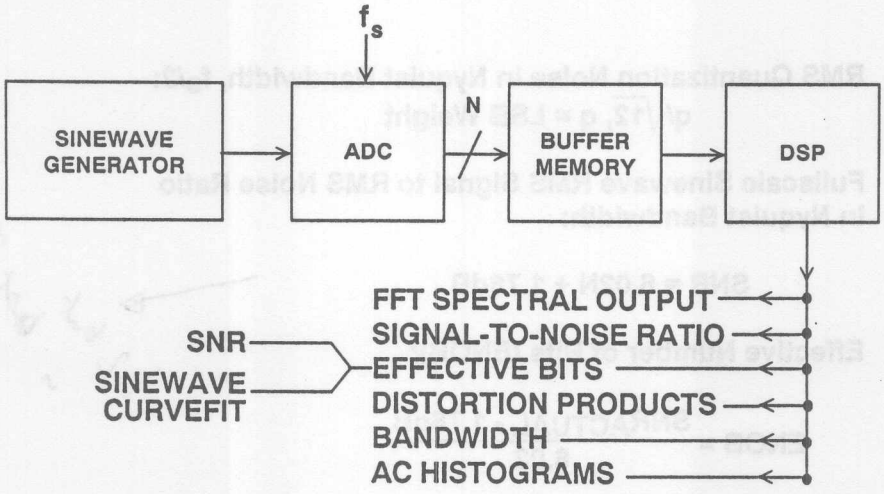


Figure 12.9

4096 POINT FFT OUTPUTS FOR AD9022 12-BIT, 20MSPS ADC

F_S = 20 MSPS

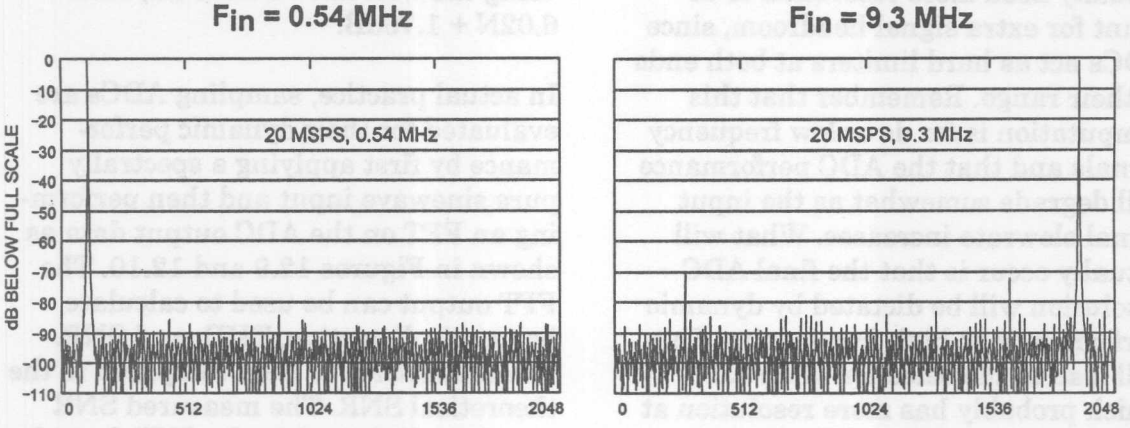


Figure 12.10

QUANTIZATION THEORY BASICS

- RMS Quantization Noise in Nyquist Bandwidth, $f_S/2$:
  $q/\sqrt{12}$, q = LSB Weight
- Fullscale Sinewave RMS Signal to RMS Noise Ratio in Nyquist Bandwidth:

$$SNR = 6.02N + 1.76dB$$

- Effective Number of Bits (ENOB):

$$ENOB = \frac{SNR_{ACTUAL} - 1.76dB}{6.02}$$

Figure 12.11

The SNR and effective bits measurement is made for both low, intermediate, and high frequency input signals. Practically all ADCs exhibit some degradation in SNR and ENOBs at higher input signal frequencies due to various sources of ac nonlinearities. Figure 12.12 shows the S/(N + D) for the AD9022 12 bit, 20MSPS monolithic sampling ADC.

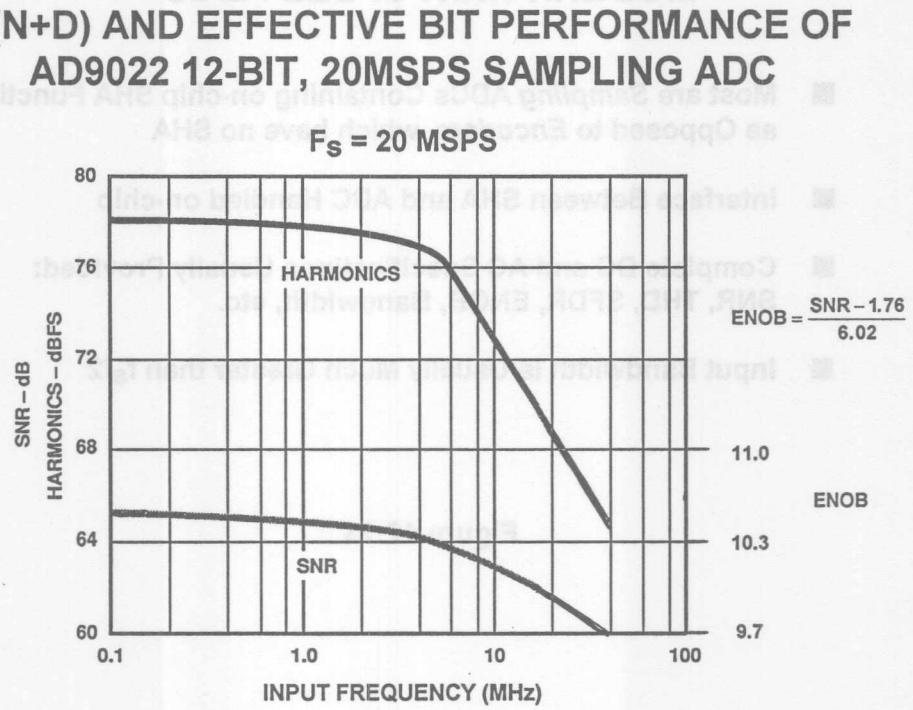


Figure 12.12

The AD9022 is representative of a class of high-performance *sampling* ADCs. Sampling ADCs have the sample-and-hold function on-chip and are characterized in terms of both dc and ac specifications.

MODERN HIGH SPEED ADCs

- Most are *Sampling* ADCs Containing on-chip SHA Function as Opposed to *Encoders*, which have no SHA
- Interface Between SHA and ADC Handled on-chip
- Complete DC and AC Specifications Usually Provided: SNR, THD, SFDR, ENOB, Bandwidth, etc.
- Input Bandwidth is Usually Much Greater than $f_S/2$

Figure 12.13

ADC FULL-POWER BANDWIDTH

- The Frequency at Which the Amplitude of the *Fundamental* Component in the FFT Output is Down 3dB
- FPBW Usually > f_S (Except for $\Sigma\Delta$ ADCs)
- Must Examine ENOB and THD at FPBW Frequency - Usually Reduced
- Example: AD9022 FPBW = 100MHz, 9.7 ENOB @ 40MHz INPUT
- Use FPBW or Small Signal BW (if Greater Than FPBW) for Noise Calculations

Figure 12.14

The input bandwidth of the ADC should be considerably greater than the highest-frequency baseband signal of interest. The full-power bandwidth (FPBW) of an ADC is that input frequency at which the amplitude of the reconstructed FFT *fundamental* is reduced by 3dB for a fullscale input. Generally, though, there is considerable loss of *resolution* at frequencies well below this. Full-power bandwidth must be examined in conjunction with SNR, ENOB, and THD in order to determine the actual dynamic performance of the ADC at the FPBW frequency. The small signal ADC bandwidth is approximately equal to the FPBW if there is no slewrate limiting.

The next step in the process of determining the ADC resolution is to determine the effective bit (ENOB) requirement or SNR at the highest input frequency of interest, f_a. Most modern sampling ADCs have these specifications and also curves similar to that of Figure 12.12. Remember that the S/(N+D) calculation includes all distortion products as well as those due to quantization.

The *peak spurious* or peak harmonic component is the largest spectral component excluding the input signal and dc (measured with FFT techniques). This value is expressed in dB relative to the rms value of the input signal. This specification is also referred to as *spurious free dynamic range*, or SFDR. In applications such as digital spectral analysis using FFT techniques, harmonic distortion, THD, or spurious free dynamic range (SFDR) may be of greater concern than the actual broadband rms noise level.

The FFT takes a discrete number of time samples, M, and converts them into M/2 discrete spectral components. The spacing between the spectral lines is $\Delta f = f_S/M$. If an FFT is performed on broadband quantization noise which has a bandwidth of $f_S/2$, the average value of the noise contained in each FFT frequency cell is $10\log_{10}(M/2)$ dB less than the rms value of the quantization noise. This is illustrated in Figure 12.15. This is equivalent to sweeping an analog spectrum analyzer from dc to $f_S/2$ with the bandwidth set to Δf. The average value of the noise components in each frequency bin can be reduced 3dB by doubling the record length M. Using deeper FFTs, averaging the results of a number of FFTs, or other filtering techniques may also be used to reduce the rms noise floor and allow greater dynamic range. (This topic will be addressed in greater detail in the section on wide dynamic range applications).

THE EFFECTIVE NOISE FLOOR OF AN M-POINT FFT (MEASUREMENT BANDWIDTH = f_S/M) IS MUCH LESS THAN THE RMS VALUE OF THE QUANTIZATION NOISE (MEASUREMENT BANDWIDTH = $f_S/2$)

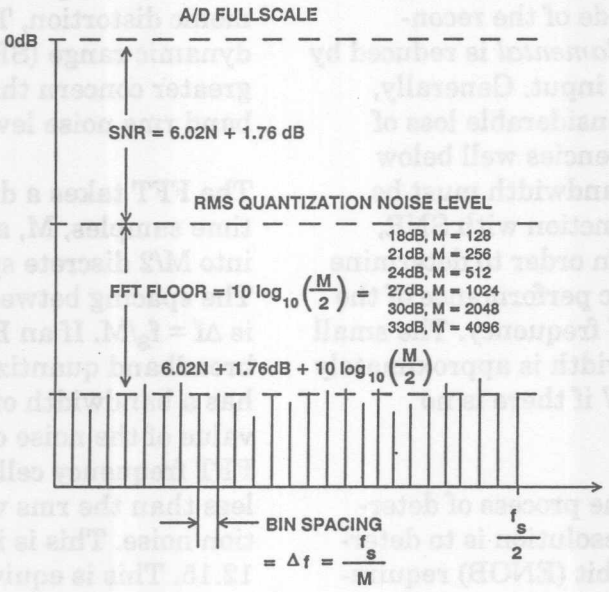


Figure 12.15

SPURIOUS FREE DYNAMIC RANGE AS A FUNCTION OF INPUT SIGNAL LEVEL FOR THE AD9014 14-BIT, 10MSPS ADC

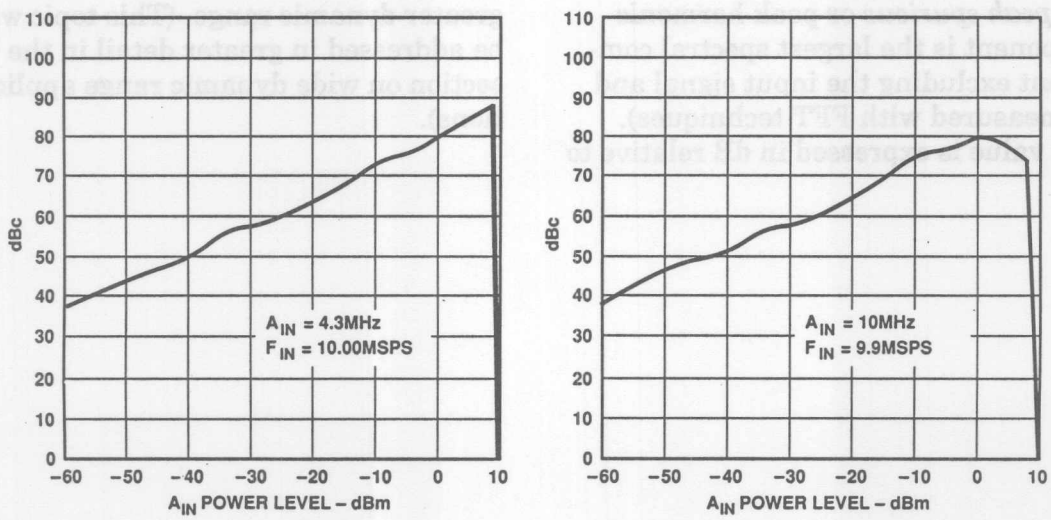


Figure 12.16

The SFDR of an ADC is generally a function of both input frequency and amplitude. Figure 12.16 shows the SFDR versus the input signal level for the AD9014 14 bit 10MSPS ADC. The data is given for two input frequencies: 4.3MHz and 9.9MHz. Notice that the SFDR at 4.3MHz reaches its maximum value at fullscale. For the 9.9MHz input, however, the point of maximum SFDR occurs several dB below fullscale.

As discussed above, SFDR should not be confused with SNR. SNR depends more on the rms value of the quantization noise and is therefore a function of the number of ADC bits. SFDR, on the other hand, depends more on the linearity of the ADC and is relatively independent of the number of actual bits. This is dramatically illustrated in Figure 12.17, where SNR and SFDR is shown for the AD9014 ADC. The top curve in the figure shows the SFDR of the AD9014 utilizing 14, 12, and 10 bits of the ADC. The bottom three curves show the SNR of the AD9014 operating with 14, 12, and 10 bits. The level of the internally generated spurs will not rise as bits are omitted, but the broadband rms noise floor rises for each bit that is dropped.

AD9014 SFDR AND SNR VERSUS FREQUENCY FOR 14, 12, AND 10 ACTIVE BITS

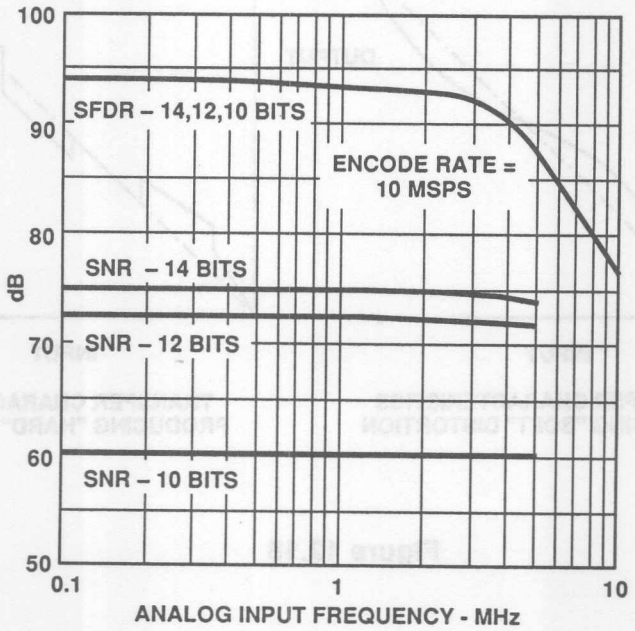


Figure 12.17

The distortion produced by an ADC cannot be analyzed in terms of second and third-order intercepts as in the case of an amplifier. This is because there are two components of distortion in a high performance ADC. One component is due to the non-linearity associated with the analog front end amplifier and the sample-and-hold. This non-linearity has the familiar "bow" or "s"-shaped curve shown in Figure 12.18. The distortion associated with this type of non-linearity is sometimes referred to as *soft* distortion and produces low-order distortion products. This component of distortion behaves in the traditional manner and is a function of signal level. In a practical ADC, however, the soft distortion is usually much less than the other component of distortion in an ADC which is due to the nonlinearity of the encoder transfer function itself. This function is more likely to have discrete points of discontinuity across the signal range as shown in Figure 12.18.

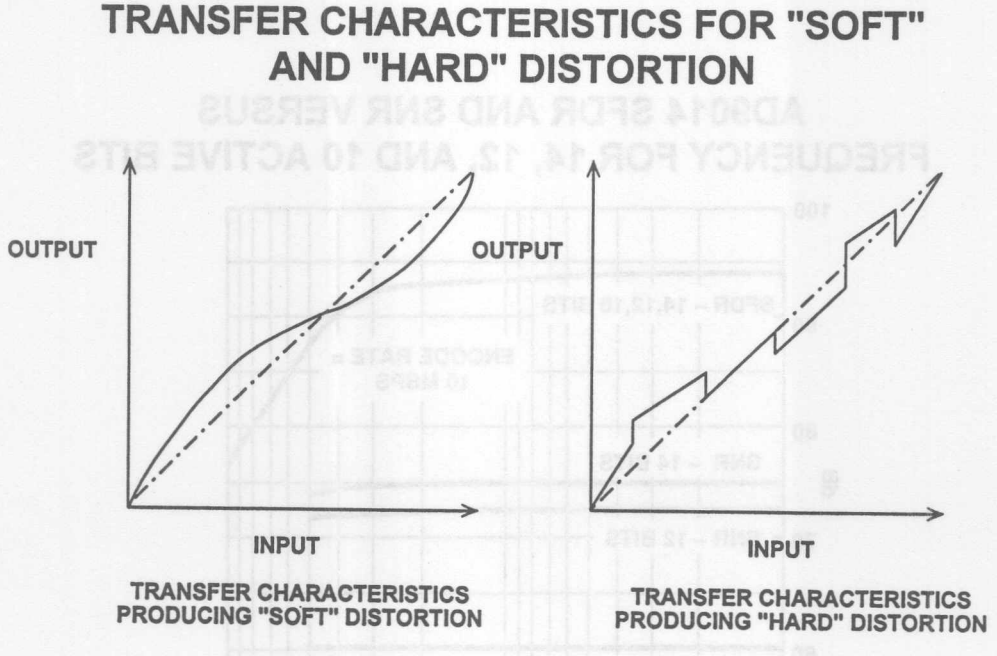


Figure 12.18

The actual location of the points of discontinuity depends on the particular ADC architecture, but nevertheless such discontinuities occur in practically all high speed ADCs. Non-linearity of this type produces high-order distortion products which are relatively unpredictable with respect to input signal level. For lower-amplitude signals, this constant level *hard* distortion causes the SFDR of the ADC to decrease as input amplitude decreases. The soft distortion in a well-designed ADC generally only comes into play for high frequency large-amplitude input signals where it may rise above the hard distortion floor. This can be observed in Figure 12.16, where the 4.3MHz input data indicates a relatively constant hard distortion floor as the signal amplitude is increased to fullscale. The 9.9MHz data, however, indicates an increase in soft distortion as the input signal approaches fullscale.

HIGH SPEED FLASH CONVERTERS AND ERROR SOURCES

The ADC architecture which offers the highest possible sampling rate is the flash converter. Recent advances in VLSI process technology and circuit design techniques have made flash ADCs with up to 10 bits of resolution practical. As well as offering high sampling rates for digitizing high frequency signals, flash converters are often used as building blocks for higher resolution ADCs.

A block diagram of a typical flash converter is shown in Figure 12.19. The analog input signal to be digitized is applied simultaneously to $2^N - 1$ latched comparators, where N is the number of bits. The reference voltage input for each comparator is derived from a resistive voltage divider string. The reference voltage for each comparator is one LSB higher than the one immediately below it.

When an analog signal is present at the input of the comparator bank, all comparators which have a reference voltage below the level of the input signal will assume a logic "1" output. The comparators which have their reference voltage above the input signal will assume a logic "0" output. The result is often referred to as a *thermometer code* (shown in Figure 12.20), and is applied to the decoding logic stage. This decoding can be accomplished in a variety of ways (such as a simple priority encoder) and ultimately results in the digital output word.

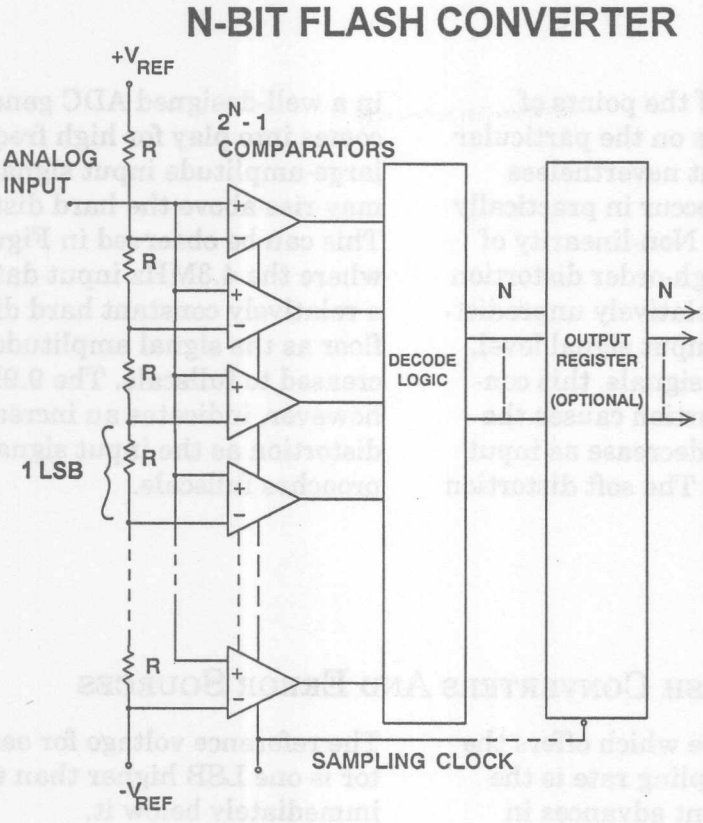


Figure 12.19

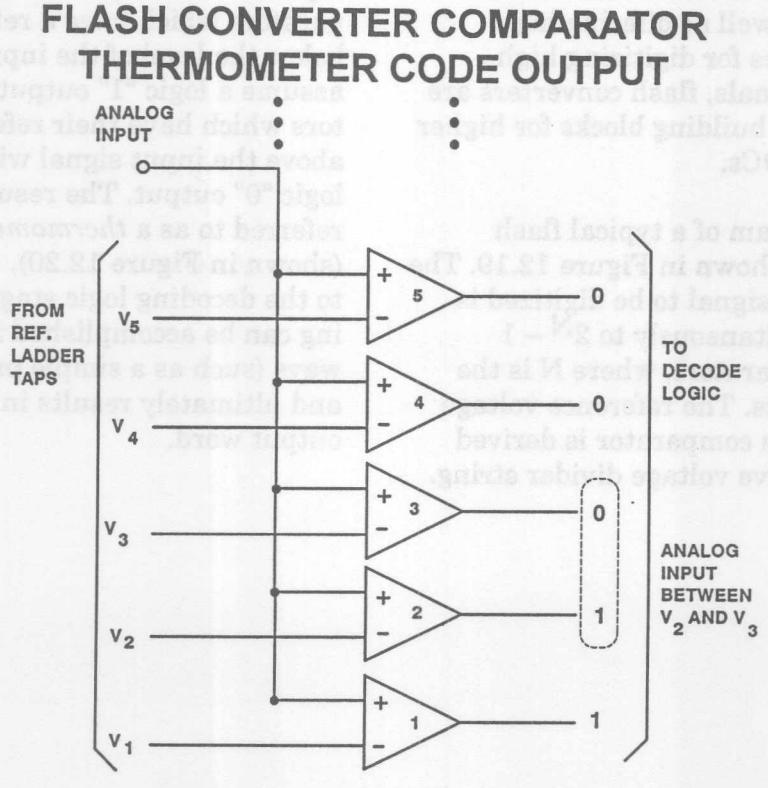


Figure 12.20

The primary source of dc nonlinearity in a flash converter is the comparator input offset voltage variation. In a good flash converter this nonlinearity should be less than ±½LSB. The reference voltage resistor ladder string rarely contributes significant error as it has inherently good ratio matching.

Dynamic errors in a flash converter come from several sources, the chief source being the ac mismatch between comparators. In an ideal flash converter with perfectly matched (ac and dc) comparators, each comparator latches simultaneously when the sampling clock is asserted. This effectively provides an internal SHA function, and the overall ADC nonlinearity is independent of the input signal slewrate. In actual flash converters, however, the delay and bandwidth matching of the comparators is not perfect. Although this mismatch does not affect dc performance, it will introduce slewrate-dependent nonlinearities. The effect is to reduce the SNR and ENOB performance of the flash converter at high frequencies. Well designed flash converters, however, are capable of maintaining good performance at fairly high input frequencies without the necessity for an external SHA. The SNR and ENOB performance of the AD9058 dual 8 bit 50MSPS flash converter is shown in Figure 12.21. Notice that 40dB SNR (6.4 ENOBs) is achieved at an input frequency of 20MHz.

SNR, EFFECTIVE BIT, AND HARMONIC DISTORTION OF THE AD9058 DUAL 8-BIT, 50MSPS FLASH CONVERTER

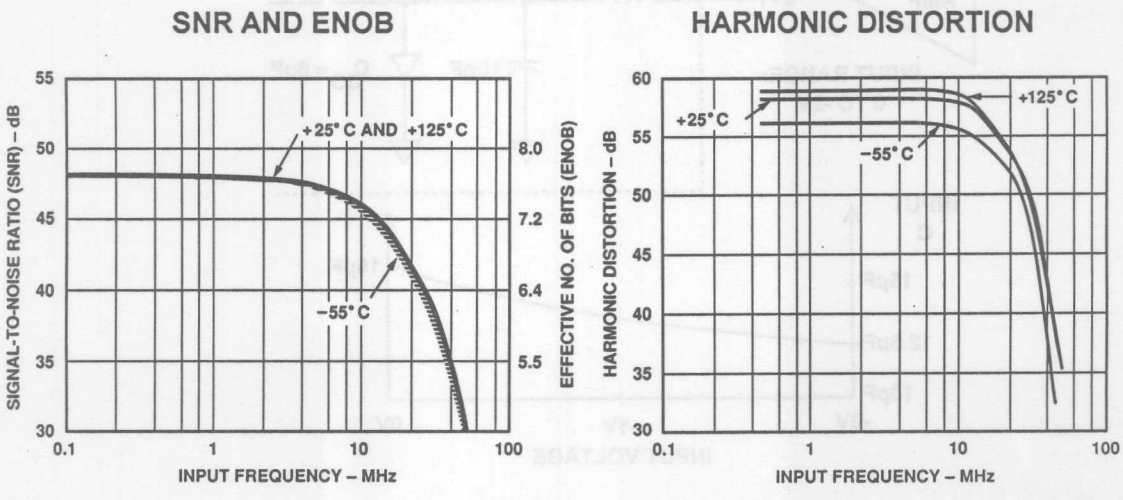


Figure 12.21

Another source of dynamic errors in a flash converter is the signal-dependent input capacitance. The input stage of each comparator in a flash converter is a long tail, common emitter differential pair. The analog input is applied to one base, and the reference ladder voltage to the other base. As the input signal changes, the corresponding input capacitance will also change. The problem is compounded because of the large number of comparators in parallel.

The input circuit of the AD9028/ AD9038 8 bit, 300MSPS flash converter is modeled in Figure 12.22. The signal-dependent capacitance is modeled as a reverse-biased diode. The total input capacitance as a function of signal level is also shown in Figure 12.22.

Wideband, low-distortion current feedback amplifiers such as the AD9617 are ideal for driving this type of flash converter. However, a series resistor of approximately 50Ω is required to isolate the amplifier from the converter input capacitance in order to prevent peaking and to maintain stability. Because of the series resistor and the signal-dependent capacitance, harmonic distortion will result as shown in Figure 12.23. The series isolation resistor should therefore be no larger than is necessary to maintain op amp stability. Large resistor values will increase the distortion and limit the input bandwidth. Datasheets for flash converters should provide you with recommended drive circuits for optimum performance.

AD9028/AD9038 EQUIVALENT INPUT CIRCUIT AND SIGNAL-DEPENDENT CAPACITANCE

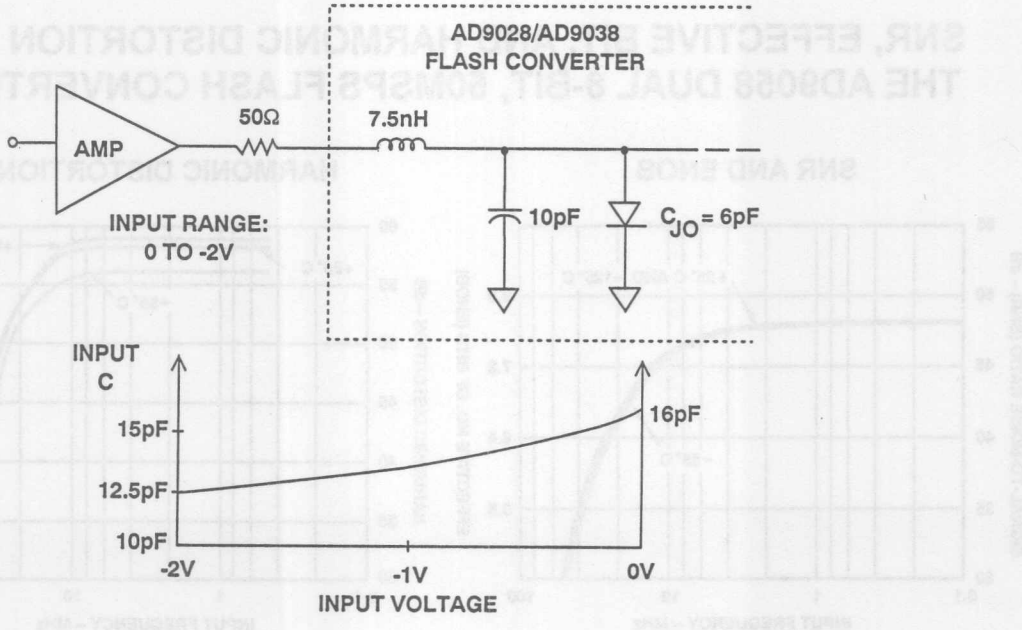


Figure 12.22

SIMULATED THD DUE TO SIGNAL-DEPENDENT INPUT CAPACITANCE

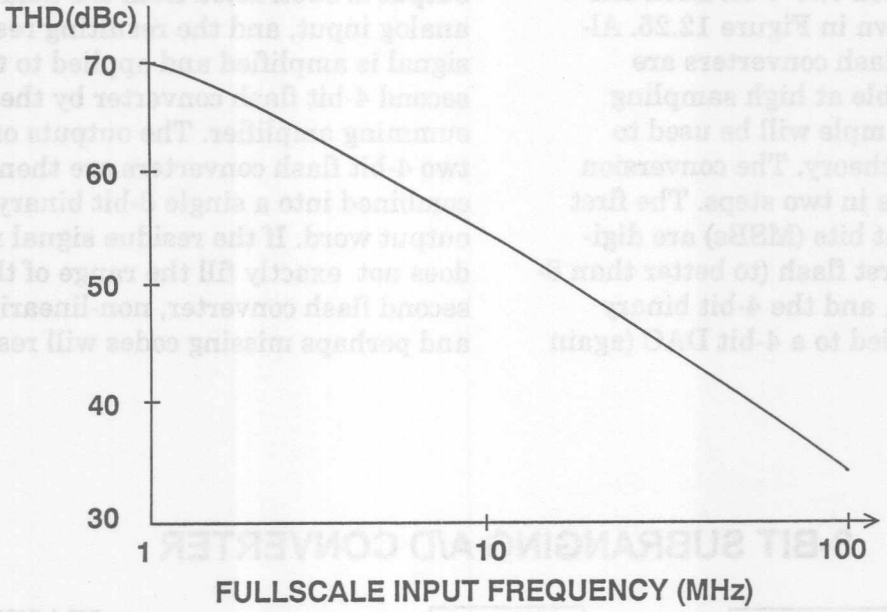


Figure 12.23

12

FLASH CONVERTER PRIMARY ERROR SOURCES

- **Static Errors:**
  - **Comparator Input Offset Voltage Mismatch**
- **Dynamic Errors:**
  - **Comparator Bandwidth and Delay Mismatch**
  - **Signal-Dependent Input Capacitance**
  - **Layout Parasitics**

Figure 12.24

HIGH SPEED SUBRANGING ADCS AND ERROR SOURCES

A block diagram of an 8-bit subranging ADC based upon two 4-bit flash converters is shown in Figure 12.25. Although 8-bit flash converters are readily available at high sampling rates, this example will be used to illustrate the theory. The conversion process is done in two steps. The first four significant bits (MSBs) are digitized by the first flash (to better than 8-bits accuracy), and the 4-bit binary output is applied to a 4-bit DAC (again better than 8-bit accurate). The DAC output is subtracted from the held analog input, and the resulting residue signal is amplified and applied to the second 4-bit flash converter by the summing amplifier. The outputs of the two 4-bit flash converters are then combined into a single 8-bit binary output word. If the residue signal range does not exactly fill the range of the second flash converter, non-linearities and perhaps missing codes will result.

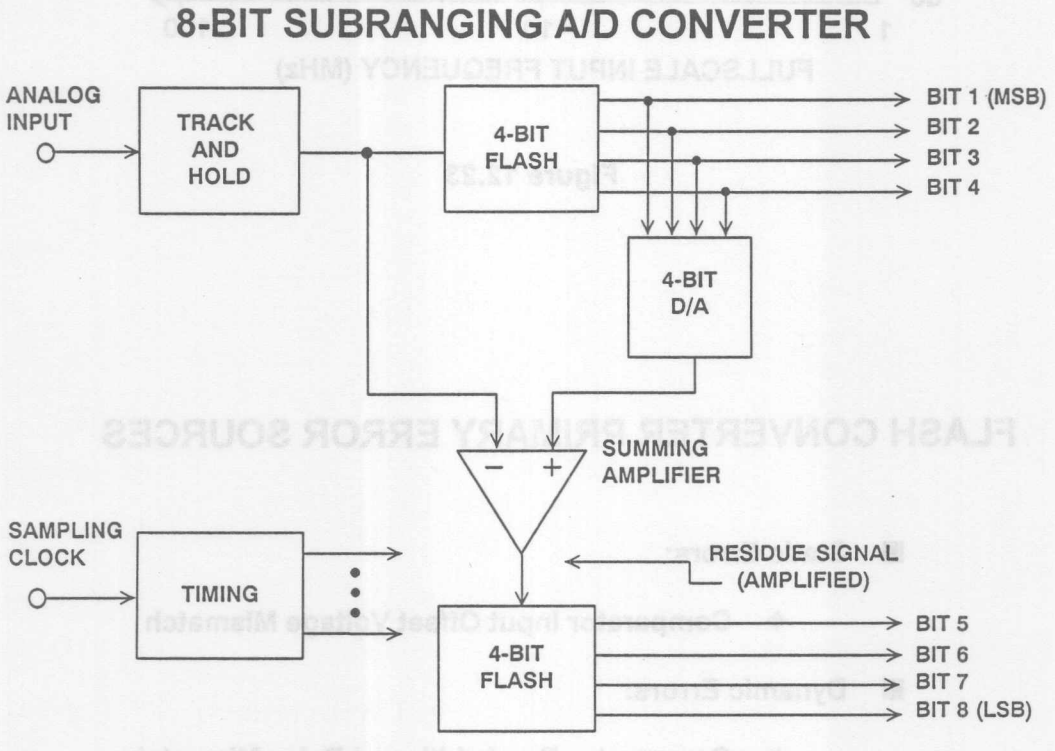


Figure 12.25

Modern subranging ADCs use a technique called *digital correction* to eliminate problems associated with the architecture of Figure 12.25. A block diagram of a 12-bit digitally corrected subranging (DCS) ADC is shown in Figure 12.26. Note that a 5-bit and an 8-bit flash converter have been used to achieve an overall 12-bit output. If there were no errors, the 5-bit "residue" signal applied to the 8-bit flash converter by the summing amplifier would never exceed one-half of the range of the 8-bit flash. The extra range in the second flash converter is used in conjunction with the error correction logic (usually just an adder) to correct the output data for most of the errors inherent in the traditional uncorrected subranging converter architecture.

12-BIT DIGITALLY CORRECTED SUBRANGING ADC

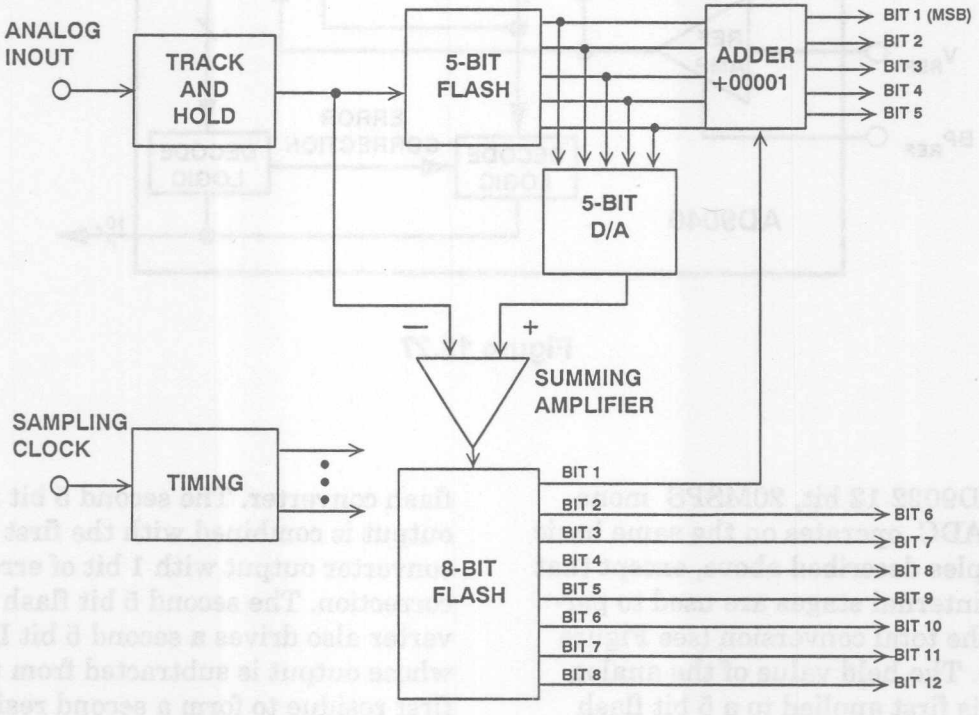


Figure 12.26

A block diagram of the AD9040 10 bit, 40MSPS ADC is shown in Figure 12.27. This ADC makes use of two stages. The held analog value of the first track-and-hold is applied to a 5 bit flash converter and a pair of internal T/Hs (shown on the diagram as a single unit). The T/Hs pipeline the analog signal to the amplifier array through a residue ladder and switching circuit while the 5 bit flash converter resolves the most significant bits (MSBs) of the held analog voltage. When the 5 bit flash converter has completed its cycle, its output activates 1-of-32 ladder switches; these, in turn, cause the correct residue signal to be applied to the error amplifier array. The output of the error amplifier is applied to a 6 bit flash converter whose output supplies the five least significant bits (LSBs) of the digital output along with one bit of error correction for the main range converter. Decoding logic combines the bits from the two converters and presents the result as a 10 bit parallel word.

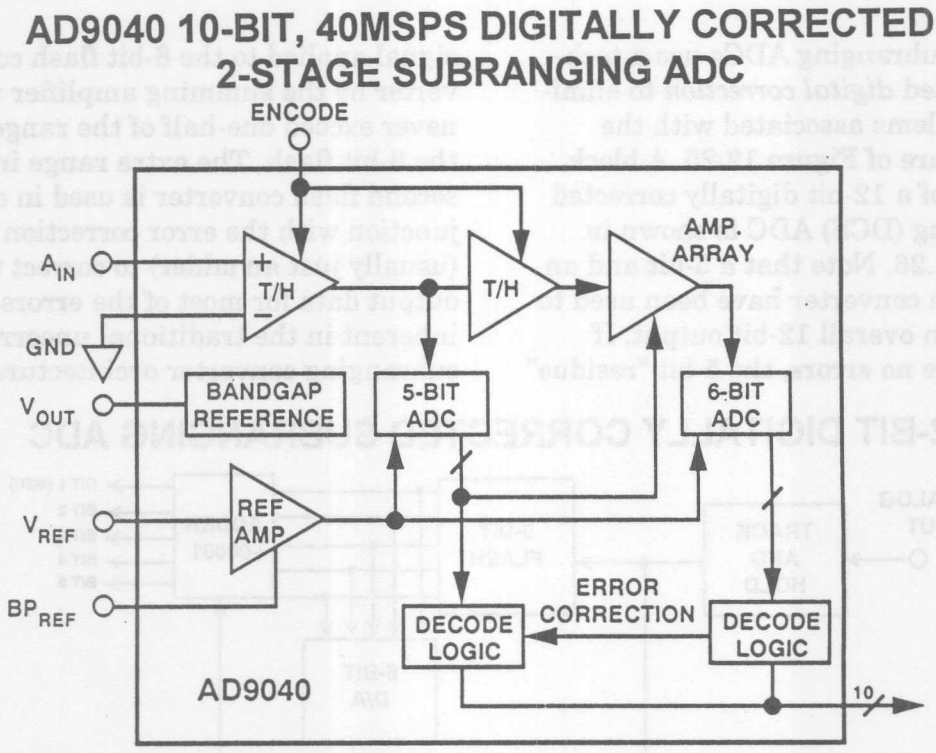


Figure 12.27

The AD9022 12 bit, 20MSPS monolithic ADC operates on the same basic principles described above, except that three internal stages are used to perform the total conversion (see Figure 12.28). The held value of the analog input is first applied to a 5 bit flash converter which performs the first coarse conversion. The first 5 bit flash converter output also drives a 5 bit DAC whose output is subtracted from the held analog signal to form the first residue. The second T/H pipelines the residue and applies it to a gain-of-16 amplifier which drives a second 5 bit flash converter. The second 5 bit flash output is combined with the first flash converter output with 1 bit of error correction. The second 5 bit flash converter also drives a second 5 bit DAC whose output is subtracted from the first residue to form a second residue . The second residue is applied to a gain-of-8 amplifier which drives a 4 bit flash converter. The final 4 bit flash converter output is combined with the outputs of the two 5 bit converters in a logic block which performs the digital error correction and generates the final ADC output word.

AD9022 12-BIT, 20MSPS DIGITALLY CORRECTED 3-STAGE SUBRANGING ADC

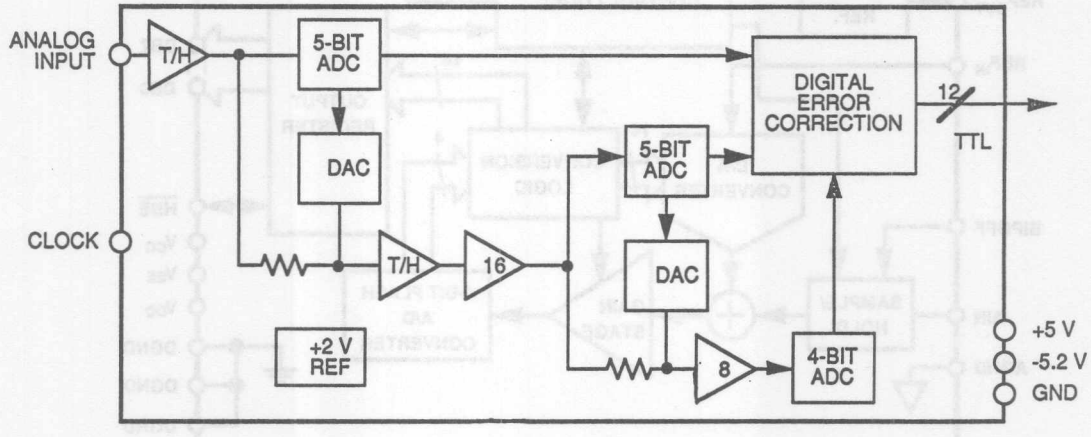


Figure 12.28

At slower sampling rates it is possible to use a single flash converter in multiple passes to perform the conversions as shown in Figure 12.29. The AD679 is a 14 bit 100kSPS ADC which uses this *recursive subranging* approach. The 4 bit flash first produces a 4 bit representation of the analog input. This value is reconstructed by the DAC, and the difference between the DAC output is amplified (to take full advantage of the dynamic range of the 4 bit flash), and the whole cycle then repeats itself. After 5 cycles, the result is presented to the final output. A 1 bit overlap between cycles serves as error correction.

AD679 14-BIT, 100kSPS RECURSIVE SUBRANGING ADC

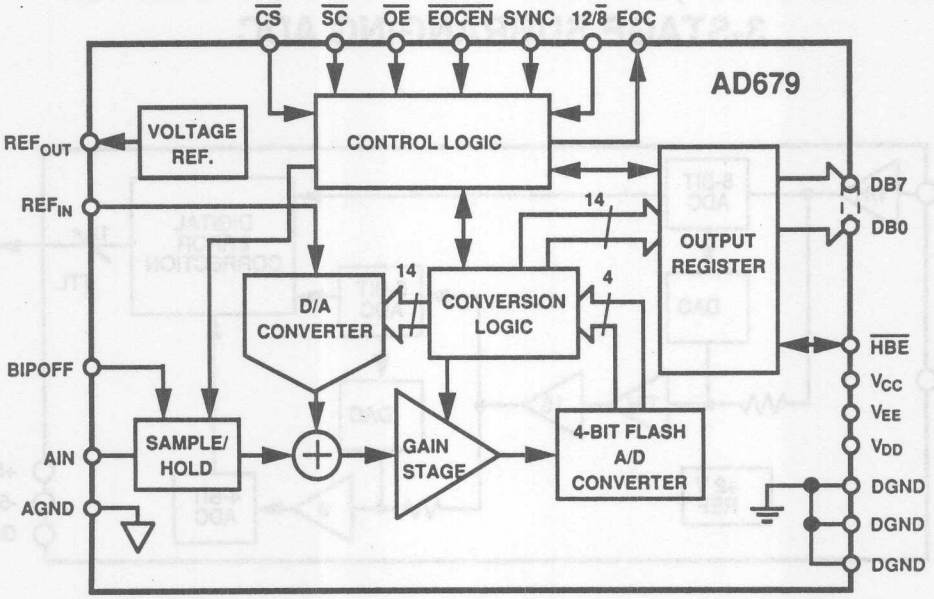


Figure 12.29

The error correction schemes described above are designed to correct for errors made in the early pipelined sub-conversions. Flash converter gain, offset, and linearity errors are corrected as long as the residue signals fall within the range of the next-stage flash conversion. These errors will not affect the linearity of the overall ADC transfer characteristic. Errors made in the final flash conversion, however, do translate directly as errors in the overall transfer function. Also, linearity errors or gain errors either in the DACs or the residue amplifiers will not be corrected and will show up as nonlinearities or non-monotonic behavior in the overall ADC transfer function. If the converter is not properly trimmed or drifts over temperature, errors such as those shown in Figure 12.31 may develop at the various DAC switching points along the ADC transfer function. A properly designed and trimmed ADC, however, should not exhibit errors such as these over the operating temperature range of the device.

SOME ERROR SOURCES IN DIGITALLY CORRECTED SUBRANGING ADCs

- Nonlinearities in Final Flash Conversion
- Internal DAC Linearity or Gain Errors
- Residue Amplifier Gain Errors
- Improper Laser Trimming of Thin Film Resistors
- Internal Timing Errors

Figure 12.30

IMPROPERLY TRIMMED SUBRANGING ADC LINEARITY ERRORS

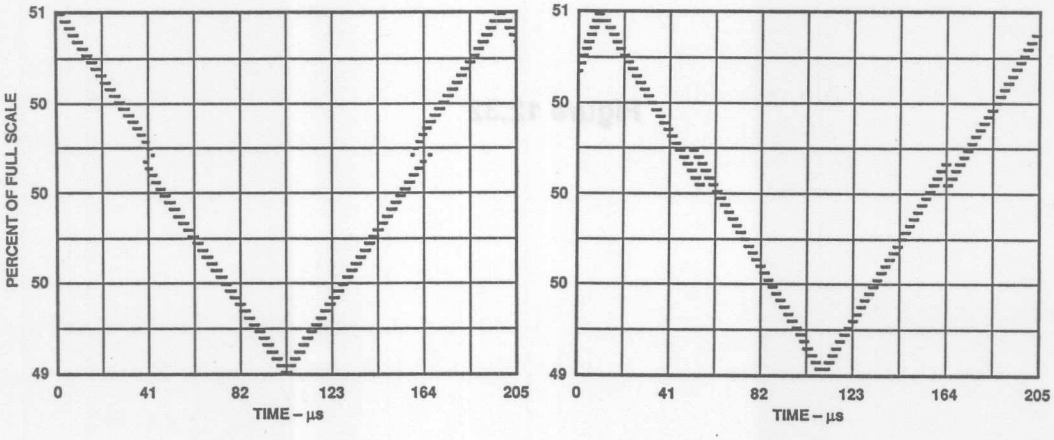


Figure 12.31

APERTURE DELAY TIME (OR EFFECTIVE APERTURE DELAY TIME)

Aperture delay time (sometimes called aperture time) is the amount of time from the leading edge of the sampling clock until the ADC actually takes the sample (see Figure 12.32). This specification is important because it helps the user to know when to apply the sampling clock with respect to the input signal timing. The variation or tolerance placed on this parameter from part to part is important in simultaneous sampling applications or other applications such as I and Q demodulation where the ADCs are required to track each other when processing dynamic signals.

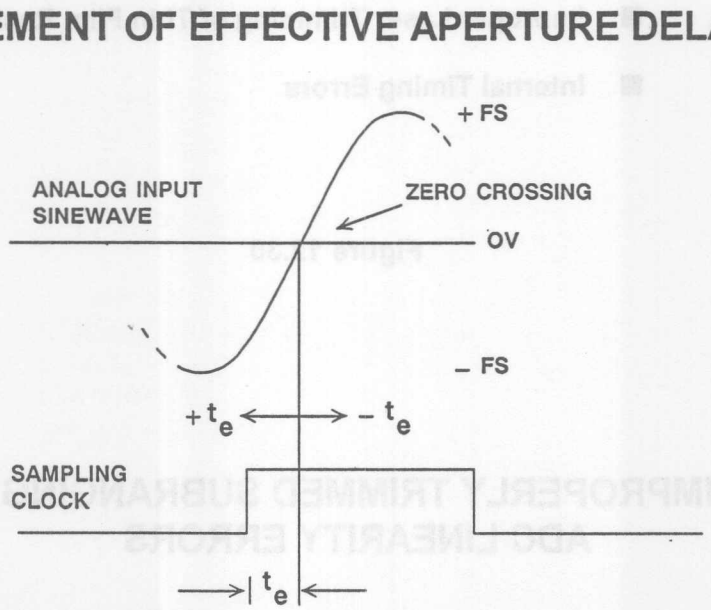


Figure 12.32

ERRORS DUE TO APERTURE JITTER

Aperture jitter is the sample-to-sample variation in the effective point in time at which the actual sample is taken (Figure 12.33). These errors generally emanate from several sources. In practical systems, the sampling clock is often phase-modulated by an external noise source; the source can be wideband random noise, power line noise, or digital noise due to poor layout, bypassing, and grounding techniques. While it is true that a portion of the total aperture jitter may be generated internal to the ADC, this component is rarely the dominant source of SNR degradation at high input frequencies. Nonlinearity in the ac transfer function and increased distortion are usually the major problems.

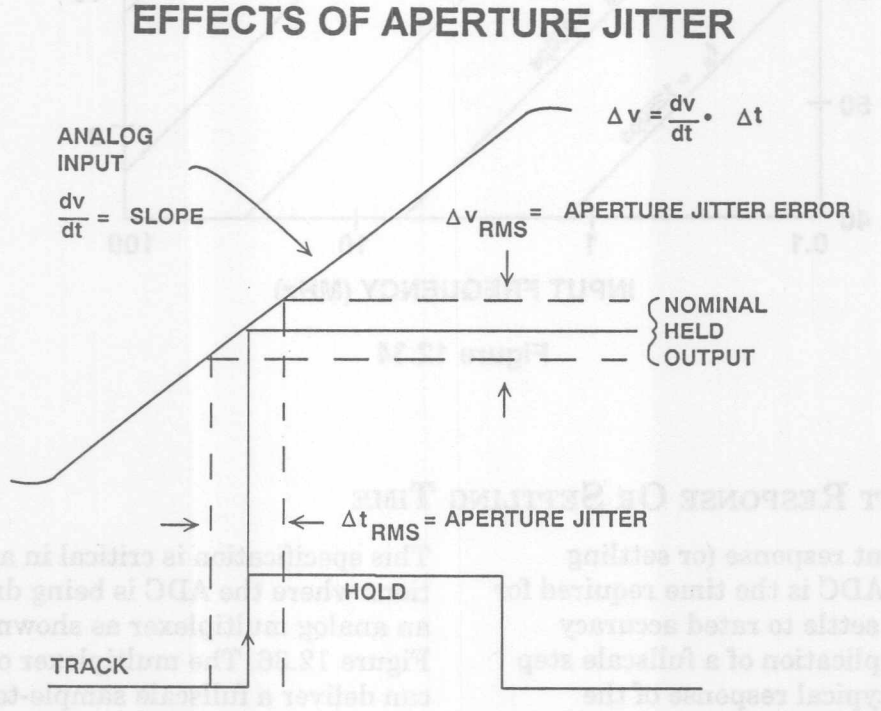


Figure 12.33

The resulting error can be expressed in terms of an rms time jitter. The corresponding rms voltage error caused by rms aperture jitter decreases the overall ADC signal-to-noise ratio. Phase jitter on the input sinewave can produce the same effect as jitter on the sampling clock. The SNR due exclusively to aperture jitter is plotted in Figure 12.34 as a function of fullscale sinewave input frequency for various values of aperture jitter. The equation for SNR due to aperture jitter is derived in Reference 2. Close examination of these curves indicates the importance of maintaining a low-jitter sampling clock if high values of SNR are required.

EFFECTS OF APERTURE JITTER ON SNR AND ENOB

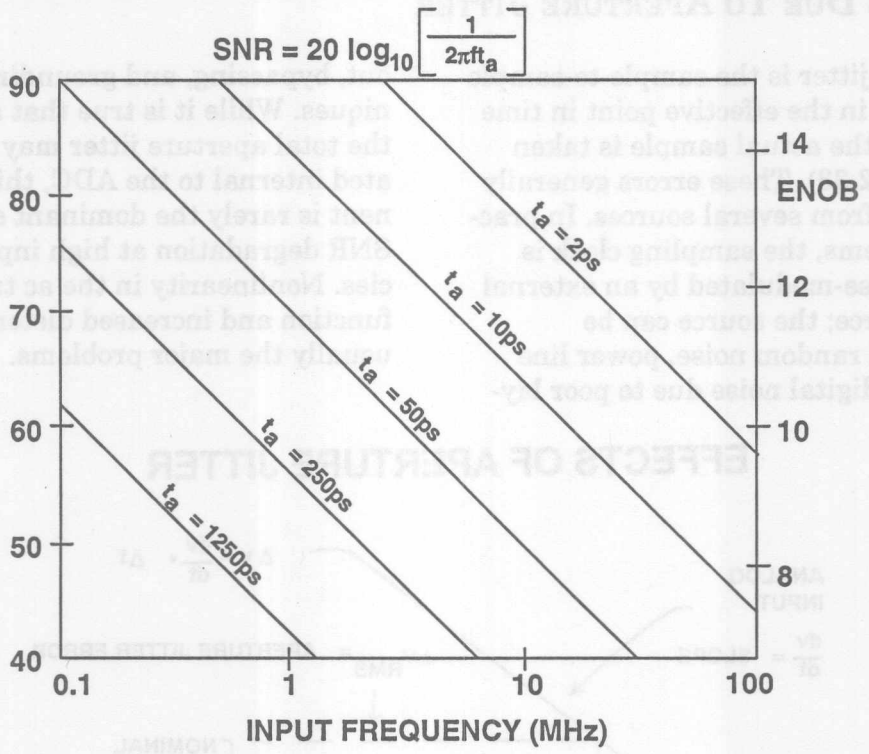


Figure 12.34

TRANSIENT RESPONSE OR SETTLING TIME

The transient response (or settling time) of an ADC is the time required for the ADC to settle to rated accuracy after the application of a fullscale step input. The typical response of the AD872 12 bit, 10MSPS ADC is shown in Figure 12.35. The AD872 can typically settle to 12 bit accuracy from a fullscale step input in less than 40ns.

This specification is critical in applications where the ADC is being driven by an analog multiplexer as shown in Figure 12.36. The multiplexer output can deliver a fullscale sample-to-sample change to the ADC input. If both the multiplexer and the ADC have not both settled to the required accuracy, channel-to-channel crosstalk will result.

AD872 12-BIT, 10MSPS ADC TRANSIENT RESPONSE

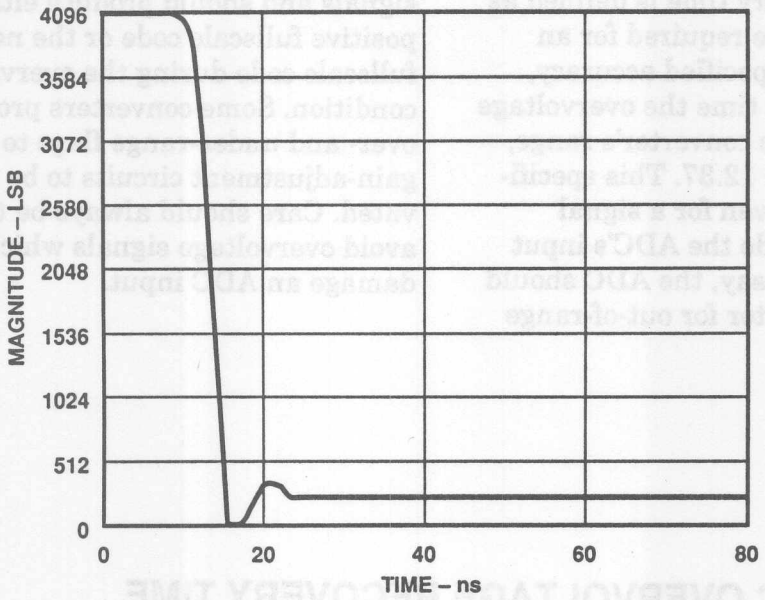


Figure 12.35

DATA ACQUISITION SYSTEM USING AN ANALOG MULTIPLEXER

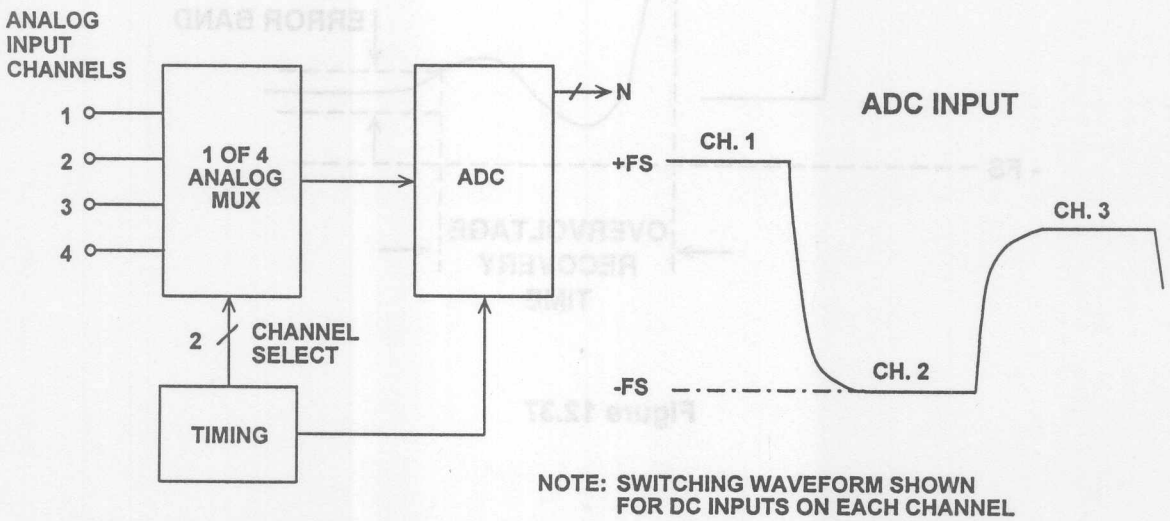


Figure 12.36

OVERVOLTAGE RECOVERY TIME

Overvoltage recovery time is defined as that amount of time required for an ADC to achieve a specified accuracy, measured from the time the overvoltage signal re-enters the converter's range, as shown in Figure 12.37. This specification is usually given for a signal which is 50% outside the ADC's input range. Needless to say, the ADC should act as an ideal limiter for out-of-range signals and should produce either the positive fullscale code or the negative fullscale code during the overvoltage condition. Some converters provide over- and under-range flags to allow gain-adjustment circuits to be activated. Care should always be taken to avoid overvoltage signals which will damage an ADC input.

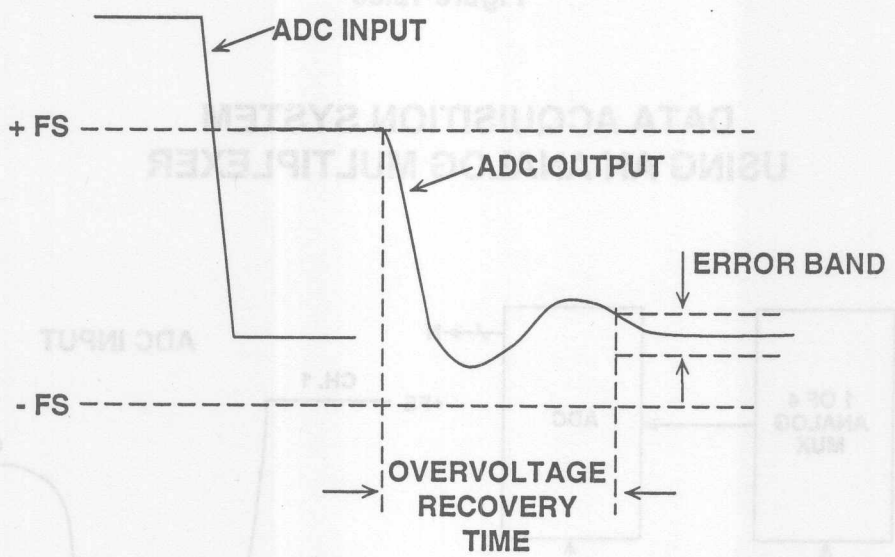


Figure 12.37

METASTABILITY AND BIT ERROR RATES IN ADCS

A primary concern in the design of many digital communications systems using ADCs is the bit error rate (BER). Unfortunately, ADCs contribute to the BER in ways that are not predictable by simple analysis. This section describes the mechanisms within the ADCs that can contribute to the error rate, ways to minimize the problem, and methods for measuring the BER.

Random noise, regardless of the source, creates a finite probability of errors (deviations from the expected output). Before describing the error code sources, however, it is important to define what constitutes an ADC error code. Noise generated prior to, or inside the ADC can be analyzed in the traditional manner. Therefore, an ADC error code is any deviation from the expected output that is not attributable to the equivalent input noise of the ADC. Figure 12.38 illustrates an exaggerated output of a pure sinewave applied to an ADC. Note that the SNR of the ADC creates some uncertainty in the output. These anomalies are not considered error codes, but are simply the result of ordinary noise and quantization. The large errors are more significant and are not expected. These errors are random and so infrequent that an SNR test of the ADC will rarely detect them. These types of errors plagued a few of the early ADCs for video applications, and were given the name *sparkle codes* because of their appearance on a TV screen as small white dots under certain test conditions. The large errors have also been called *rabbits* or *flyers*. In digital communications applications, this type of error increases the overall system bit error rate (BER).

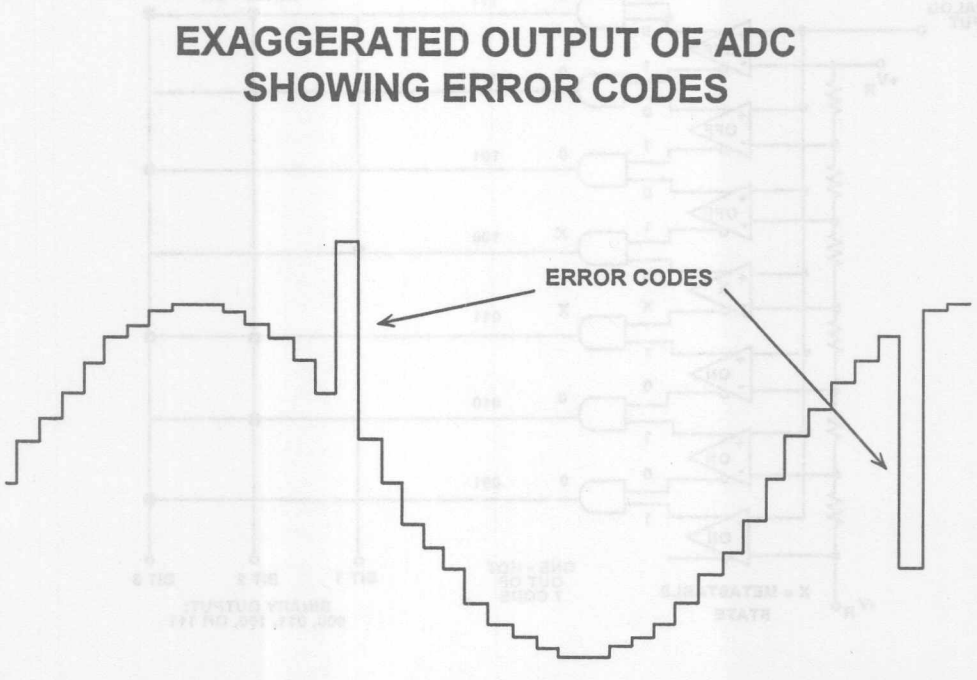


Figure 12.38

In order to understand the causes of the error codes, we will first consider the case of a simple flash converter. The comparators in a flash converter are latched comparators usually arranged in a master-slave configuration. If the input signal is in the center of the threshold of a particular comparator, that comparator will balance, and its output will take a longer period of time to reach a valid logic level after the application of the latch strobe than the outputs of its neighboring comparators which are being overdriven. This phenomenon is known as *metastability* and occurs when a balanced comparator cannot reach a valid logic level in the time allowed for decoding. If simple binary decoding logic is used to decode the thermometer code, a metastable comparator output may result in a large output code error. Consider the case of a simple 3 bit flash converter shown in Figure 12.39. Assume that the input signal is exactly at the threshold of Comparator 4 and random noise is causing the comparator to toggle between a "1" and a "0" output each time a latch strobe is applied. The corresponding binary output should be interpreted as either 011 or 100. If, however, the comparator output is in a metastable state, the simple binary decoding logic shown may produce binary codes 000, 011, 100, or 111. The codes 000 and 111 represent a one-half scale departure from the expected codes.

METASTABLE COMPARATOR OUTPUT STATES MAY PRODUCE ERROR CODES IN FLASH CONVERTERS

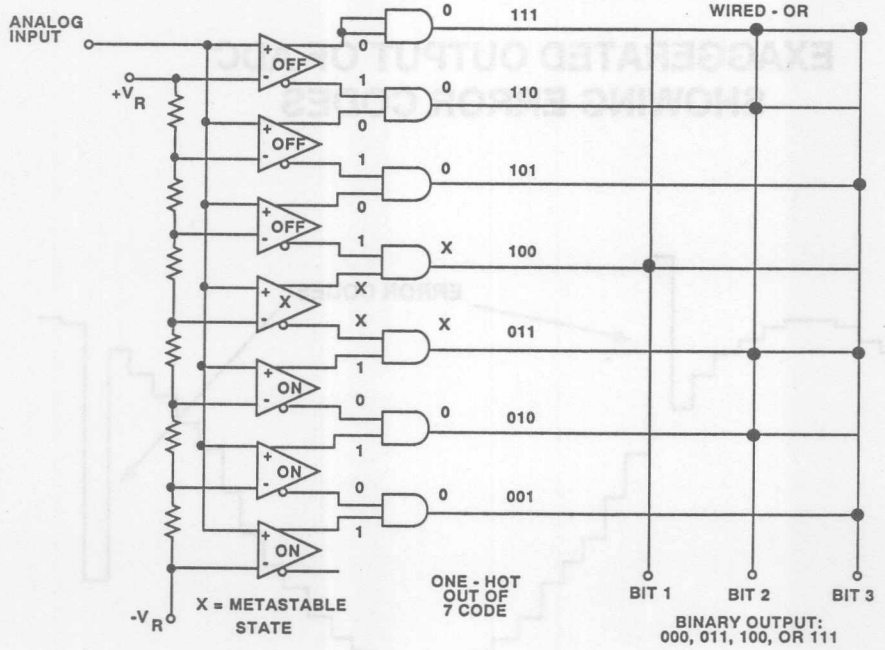


Figure 12.39

The probability of errors due to metastability increases as the sampling rate increases because less time is available for a metastable comparator to settle.

Various measures have been taken in flash converter designs to minimize the metastable state problem. Decoding schemes described in References 3 to 6 minimize the magnitude of these errors. Optimizing comparator designs for regenerative gain and small time constants is another way to reduce these problems.

Metastable state errors may also appear in subranging ADCs which make use of flash converters as building blocks. The same concepts apply, although the magnitudes and locations of the errors may be different.

The test system shown in Figure 12.40 may be used to test for BER in an ADC.

The analog input to the ADC is provided by a high stability low noise sinewave generator. The analog input level is set slightly greater than fullscale, and the frequency such that there is always slightly less than 1 LSB change between samples as shown in Figure 12.41. The test set uses series latches to acquire successive codes A and B. A logic circuit determines the absolute difference between A and B. This difference is then compared to the error limit, chosen to allow for expected random noise spikes and ADC quantization errors. Errors which cause the difference to be larger than the limit will increment the counters. The number of errors, E, are counted over a period of time, T. The error rate is then calculated as $BER = E/2Tf_S$.

ADC BIT ERROR RATE TEST SETUP

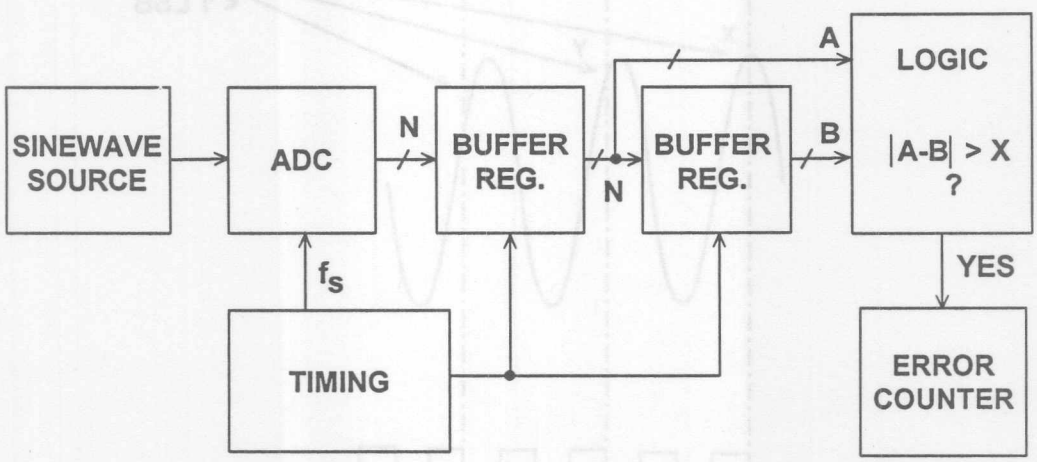


Figure 12.40

ADC ANALOG SIGNAL FOR LOW FREQUENCY BER TEST

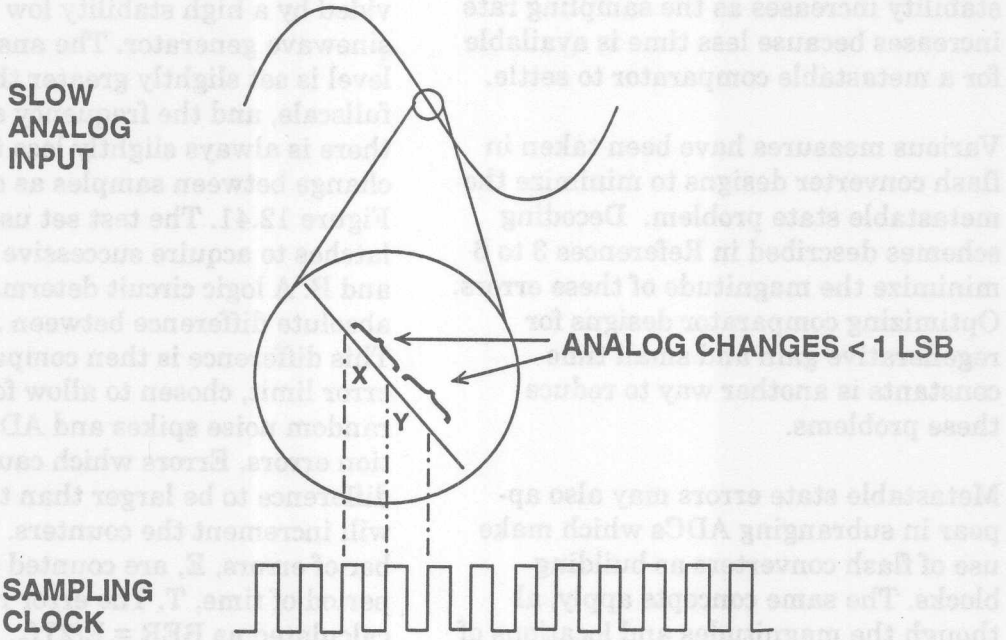


Figure 12.41

ADC ANALOG INPUT FOR HIGH FREQUENCY BER TEST

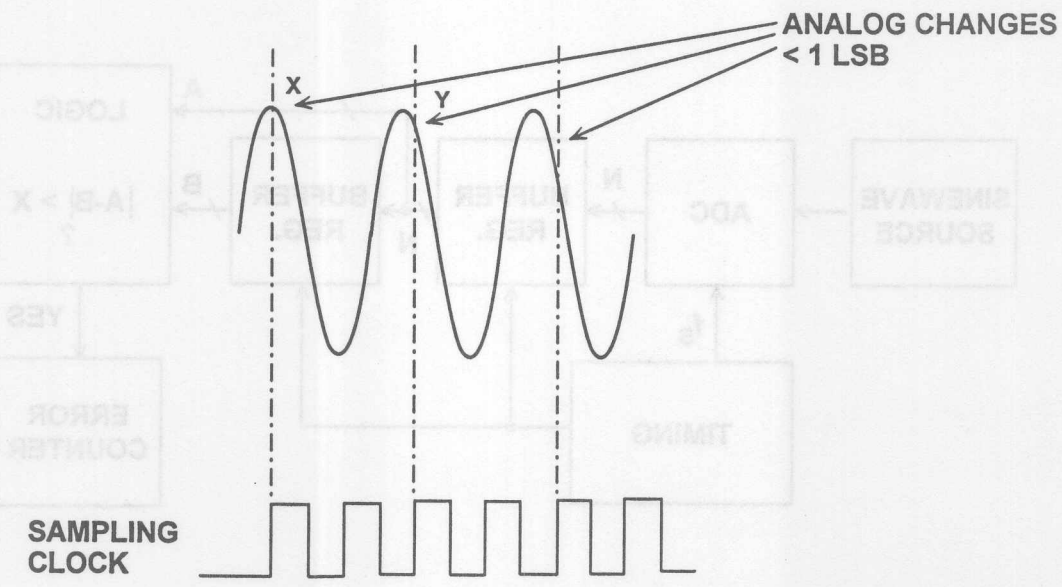


Figure 12.42

SELECTION OF INPUT FREQUENCIES FOR BER TESTING

- For Low Frequency Metastable State Errors:

$$f_{in} = \frac{f_S}{2^N \bullet 2\pi}$$

- For High Frequency Errors:

$$f_{in} = \frac{f_S}{2}\left[1 - \frac{1}{2^N \bullet 4\pi}\right]$$

- N = Number of ADC Bits, f_S = Sampling Rate

Figure 12.43

The same test can be conducted at high frequencies by applying an input frequency slightly offset from $f_S/2$ as shown in Figure 12.42. This causes the ADC to slew fullscale between conversions. Every other conversion is compared, and the "beat" frequency is chosen such that there is slightly less than 1 LSB change between alternate samples. The equations for calculating the proper frequencies for the low and high frequency BER tests are given in Figure 12.43.

Establishing the BER of a well-behaved ADC is a difficult, time-consuming task; a single unit can sometimes be tested for days without an error. For example, tests on the AD9002 8 bit flash converter operating at a sampling rate of 75MSPS yield a BER of approximately 3.7×10^{-12} (1 error per hour) with an error limit of 4 LSBs. Meaningful tests for longer periods of time require special attention to EMI/RFI effects (possibly requiring a shielded screen room), isolated power supplies, etc.

BIT ERROR RATE (BER) FOR 75MSPS SAMPLING RATE

Bit Error Rate (BER)	Average Time Between Errors
1×10^{-8}	1.3 seconds
1×10^{-9}	13.3 seconds
1×10^{-10}	2.2 minutes
1×10^{-11}	22 minutes
1×10^{-12}	3.7 hours
1×10^{-13}	1.5 days
1×10^{-14}	15 days

Figure 12.44

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3. Christopher W. Mangelsdorf, *A 400-MHz Input Flash Converter with Error Correction*, **IEEE Journal of Solid-State Circuits**, Vol. 25, No. 1, February 1990, pp. 184-191.

4. Charles E. Woodward, *A Monolithic Voltage-Comparator Array for A/D Converters*, **IEEE Journal of Solid State Circuits**, Vol. SC-10, No. 6, December 1975, pp. 392-399.

5. Yukio Akazawa et. al., *A 400MSPS 8 Bit Flash A/D Converter*, **1987 ISSCC Digest of Technical Papers**, pp. 98-99.

6. A. Matsuzawa *et al.*, *An 8b 600MHz Flash A/D Converter with Multi-stage Duplex-gray Coding*, **Symposium VLSI Circuits, Digest of Technical Papers**, May 1991, pp. 113-114.

7. Ron Waltman and David Duff, *Reducing Error Rates in Systems Using ADCs*, **Electronics Engineer**, April 1993, pp. 98-104.

SECTION 13

INTERFACING TO HIGH SPEED ADCs

- DRIVING THE HIGH SPEED ADC INPUT AND GENERATING REFERENCE VOLTAGES
- CAPTURING HIGH SPEED ADC OUTPUT DATA
- DEMULTIPLEXING HIGH SPEED ADC OUTPUTS
- DEALING WITH 16-BIT PRECISION SAMPLING ADCs
- DATA OUTPUT CONSIDERATIONS FOR PRECISION SAMPLING DSP ADCs
- PROTECTING THE ADC INPUT FROM OVERDRIVE AND PREVENTING LATCHUP
- SAMPLING CLOCK GENERATION
- POWER SUPPLIES, GROUND PLANES, DECOUPLING, AND LAYOUT
- PROTOTYPING HIGH PERFORMANCE ANALOG CIRCUITRY

SECTION 13

INTERFACING TO HIGH SPEED ADCs

Walt Kester, James Bryant

In previous sections, the amplification and transmission of high speed signals has been discussed in detail. The important characteristics of ADCs were reviewed in order to aid in specifying the appropriate converter for the signal being processed. In this section we examine the actual ADC interface. In addition to the selection of the drive amplifier, there are a number of other issues which are important to the successful application of high speed ADCs.

The input to most high speed ADCs requires an appropriate drive amplifier to buffer the signal and provide gain and offset capability. The ADC user must be able to supply a clean sampling clock which controls the conversion rate. Some high speed monolithic ADCs require an external voltage reference. Proper techniques must be used to handle the ADC output data, especially at high rates. Finally, and probably the most important, good layout, signal routing, power supply generation and decoupling, and grounding techniques must be followed in order to achieve the specified performance levels required.

SUCCESSFUL SYSTEMS REQUIRE PROPER INTERFACING WITH THE ADC

- Selection of Drive Amplifier
- Supplying External Reference Voltage if Required
- Capturing ADC Output Data
- Generation of Sampling Clock
- Proper Layout and Signal Routing
- Power Supply Generation, Filtering, Decoupling
- Proper Use of Ground Planes and Grounding Techniques

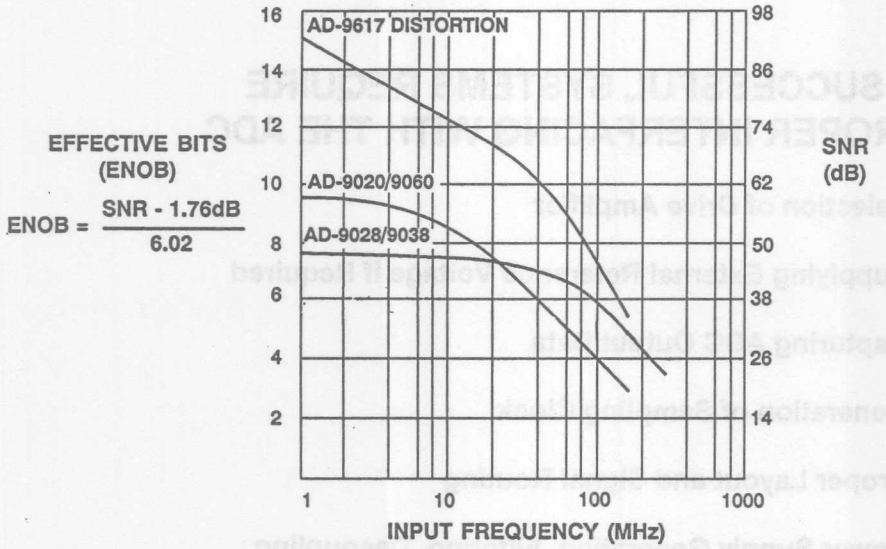
Figure 13.1

DRIVING THE HIGH SPEED ADC INPUT AND GENERATING REFERENCE VOLTAGES

Selecting the appropriate drive amplifier for a high speed ADC involves many of the considerations discussed in the section on amplification. The ac characteristics of ADCs are specified in terms of SNR, ENOBs, and distortion. The drive amplifier, therefore, should have a performance which is better than that of the ADC so that maximum dynamic performance is obtained. The second consideration involves understanding the analog input circuit of the ADC and its effect on the amplifier. Flash converters generally present a varying capacitive load to the amplifier which may cause instability. Subranging ADCs usually present rather benign loads to the drive amplifier because of their internal track-and-hold. Regardless of the ADC selected, the data sheet should always be consulted for recommended drive amplifiers.

High bandwidth, low distortion amplifiers such as the AD9617 are usually selected to drive high speed ADCs. Figure 13.2 shows the dynamic characteristics of two flash converters along with the distortion performance of the AD9617. Notice that the distortion performance of the AD9617 is better than the ADCs over the usable input bandwidths of the flash converters.

FLASH ADC AND OP AMP DYNAMIC PERFORMANCE



FLASH ADC	RESOLUTION	SAMPLING RATE
AD9020	10 BITS	40 MSPS
AD9060	10 BITS	60 MSPS
AD9028/9038	8 BITS	250 MSPS

Figure 13.2

We will now consider some of the other important high speed ADC interface considerations by examining a few actual application circuits.

A simplified block diagram of the AD9058 dual 8 bit, 50MSPS flash converter and an application diagram for a quadrature receiver is shown in Figure 13.3. The AD9058 is ideal for applications which require matched converters in order to achieve optimum performance. Since both ADCs are on the same chip, dc and ac matching are both excellent. The matching between the aperture delay of the two converters is better than 200ps. Crosstalk rejection between the two channels at 3MHz is greater than 50dBc. The AD9058 has an internal +2V reference voltage which makes the device easy to use. Low power (<1W max) makes the AD9058 a cost effective solution for systems requiring two or more ADCs.

SIMPLIFIED BLOCK DIAGRAM OF AD9058 DUAL 8-BIT, 50MSPS FLASH CONVERTER AND QUADRATURE RECEIVER APPLICATION

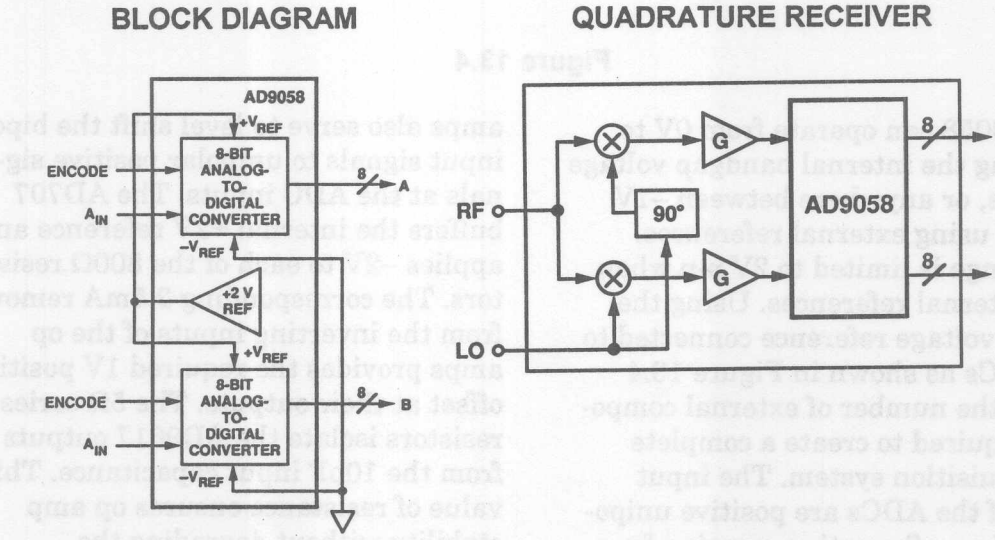


Figure 13.3

A typical interface circuit for the AD9058 is shown in Figure 13.4. The analog input range is established by the voltages applied at the voltage reference inputs $+V_{REFA}$, $+V_{REFB}$, and $-V_{REFA}$, $-V_{REFB}$. In applications requiring matched ADCs such as in quadrature receivers, $+V_{REFA}= +V_{REFB}$, and $-V_{REFA}= -V_{REFB}$. Because the reference voltages for each of the two ADCs are brought out on separate pins, it is possible to use different references for each of the two converters.

13

TYPICAL INTERFACE CIRCUIT FOR THE AD9058 DUAL FLASH CONVERTER USING INTERNAL VOLTGAGE REFERENCE

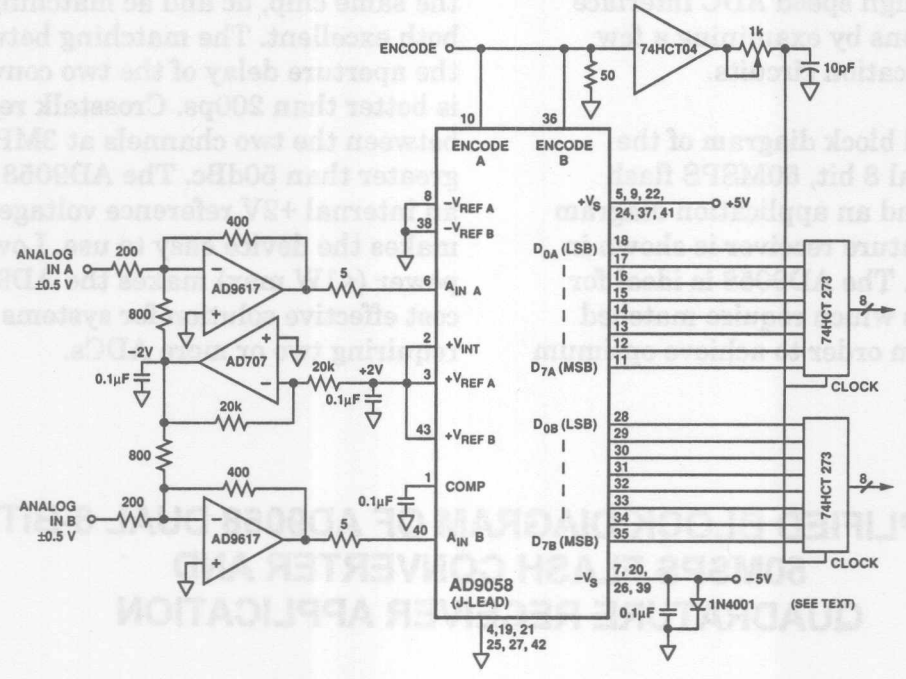


Figure 13.4

The AD9058 can operate from 0V to +2V using the internal bandgap voltage reference, or anywhere between –1V and +2V using external references. Input range is limited to 2V p-p when using external references. Using the internal voltage reference connected to both ADCs as shown in Figure 13.4 reduces the number of external components required to create a complete data acquisition system. The input ranges of the ADCs are positive unipolar in this configuration, ranging from 0V to +2V. The temperature coefficient of the internal reference is typically 150µV/°C which limits the drift to 11mV (1.4LSBs) over a 0 to +70°C temperature range.

A good low distortion amplifier such as the AD9617 (–67dBc at 20MHz) is used to buffer and amplify the signal to each ADC. The diagram shows that the bipolar signals of ±0.5V are amplified to 2V p-p by the pair of AD9617s. The op amps also serve to level shift the bipolar input signals to unipolar positive signals at the ADC inputs. The AD707 buffers the internal +2V reference and applies –2V to each of the 800Ω resistors. The corresponding 2.5mA removed from the inverting inputs of the op amps provides the required 1V positive offset at their outputs. The 5Ω series resistors isolate the AD9617 outputs from the 10pF input capacitance. This value of resistance ensures op amp stability without degrading the 175MHz input bandwidth of the AD9058.

The diode shown between ground and $-V_S$ is normally reverse biased and is used to prevent latchup. Its use is recommended for applications in which power supply sequencing might allow $+V_S$ to be applied before $-V_S$; or the $+V_S$ supply is not current limited. If the negative supply is allowed to float (the +5V supply is powered up before the

–5V supply), substantial +5V supply current will attempt to flow through the substrate (+V_S supply contact) to ground. If this current is not limited to <500mA, the device may be destroyed. The diode prevents this potentially destructive condition from occurring.

The AD9058 may be used with external references as shown in Figure 13.5, where both inputs to the AD9058 are configured for ±1V operation. The AD580 provides an external +2.5V reference with a temperature coefficient as low as 25µV/°C for the M-grade. This limits the overall temperature drift of the reference to about 2mV (0.25LSBs) over the 0 to +70°C temperature range. The 10kΩ potentiometers allow independent adjustment of the positive and negative reference voltages. The dual AD708 low-drift op amp along with the 2N3904 and 2N3906 transistors are used to buffer the potentiometer outputs to the AD9058 reference voltage inputs. The lower half of the AD708 inverts the polarity to supply the negative reference. The ±0.125V input signals are amplified by the low-distortion AD9618 op amps configured for a gain of 8.

AD9058 INTERFACE CIRCUIT USING EXTERNAL VOLTAGE REFERENCE

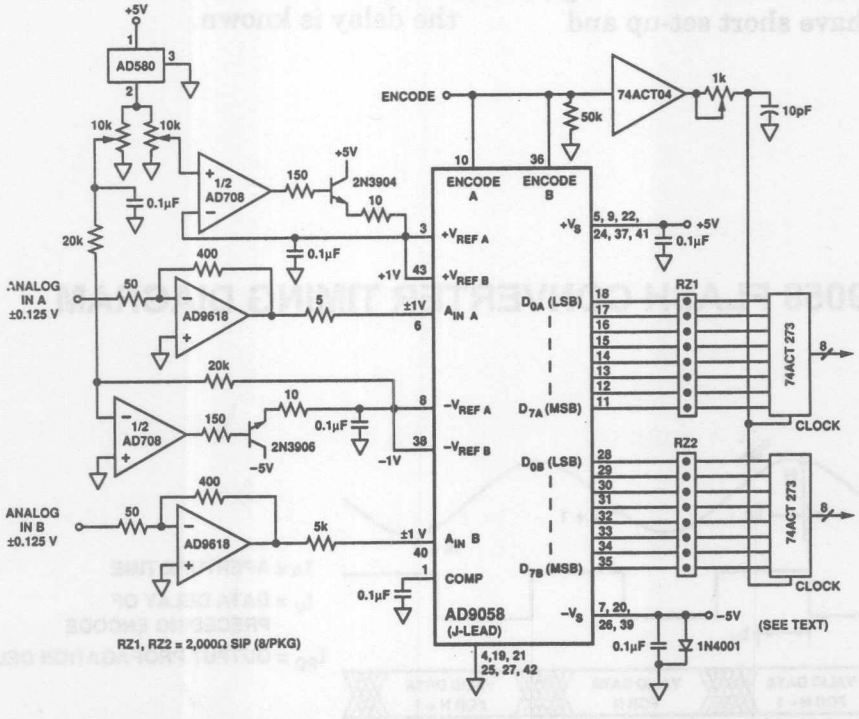


Figure 13.5

CAPTURING HIGH SPEED ADC OUTPUT DATA

A timing diagram for the AD9058 is shown in Figure 13.6. The AD9058 provides latched data outputs with no pipeline delay. To conserve power and reduce internal signal-dependent noise, the parallel data outputs have relatively slow rise and fall times. When designing system timing, it is important to observe set-up and hold times on the external latches; and the intervals when the ADC output data is changing.

Figure 13.5 shows 2kΩ pull-down resistors on each of the D_0 - D_7 output data bits. When operating at conversion rates higher than 40MSPS, these resistors help equalize rise and fall times and ease latching the output data into external latches. The 74ACT logic family devices have short set-up and hold times and are the recommended choices for speeds of 40MSPS or greater. The latch strobe may generated from the sampling clock by adding sufficient delay (if required) to center the latch strobe edge at the midpoint of the data-valid region.

Many flash converters and other ADCs, such as the AD9048 8 bit, 35MSPS ADC have one or more built-in pipeline delays associated with the output data. The block diagram of the AD9048 in Figure 13.7 shows an internal latch following the encoding logic. This latch introduces a one-clock-cycle pipeline delay, or *latency* in the output data as shown in Figure 13.8. This should not be a problem in most systems as long as the delay is known.

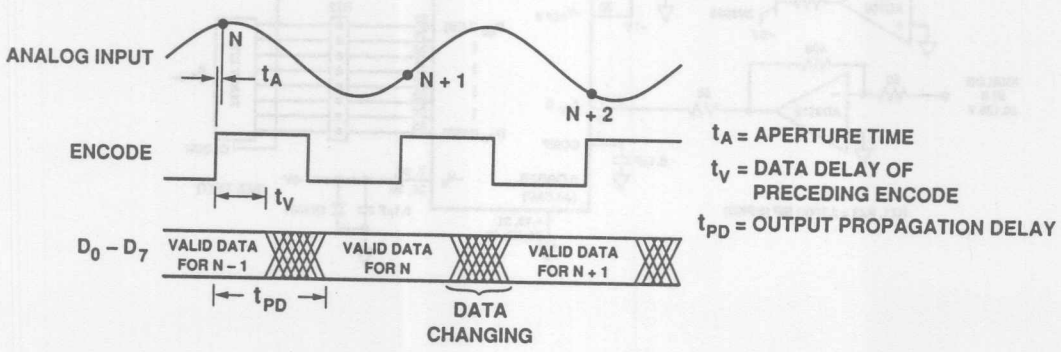


Figure 13.6

AD9048 8-BIT, 35MSPS FLASH CONVERTER HAS ONE CLOCK-CYCLE PIPELINE DELAY IN THE OUTPUT DATA DUE TO THE INTERNAL LATCH

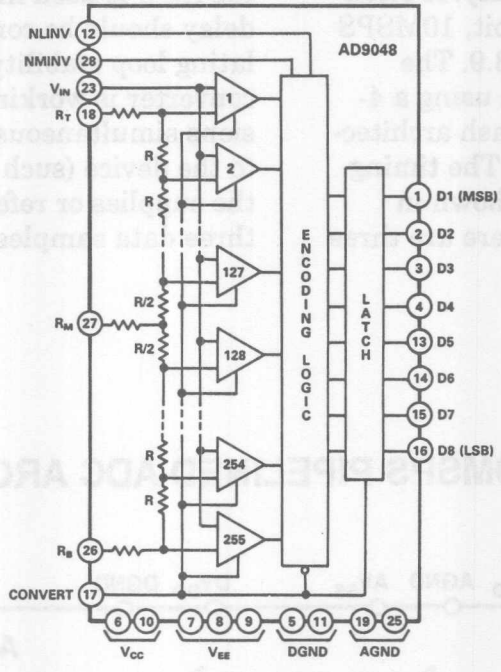


Figure 13.7

AD9048 TIMING DIAGRAM SHOWS PIPELINE DELAY (LATENCY) IN THE OUTPUT DATA

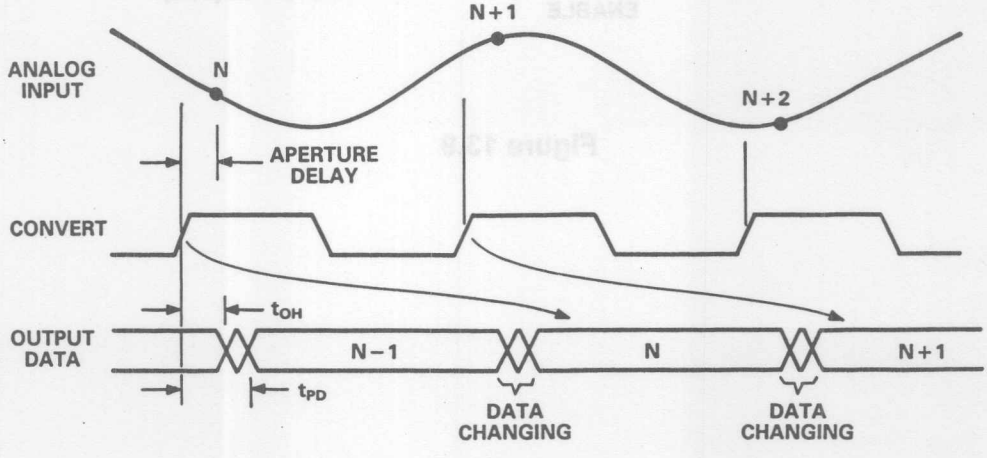


Figure 13.8

Some subranging ADCs, in fact, have several clock cycles of latency. A block diagram of the AD872 12 bit, 10MSPS ADC is shown in Figure 13.9. The conversion is implemented using a 4-stage pipelined multiple flash architecture with error correction. The timing diagram for the device is shown in Figure 13.10. Note that there are three clock-cycle delays in the output data. If the ADC is used inside a servo loop this delay should be considered when calculating loop stability. Also, because the converter is working on three conversions simultaneously, major disruptions to the device (such as a large glitch on the supplies or reference) may corrupt three data samples.

AD872 12-BIT, 10MSPS PIPELINED ADC ARCHITECTURE

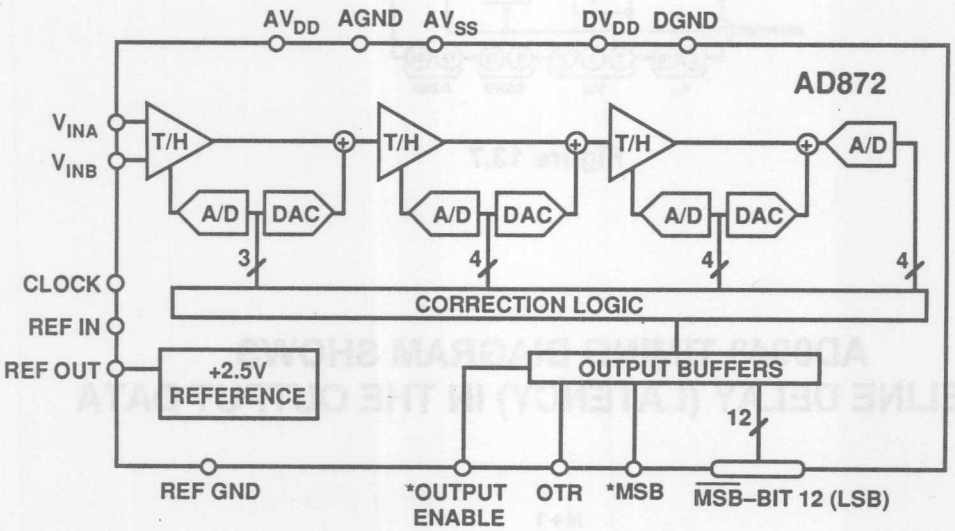


Figure 13.9

AD872 TIMING DIAGRAM SHOWS 3 CLOCK-CYCLE LATENCY

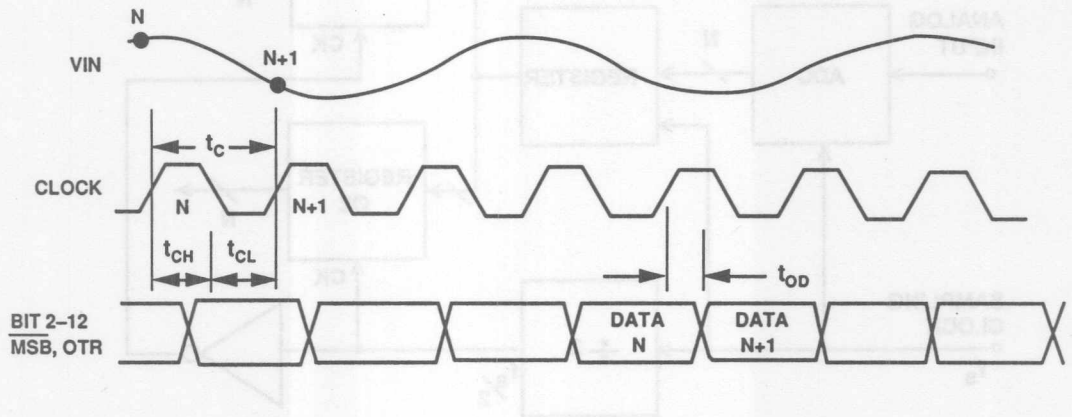


Figure 13.10

DEMULTIPLEXING HIGH SPEED ADC OUTPUTS

In most high speed applications, the output data from the ADC must be downloaded into a buffer memory for further processing. In order to avoid costly high speed, high power memory, the demultiplexing scheme shown in Figure 13.11 may be used to reduce the data output rate. This will allow low cost CMOS memory to be used for storage of the bulk of the data.

High speed flash converters may provide on-chip demultiplexing for easing the requirements on the buffer memory interface. For example, the AD9032 8 bit, 300MSPS ADC is presented to the output of the ADC on two 8 bit ports. The data rate for each port is therefore 150MSPS for a sampling clock frequency of 300MSPS. The data on each port can be further demultiplexed externally for eventual storage in CMOS memory.

DEMULTIPLEXING HIGH SPEED ADC OUTPUTS FOR STORAGE IN SLOWER MEMORIES

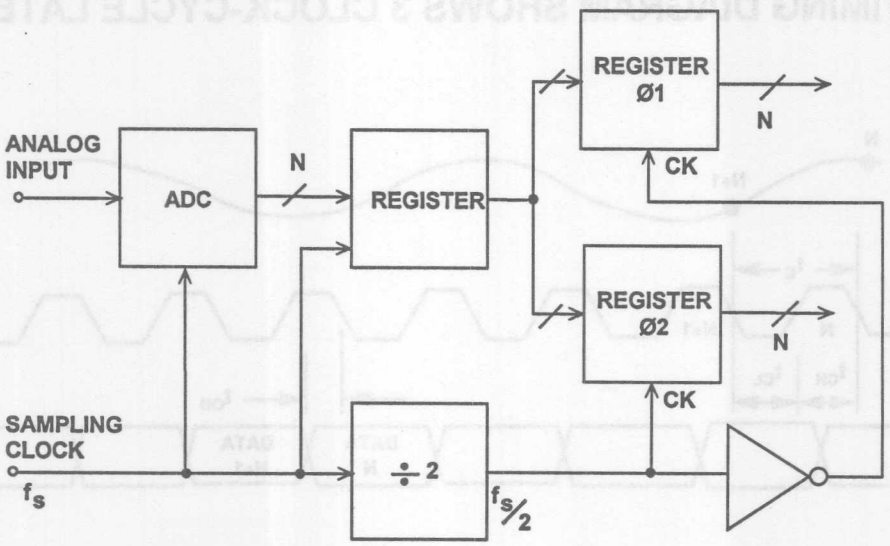


Figure 13.11

DEALING WITH 16-BIT PRECISION SAMPLING ADCS

ADCs with 16-bit resolution and sampling rates of 100kSPS or more have become very popular in real-time DSP applications. These converters present special challenges to the design engineer because they combine all the problems associated with high-speed and wide bandwidth with those problems associated with dc precision. Achieving low noise performance is perhaps the biggest challenge.

An example of a 16-bit sampling ADC is the AD7884/AD7885 166kSPS converter shown in Figure 13.13. The ADC contains an internal SHA and utilizes a recursive subranging architecture with digital error correction. Power dissipation is 250mW. The AD7884 has a 16-bit parallel output structure, while the AD7885 has a byte reading structure. Typical dynamic performance (FFT output and ENOB) is shown in Figure 13.14.

16-BIT SAMPLING ADCs

- Same Issues As High Speed ADCs: Grounding, Layout, Etc.
- Noise May Greatly Impair Performance @ 16 Bits
- Autocalibration Usually Required to Maintain Accuracy Over Extended Temperature Ranges
- Monolithic Solutions Require External Support Circuitry: Voltage References, Input Buffers, Clock Generators
- High Performance Hybrids Offer Complete Solutions at Higher Cost And Power

Figure 13.12

AD7884 16-BIT, 166kSPS ADC BLOCK DIAGRAM

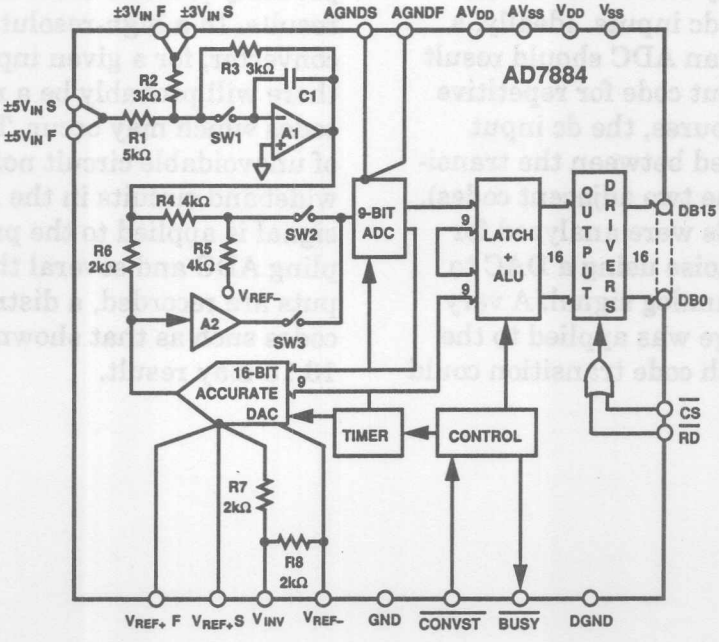


Figure 13.13

AD7884 / AD7885 ADC FFT OUTPUT AND EFFECTIVE BIT PERFORMANCE

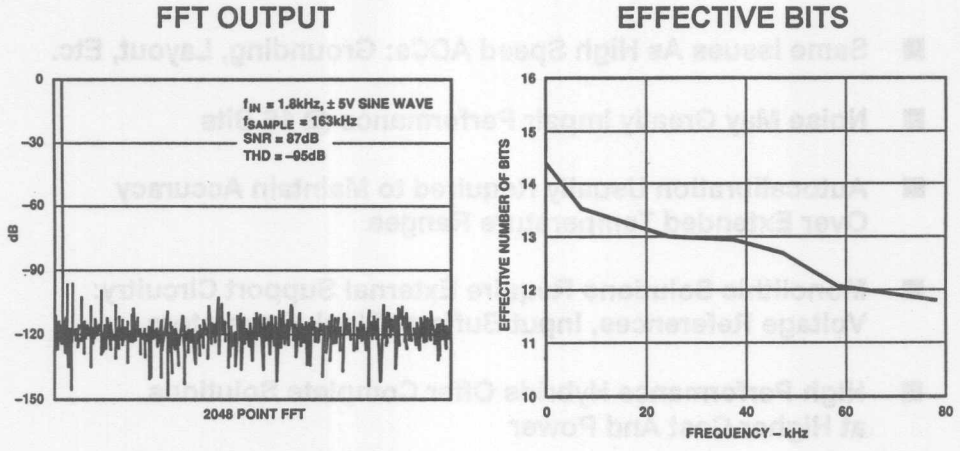


Figure 13.14

Precision 16-bit sampling ADCs such as the AD7884/AD7885 may very well behave differently from their 12-bit counterparts for dc inputs. Ideally, a fixed dc input to an ADC should result in the same output code for repetitive conversions (of course, the dc input should be centered between the transition regions of the two adjacent codes). In the past, ADCs were analyzed for code transition noise using a DAC to reconstruct the analog signal. A very slow ramp voltage was applied to the ADC, so that each code transition could be observed. With a precision 16-bit sampling ADC, however, this test will probably produce some unfamiliar results. In a high-resolution sampling converter, for a given input voltage, there will probably be a range of output codes which may occur. This is because of unavoidable circuit noise within the wideband circuits in the ADC. If a dc signal is applied to the precision sampling ADC and several thousand outputs are recorded, a distribution of codes such as that shown in Figure 13.15 may result.

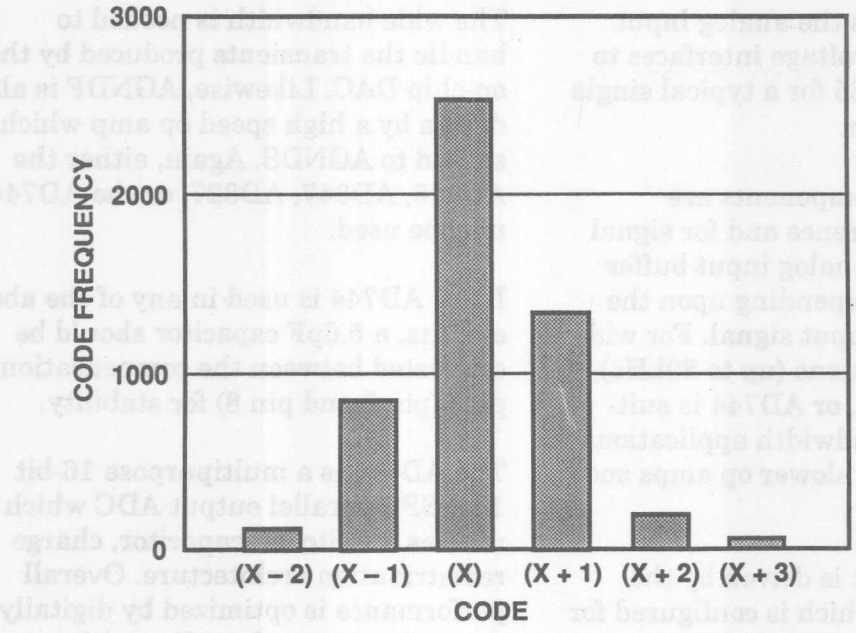


Figure 13.15

The correct code appears most of the time, but adjacent codes appear as well with reduced probability. If a Gaussian probability distribution is fitted to the histogram, the standard deviation is approximately equivalent to the equivalent input rms noise of the ADC. The actual specification on the ADC data sheet may be given in terms of a histogram or may be converted into an equivalent input rms noise voltage. In Figure 13.15, the peak-to-peak noise is about 5 LSBs, corresponding to 5/6 = 0.8 LSBs rms (Peak-to-peak values may be converted into rms values by dividing by 6). For a 6V peak-to-peak input range, this corresponds to 74μV rms equivalent input noise.

This noise may come from several sources. For example, a 1MΩ resistor generates 158μV rms noise over a 1MHz single-pole bandwidth (the equivalent noise bandwidth is 1.57MHz). One LSB for the AD7884 operating with a 6V peak-to-peak input range is 92μV. This illustrates the importance of keeping the source impedances low. Some of the internal ADC noise is generated in the wideband SHA. Sampling ADCs generally have input bandwidths which exceed the Nyquist frequency of one-half the sampling rate. (The AD7884/AD7885 has an input bandwidth which exceeds 1MHz, even though the maximum sampling rate is 166kSPS). These wide bandwidth front ends are required in order to minimize gain and phase distortion at the signal frequencies. A certain amount of unavoidable noise is generated in the SHA and the other wideband circuits within the ADC which cause the sample-to-sample variation in output codes for dc inputs. In addition, good layout, grounding, and decoupling techniques are essential to prevent additional external noise from coupling into the ADC adding to the inherent equivalent input noise.

The AD7884/AD7885 ADC is designed to operate with an external low noise +3V reference such as the AD780. Figure 13.16 shows the analog input and the reference voltage interfaces to the AD7884/AD7885 for a typical single channel application.

Several external components are needed for the reference and for signal conditioning. The analog input buffer should be chosen depending upon the bandwidth of the input signal. For wide bandwidth applications (up to 80kHz), the AD845, AD847, or AD744 is suitable. For lower bandwidth applications it is possible to use slower op amps such as the AD711.

The VREF(+) input is driven by the AD780 reference which is configured for a 3V output range. The AD780 output is decoupled directly to ground with a 10µF capacitor to absorb the transient voltages generated by the on-chip DAC.

The VREF(–) input is driven with a high speed amplifier like the AD845, AD847, AD827 (dual), or the AD744. The wide bandwidth is needed to handle the transients produced by the on-chip DAC. Likewise, AGNDF is also driven by a high speed op amp which is sensed to AGNDS. Again, either the AD845, AD847, AD827, or the AD744 may be used.

If the AD744 is used in any of the above circuits, a 5.6pF capacitor should be connected between the compensation pins (pin 5 and pin 8) for stability.

The AD676 is a multipurpose 16-bit 100kSPS parallel output ADC which utilizes a switched-capacitor, charge redistribution architecture. Overall performance is optimized by digitally correcting internal nonlinearities through on-chip autocalibration. A block diagram of the AD676 is shown in Figure 13.17.

INPUT AND REFERENCE INTERFACE TO THE AD7884/AD7885

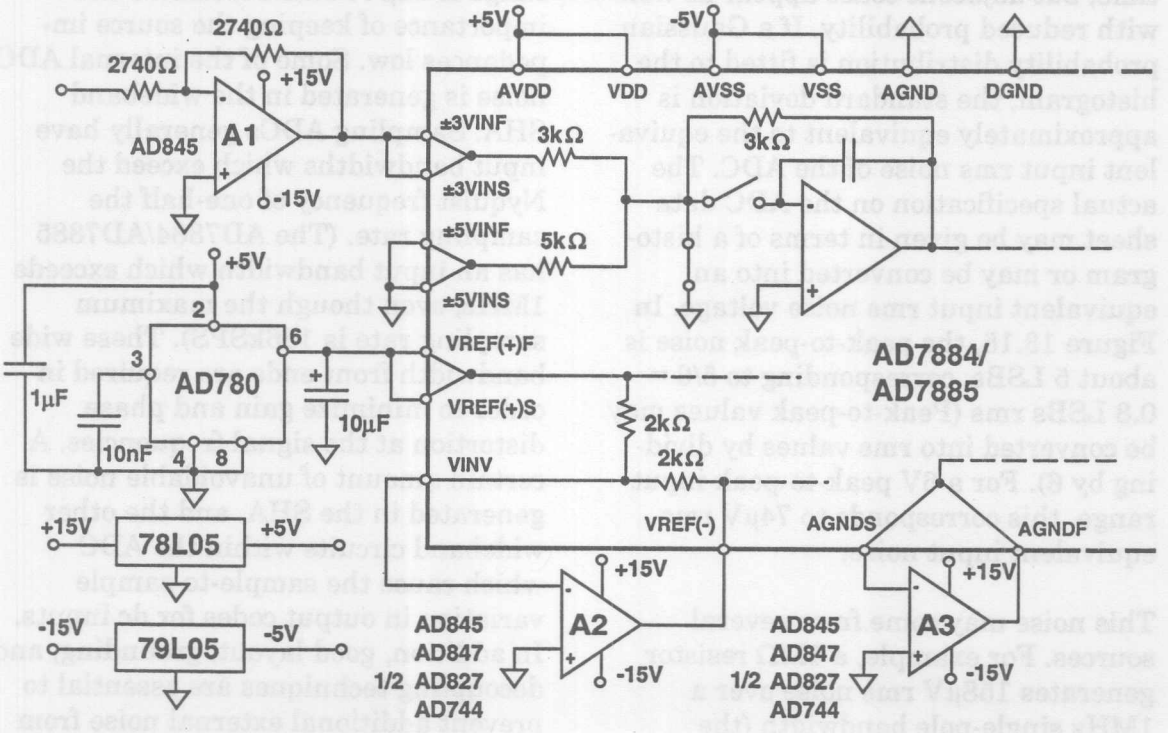


Figure 13.16

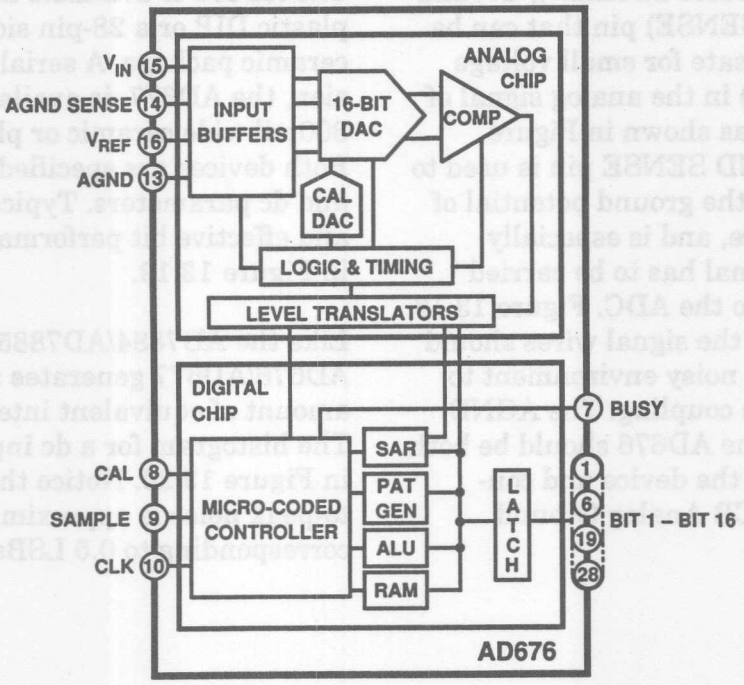


Figure 13.17

The AD676/AD677 employs a successive approximation technique to determine the value of the analog input voltage. However, instead of the traditional laser trimmed resistor ladder approach, this device uses a capacitor array, charge redistribution technique. Binary-weighted capacitors subdivide the input sample to perform the actual analog to digital conversion. The capacitor array eliminates variation in the linearity of the device due to temperature-induced mismatches of resistor values. Since a capacitor array is used to perform the data conversion, the SHA function is included without the need for additional circuitry.

Initial errors in capacitor matching are eliminated by an autocalibration circuit. This circuit employs an on-chip microcontroller and a calibration DAC to measure and compensate capacitor mismatch errors. In the calibration mode, each individual code (65,536 total) is checked for INL and DNL errors. When an error is detected, a correction value is stored in RAM. In normal operation, the ADC actually outputs the coded input plus the correction factor for that output code. The autocalibration routine may be invoked at any time. The complete autocalibration cycle requires approximately 50ms when sampling at 100kSPS. Autocalibration ensures high performance while eliminating the need for any user adjustments.

Designing with high resolution ADCs requires careful attention to board layout. Trace impedance is a significant issue. A 1.22mA current through a 0.5Ω trace will develop a voltage drop of 0.6mV, which is 4 LSBs at the 16-bit level for a 10V fullscale span.

The AD676 provides an Analog Ground Sense (AGND SENSE) pin that can be used to compensate for small voltage drops (<100mV) in the analog signal of the return line as shown in Figure 13.18. The AGND SENSE pin is used to remotely sense the ground potential of the signal source, and is especially useful if the signal has to be carried some distance to the ADC. Figure 13.18 also shows how the signal wires should be shielded in a noisy environment to avoid capacitive coupling. The AGND and DGND of the AD676 should be both tied together at the device and connected to the PCB Analog Ground Plane.

The AD676 is available in a 28-pin plastic DIP or a 28-pin side-brazed ceramic package. A serial output version, the AD677, is available in a 16-pin 300mil wide ceramic or plastic package. Both devices are specified for both ac and dc parameters. Typical S/(N+D) and effective bit performance is shown in Figure 13.19.

Like the AD7884/AD7885 ADC, the AD676/AD677 generates a certain amount of equivalent internal noise. The histogram for a dc input is shown in Figure 13.20. Notice that the peak-to-peak noise is approximately 3 LSBs, corresponding to 0.5 LSBs rms.

AD676 AGND SENSE PIN CONNECTIONS FOR SHIELDED TWISTED PAIR CABLE

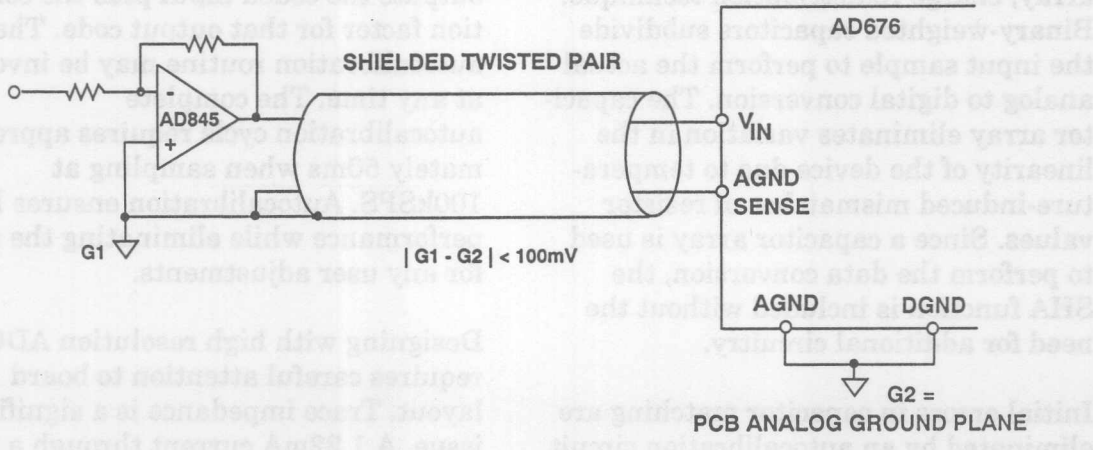


Figure 13.18

AD676 16-BIT, 100kSPS SAMPLING ADC S/N + D AND EFFECTIVE BIT PERFORMANCE

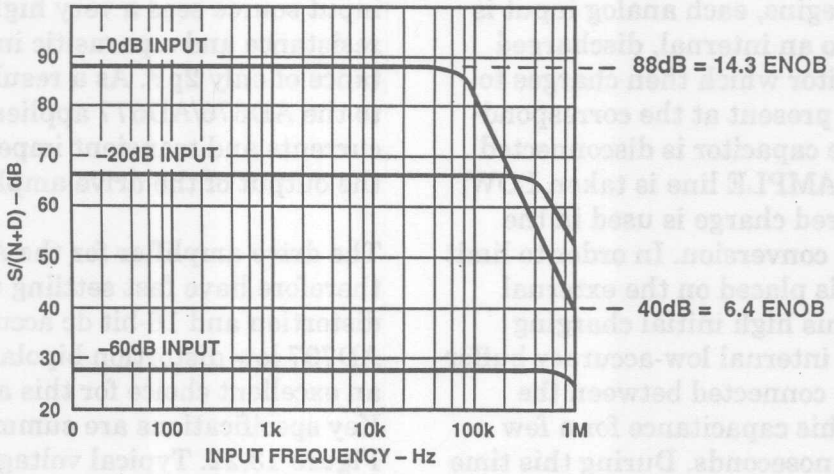


Figure 13.19

AD676 DISTRIBUTION OF CODES FROM 1000 CONVERSIONS FOR A DC INPUT SHOWS 3 LSBs p-p, OR 0.5 LSBs RMS EQUIVALENT INPUT NOISE

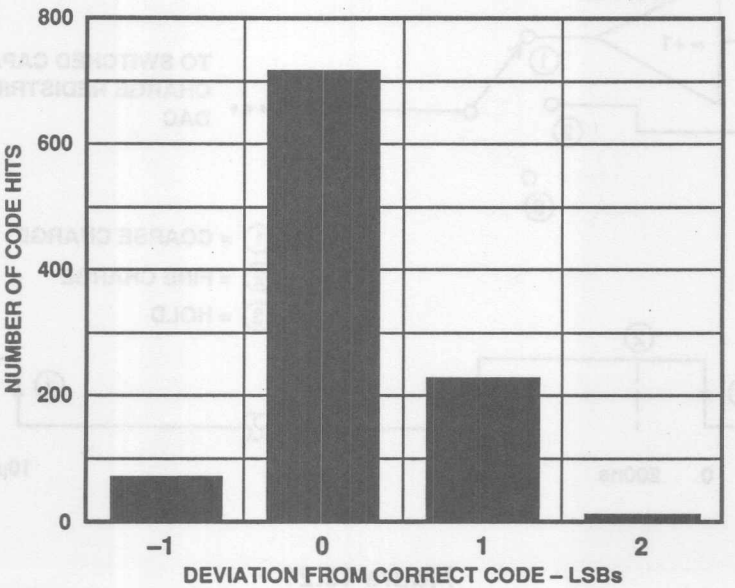


Figure 13.20

13

A simplified schematic of the input circuit of the AD676 is shown in Figure 13.21. All of the inputs (V_{in}, V_{ref}, and AGND SENSE) produce transient load currents which must be absorbed by their respective drivers. When a conversion cycle begins, each analog input is connected to an internal, discharged 50pF capacitor which then charges to the voltage present at the corresponding pin. The capacitor is disconnected when the SAMPLE line is taken LOW, and the stored charge is used in the subsequent conversion. In order to limit the demands placed on the external source by this high initial charging current, an internal low-accuracy buffer amplifier is connected between the input and this capacitance for a few hundred nanoseconds. During this time the input pin exhibits typically 20kΩ | | 10pF and ±40μA bias current.

Next, the input is switched directly to the now precharged capacitor and allowed to fully settle. During this time, the input appears as a 50pF capacitor. Once the sample is taken, the input is internally floated so that the external input source sees a very high input resistance and a parasitic input capacitance of only 2pF. As a result, the input to the AD676/AD677 applies transient currents and transient impedances to the output of the drive amplifer.

The drive amplifier for the AD676 must therefore have fast settling time, low distortion and 16-bit dc accuracy. The AD797 low distortion bipolar op amp is an excellent choice for this application. Key specifications are summarized in Figure 13.22. Typical voltage noise and THD are shown in Figure 13.23.

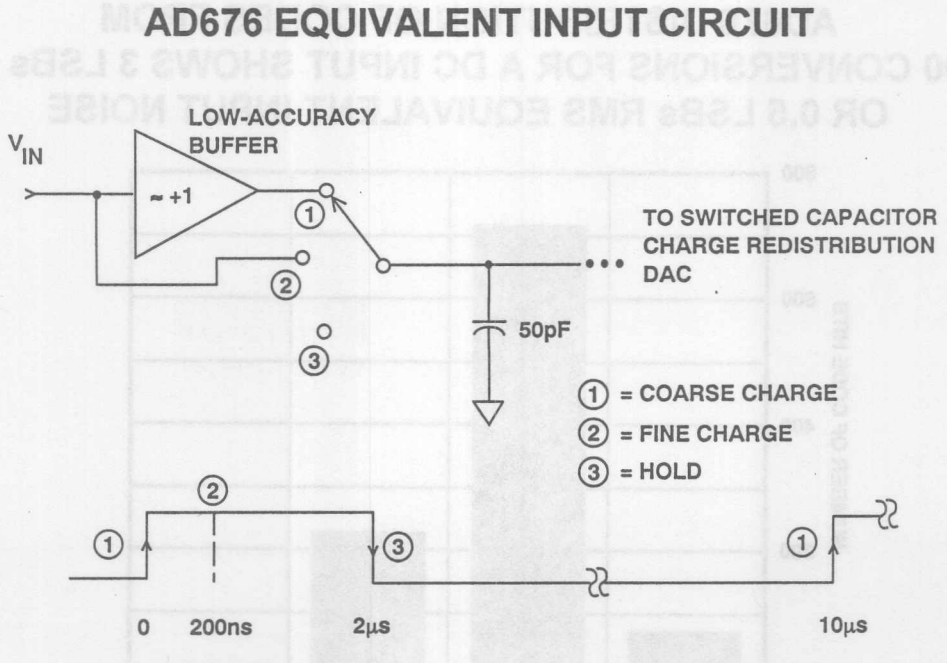


Figure 13.21

AD797 PRECISION LOW DISTORTION BIPOLAR OP AMP KEY SPECIFICATIONS

- 0.1mV Input Offset Voltage
- 0.2μV/°C Offset Voltage Drift
- 100nA Input Offset Current
- 1,000,000 dc Open Loop Gain
- 100MHz Gain Bandwidth Product
- 110dB THD @ 20kHz, 3Vrms into 600Ω
- 0.9nV/$\sqrt{Hz}$, 2pA/$\sqrt{Hz}$ Input Noise at 1kHz

Figure 13.22

AD797 ULTRA-LOW-NOISE OP AMP VOLTAGE NOISE AND THD PERFORMANCE

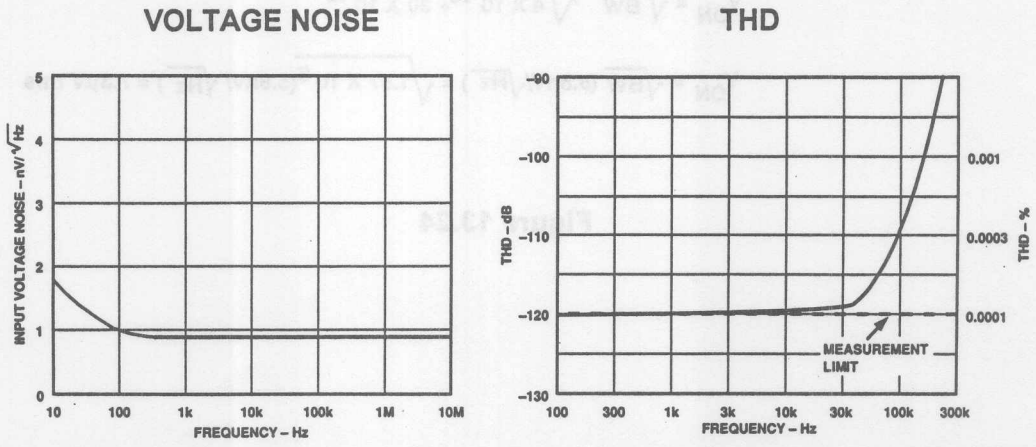
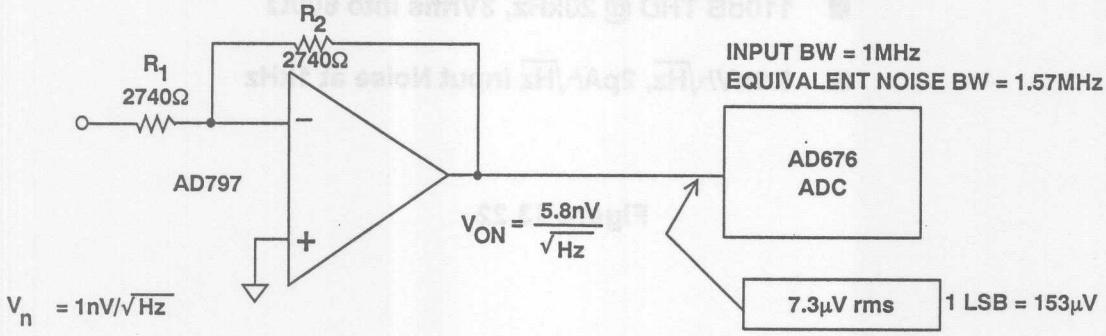


Figure 13.23

Figure 13.24 shows the calculations for the total output noise of the AD797 over the 1MHz input bandwidth of the AD676. The total noise is computed to be only 7μV rms compared to the theoretical 16-bit quantization noise (10V fullscale range) of 44μV rms.

If the application requires a FET input amplifier, the AD845 may be used as a drive amplifier for the AD676 yielding a total output noise of 30μV rms as shown in Figure 13.25.

NOISE CALCULATIONS FOR AD797 DRIVING AD676 16-BIT, 100kSPS ADC



$V_n = 1nV/\sqrt{Hz}$

$I_n = 2pA/\sqrt{Hz}$

$$V_{ON} = \sqrt{BW}\sqrt{V_n^2\left[1+\frac{R_2}{R_1}\right]^2 I_{n-}^2 R_2^2}$$

$$V_{ON} = \sqrt{BW}\sqrt{(1\times10^{-9})^2(2)^2+(2\times10^{-12})^2(2740)^2}$$

$$V_{ON} = \sqrt{BW}\sqrt{4\times10^{-18}+30\times10^{-18}}$$

$$V_{ON} = \sqrt{BW}\,(5.8nV/\sqrt{Hz}) = \sqrt{1.57\times10^6}(5.8nV/\sqrt{Hz}) = 7.3\mu V\ rms$$

Figure 13.24

AD845 DRIVING AD676 16-BIT, 100kSPS ADC

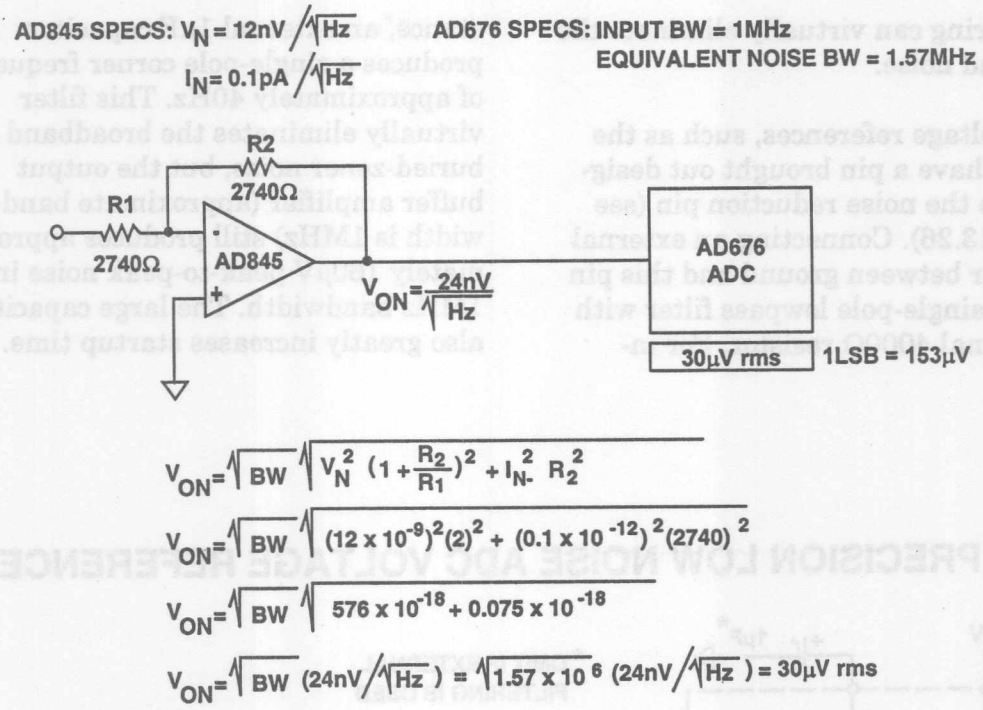


Figure 13.25

Both the AD7884/AD7885 and the AD676/AD677 ADCs require an external voltage reference. This is because the IC processes which are typically used for precision sampling converters do not support 16-bit accurate (or better) voltage reference circuits. The reference voltage establishes the fullscale range of the ADC, and the overall dc accuracy and stability of the ADC can be no better than that of the reference. Standard monolithic reference voltage values are 2.5V and 3V (AD780), and 5V (AD586) and 10V (AD587).

The entire voltage reference function is available in ICs which utilize laser trimmed thin film resistors for excellent accuracy and low drift. Standard dc specifications for such a voltage reference are output current capability, line regulation, load regulation, output voltage tolerance, and output voltage change with temperature. AC specifications include turn-on settling time, transient load current settling time, and noise. Selecting voltage references based on dc requirements is relatively straightforward. Evaluating its noise performance deserves further discussion because noise on the ADC reference voltage input usually translates directly into increased internal noise levels and degraded SNR performance.

Most voltage references specify peak-to-peak noise in a 0.1Hz to 10Hz bandwidth. For instance, the AD586 (a 5V buried zener reference with on-chip output buffer) specification in this bandwidth is 4μV peak-to-peak. In most sampling ADC applications, however, the wideband noise is usually of more concern. For the AD586, the unfiltered noise in a 1MHz bandwidth is approximately 200μV peak-to-peak, corresponding to 200/6 = 33μV rms. This value is usually larger for bandgap voltage references such as the REF-02 (800μV peak-to-peak). Regardless of the type of reference chosen, proper exter-

nal filtering can virtually eliminate the wideband noise.

Some voltage references, such as the AD586, have a pin brought out designated as the noise reduction pin (see Figure 13.26). Connecting an external capacitor between ground and this pin forms a single-pole lowpass filter with an internal 4000Ω resistor. For instance, an external 1μF capacitor produces a single-pole corner frequency of approximately 40Hz. This filter virtually eliminates the broadband buried-zener noise, but the output buffer amplifier (approximate bandwidth is 1MHz) still produces approximately 160μV peak-to-peak noise in the 1MHz bandwidth. The large capacitor also greatly increases startup time.

PRECISION LOW NOISE ADC VOLTAGE REFERENCE

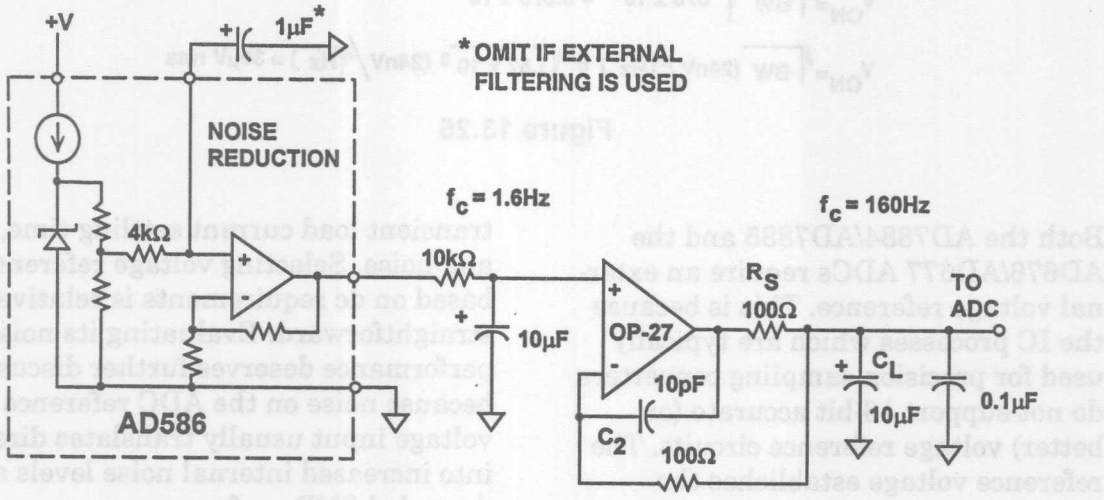


Figure 13.26

If low noise is required, adding a large capacitor on the reference output (10μF) will reduce the noise. This, however, may not produce the expected results for two reasons. First, the voltage reference output buffer amplifier has a low closed-loop output impedance on the order of a few ohms at low frequencies. The additional large capacitor does little to reduce this impedance further. Second, loading the output of the internal op amp with a large capacitor may cause the op amp to become unstable and to oscillate or ring under transient load conditions. (This is not the case with the AD780 2.5V/3V reference which is designed to be stable regardless of the capacitive load).

The ideal solution in precision applications is to use an external filter such as the one shown in Figure 13.26. The 10kΩ resistor and the 10μF capacitor form a single-pole passive filter which has a corner frequency of 1.6Hz, and reduces the noise to approximately the value specified in the 0.1 to 10Hz frequency band (4μV peak-to-peak for

the AD586 and the AD780). This passive filter is followed by a precision low noise buffer amp such as the OP-27 (V_n= 3nV/√Hz). The large load capacitor (C_L = 10μF) serves two purposes. First, it forms a lowpass filter with R_S having a corner frequency of approximately 160Hz. This reduces the output voltage noise of the op amp to a negligible value. Second, it provides additional reference voltage stability by acting as a charge reservoir to any transient load current. This amount of capacitance is a heavy load on any op amp; therefore, R_S and C_2 compensate for the pole introduced by C_L and the op amp's output resistance. This compensation scheme ensures that the buffer circuit recovers and settles from the output transients quickly without the long settling tails that might produce conversion errors. The 0.1μF capacitor in parallel with C_L is to keep the output impedance low at high frequencies, where the large 10μF electrolytic capacitor becomes less effective. When using external filtering, do not decouple the noise reduction pin with a capacitor. The capacitor will increase the refrence startup time.

In applications where filtering the voltage reference noise is not required, the decoupling capacitors on the ADC reference voltage input terminal may be eliminated completely. Simply buffer the voltage reference output with a precision low noise high bandwidth amplifier which has sufficient transient load settling time, such as the AD845 as shown in Figure 13.27. This approach will minimize the need for additional components, but dc precision and noise performance will be sacrificed.

WIDEBAND BUFFER AMPLIFIER ELIMINATES THE NEED FOR LARGE DECOUPLING CAPACITORS

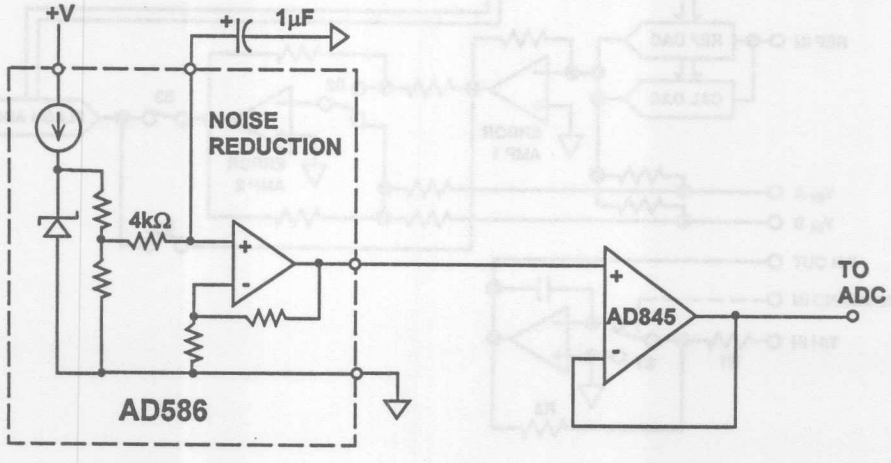


Figure 13.27

The AD1385 is a 16 bit, 500kSPS hybrid sampling ADC which contains on-board autocalibration circuits. The device is both ac and dc specified over the full temperature range of –55°C to +125°C. A block diagram of the device is shown in Figure 13.28.

The AD1385 architecture includes a low noise, low distortion track/hold, a three pass digitally corrected subranging ADC, and autocalibrating circuitry for excellent linearity. A complete linearity calibration requires 15ms. Precision thin film resistors and a proprietary DAC contribute to the outstanding dynamic and static performance. The AD1382 is a similar device, but is factory calibrated to meet full specifications from +10°C to +40°C.

Figure 13.29 shows the FFT output of the AD1385 at 25°C before and after autocalibration. Recalibration is recommended whenever the device's temperature has changed by more than 15°C. Performance degrades gracefully with temperature changes, resulting in small but gradual decreases in SNR and increases in distortion which may be eliminated by recalibration. The first FFT plot in Figure 13.30 was obtained by calibrating the AD1385 at +25°C and then elevating the case temperature to +125°C. The second FFT plot shows the AD1385 performance after recalibration at +125°C.

AD1385 16-BIT, 500kSPS ADC BLOCK DIAGRAM

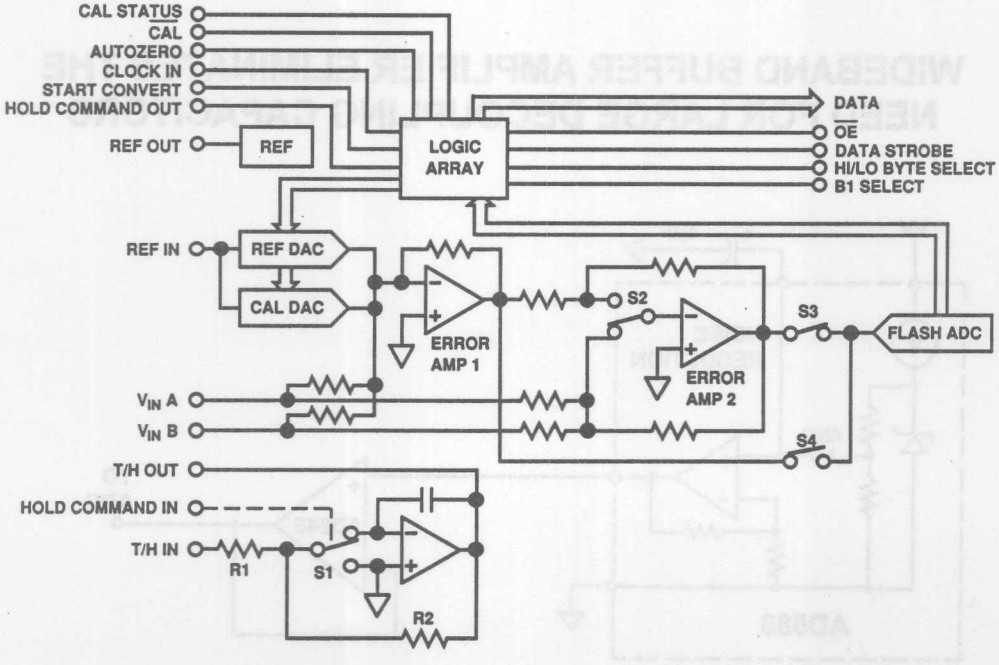
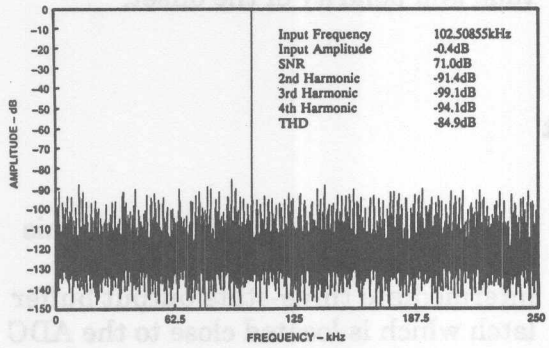


Figure 13.28

AD1385 ADC FFT OUTPUT AT +25°C BEFORE AND AFTER AUTO-CALIBRATION

BEFORE



AFTER

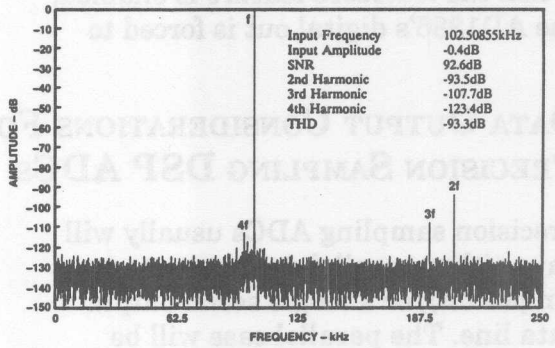
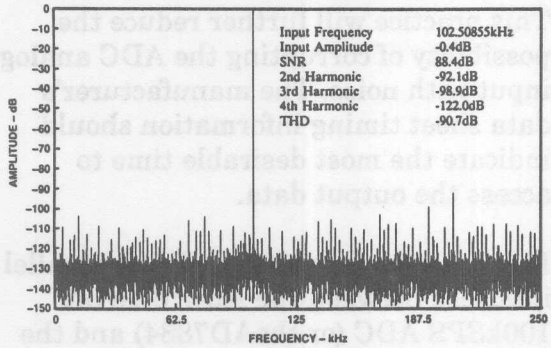


Figure 13.29

AD1385 ADC FFT OUTPUT AT +125°C BEFORE AND AFTER AUTO-CALIBRATION

BEFORE



AFTER

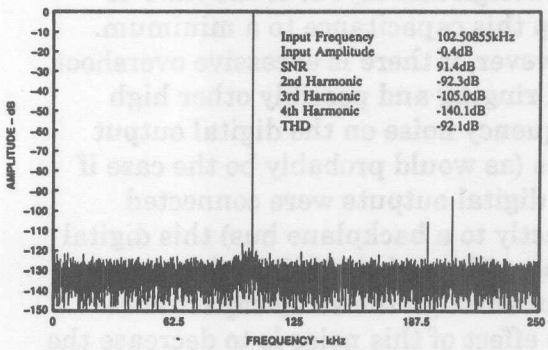


Figure 13.30

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The AD1385 also has an Autozero function which may be used to digitally correct internal offsets in the track/hold and the ADC circuit. To use the Autozero function, the track/hold input must be connected to a zero reference prior to the zeroing conversion. This connection is external to the AD1385 and must be provided by the user. When the Autozero feature is enabled, the AD1385's digital out is forced to indicate exactly zero when its input is at the zero point, nominally 0V. Autozero operates by storing the digital result of a zeroing conversion and subtracting it from all subsequent conversion results. This reduces the maximum nonsaturating input of the AD1385 by a small amount at one end of its range depending on the magnitude and polarity of the offset.

DATA OUTPUT CONSIDERATIONS FOR PRECISION SAMPLING DSP ADCS

Precision sampling ADCs usually will have either parallel data outputs (one pin per bit), or a single serial output data line. The parallel case will be considered first.

Many parallel output sampling ADCs offer three-state outputs which can be enabled or disabled using an *output enable* pin on the IC. While it may be tempting to connect these three-state outputs directly to a backplane data bus, severe performance-degrading noise problems may result for the following reasons. All ADCs have a small amount of internal stray capacitance between the digital outputs and the analog input (typically 0.1 to 0.5pF). Every attempt is made during the design and layout of the ADC to keep this capacitance to a minimum. However, if there is excessive overshoot and ringing and possibly other high frequency noise on the digital output lines (as would probably be the case if the digital outputs were connected directly to a backplane bus) this digital noise will couple back into the analog input through the stray capacitance. The effect of this noise is to decrease the overall ADC SNR and ENOB. Any code-dependent noise will also tend to increase the ADC harmonic distortion.

The best approach to eliminating this potential problem is to provide an intermediate three-state output buffer latch which is located close to the ADC data outputs. This latch serves to isolate the noisy signals on the data bus from the ADC data outputs, thereby minimizing any coupling back into the ADC analog input.

The ADC data sheet should be consulted regarding exactly how the ADC data should be clocked into the buffer latch. Usually, a signal called *conversion complete*, or *busy* is provided from the ADC for this purpose.

It is also a good idea not to access the data in the intermediate latch during the actual conversion time of the ADC. This practice will further reduce the possibility of corrupting the ADC analog input with noise. The manufacturer's data sheet timing information should indicate the most desirable time to access the output data.

Figure 13.31 shows a simplified parallel interface between the AD676 16 bit, 100kSPS ADC (or theAD7884) and the ADSP-2101 microcomputer. (Note: the actual device pins shown have been relabled to simplify the following gen-

eral discussion). In a realtime DSP application (such as in digital filtering) the processor must complete its series of instructions within the ADC sampling interval. Note that the entire cycle is initiated by the sampling clock edge from the sampling clock generator. Even though some DSP chips offer the capability to generate lower frequency clocks from the DSP master clock, the use of these signals as precision sampling clock sources is not recommended due to potential excess timing jitter. It is preferable to generate the ADC sampling clock from a well-designed low noise crystal oscillator circuit as has been previously described.

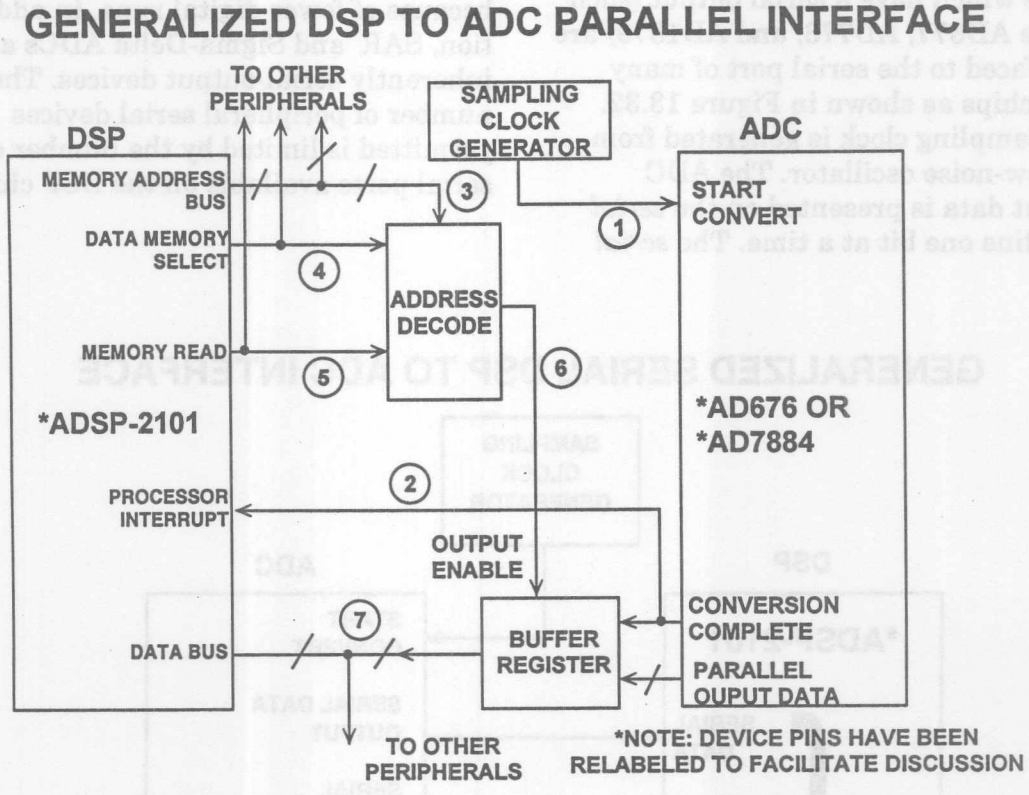


Figure 13.31

The sampling clock edge initiates the ADC conversion cycle. After the conversion is completed, the ADC *conversion complete* line is asserted which in turn interrupts the DSP. The DSP then places the address of the ADC which generated the interrupt on the *data memory address* bus and asserts the *data memory select* line. The *read* line of the DSP is then asserted. This enables the external three-state ADC buffer register outputs and places the ADC data on the *data bus*. The trailing edge of the *read* pulse latches the ADC data on the *data bus* into the DSP internal registers. At this time, the DSP is free to address other peripherals which may share the common data bus.

Because of the high-speed internal DSP clock (50MHz for the ADSP-2101), the width of the *read* pulse may be too narrow to properly access the data in the buffer latch. If this is the case,

adding the appropriate number of programmable software wait states in the DSP will both increase the width of the *read* pulse and also cause the *data memory select* and the *data memory address* lines to remain asserted for a correspondingly longer period of time. In the case of the ADSP-2101, one wait state is one instruction cycle, or 80ns.

ADCs which have a serial output (such as the AD677, AD776, and AD1879) are interfaced to the serial port of many DSP chips as shown in Figure 13.32. The sampling clock is generated from the low-noise oscillator. The ADC output data is presented on the *serial data* line one bit at a time. The *serial clock* signal from the ADC is used to latch the individual bits into the serial input shift register of the DSP serial port. After all the serial data is transferred into the serial input register, the serial port logic generates the required processor interrupt signal. The advantages of using serial output ADCs are the reduction in the number of interface connnections as well as reduced noise because of fewer digital runs. In addition, SAR and Sigma-Delta ADCs are inherently serial-output devices. The number of peripheral serial devices permitted is limited by the number of serial ports available on the DSP chip.

GENERALIZED SERIAL DSP TO ADC INTERFACE

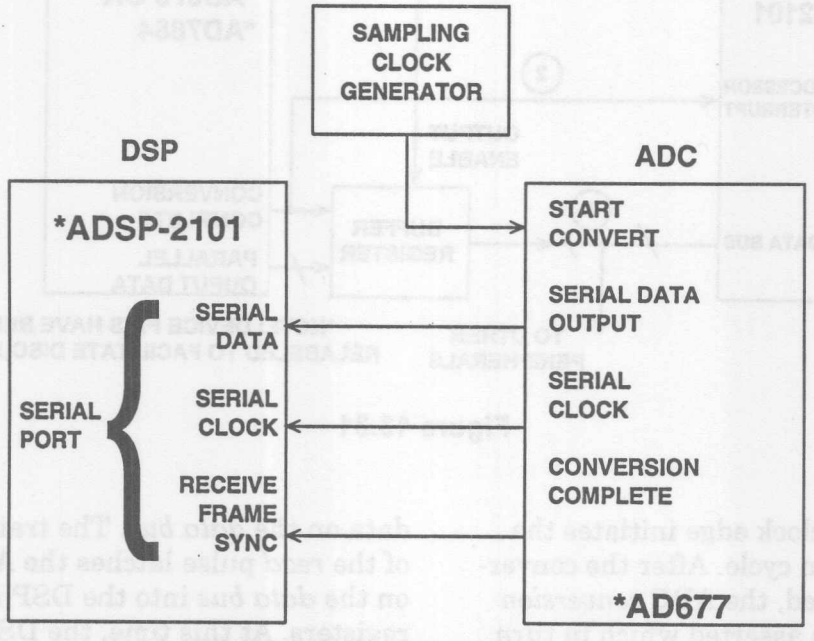


Figure 13.32

PROTECTING THE ADC INPUT FROM OVERDRIVE AND PREVENTING LATCHUP

Most ADCs will tolerate moderate out-of-range signals in the order of 50% or so without damage to the input circuit. The exception to this are certain flash converters which have unipolar negative input ranges. This will be discussed shortly.

For example, an ADC with an input range of ±5V should tolerate an input signal up to ±7.5V. It is usually true, however, that the overvoltage recovery time of an ADC increases as the input signal moves further out of range.

It may be desirable, therefore, to clamp the ADC input so that the input signal is limited to small overrange values. This is especially true if large out-of-range signals are frequently expected. Clamping therefore not only protects the internal ADC input circuits from damage, but also reduces the overvoltage recovery time.

Because the clamping circuit is in the signal path (between the drive amplifier and the ADC), care must be taken to insure that the clamp circuit does not degrade the system performance for normal in-range signals.

The circuit shown in Figure 13.33 utilizes low capacitance (1.2pF), low leakage (100nA @ 15V reverse bias) Schottky diodes (1N5712) to clamp the ADC input to adjustable levels. The series resistor must be chosen so that the drive amplifier output current is limited to acceptable values for overrange signals. A single Schottky diode is capable of withstanding up to 50mA of forward current for short periods of time. If additional current-handling capability is required, two diodes may be paralleled at the expense of additional capacitance and reverse leakage current.

ADJUSTABLE POSITIVE AND NEGATIVE CLAMP CIRCUIT

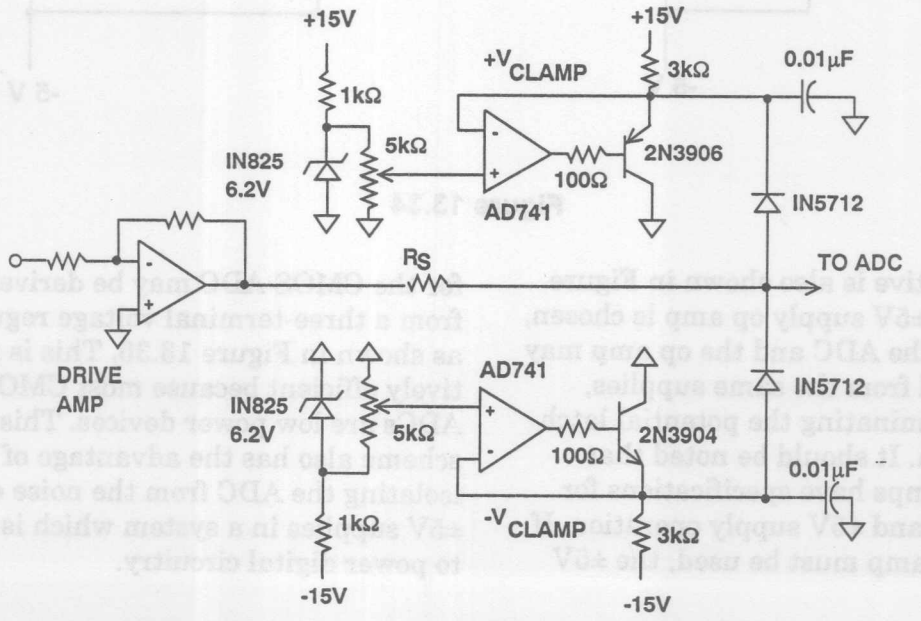


Figure 13.33

Other conditions of temporary overvoltage may occur because of power supply sequencing. Several possibilities will be discussed briefly.

Figure 13.34 shows an op amp powered by ±15V supplies driving an ADC which is powered by ±5V supplies (typical of many high speed ADCs). If the op amp supplies are brought up before the ADC supplies, an overvoltage condition on the ADC input may cause latch up and destroy the device. In addition, the analog input voltage to a CMOS ADC should never exceed the supply voltages, or a latch-up condition may occur. The diodes shown in the figure will protect against this condition. In fact, some CMOS ADCs have the protection diodes on-chip.

PROTECTION AGAINST LATCH-UP AND DAMAGE DUE TO SUPPLY SEQUENCING

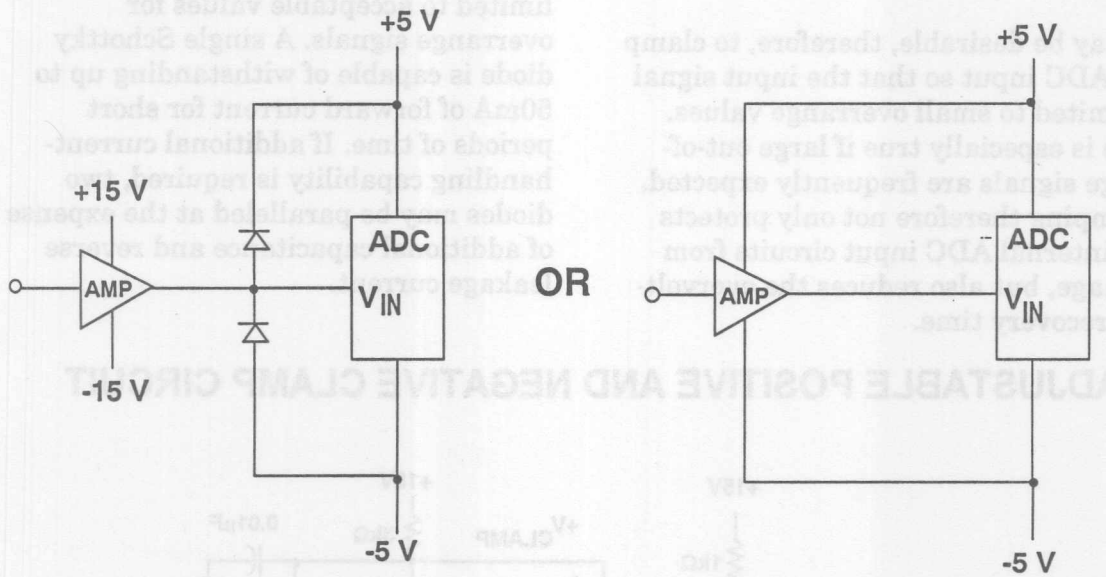


Figure 13.34

An alternative is also shown in Figure 13.34. If a ±5V supply op amp is chosen, then both the ADC and the op amp may be powered from the same supplies, thereby eliminating the potential latch-up problem. It should be noted that many op amps have specifications for both ±15V and ±5V supply operation. If a ±15V op amp must be used, the ±5V for the CMOS ADC may be derived from a three-terminal voltage regulator as shown in Figure 13.35. This is relatively efficient because most CMOS ADCs are low power devices. This scheme also has the advantage of isolating the ADC from the noise on the ±5V supplies in a system which is used to power digital circuitry.

USING 3-TERMINAL REGULATORS AS ADC SUPPLIES

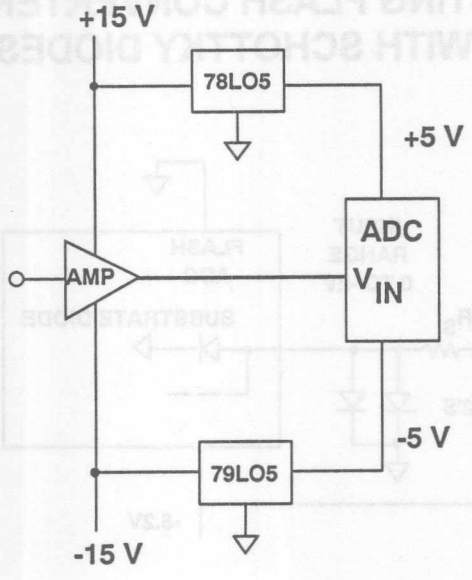


Figure 13.35

Many flash converters are designed to operate on a single –5.2V power supply and have a negative input voltage range of 0 to –2V. If the input goes positive, the substrate silicon diode begins to conduct. Any amount of forward current above a few mA may permanently degrade the performance of the flash converter. Input Schottky diodes should be installed as shown in Figure 13.36 to prevent this condition. Most amplifiers suitable for driving flash converters (such as the AD9617) operate on dual 5V supplies and can deliver 50 to 100mA of output current. The series resistor should be chosen to limit this current to an acceptable level. Two diodes should be paralleled if more than 50mA current is expected from the drive amplifier.

PROTECTING FLASH CONVERTER INPUTS WITH SCHOTTKY DIODES

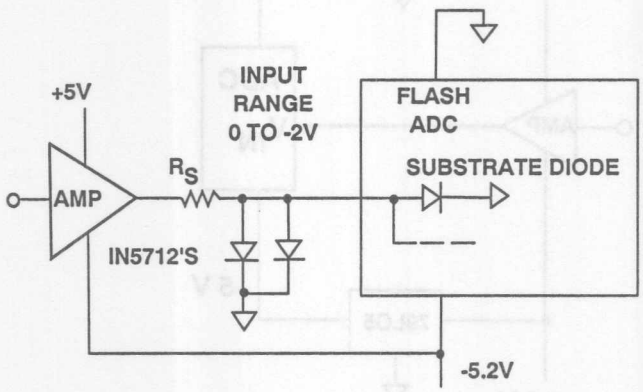


Figure 13.36

SAMPLING CLOCK GENERATION

Many users of sampling ADCs fail to understand the critical nature of the sampling clock signal. The tendency is to focus more on the ADC aperture jitter specification, when in reality, ADC dynamic errors due to noise and jitter on the sampling clock input may far exceed those caused by the internal ADC aperture jitter itself.

Aperture jitter, t_a, is simply the rms value of the sample-to-sample variation in the precise point in time at which the input signal is sampled. This rms time jitter produces a corresponding rms voltage error which is proportional to the slew rate of the input signal. The effect of broadband time jitter is to degrade the overall SNR of the ADC.

Aperture jitter for an ADC is usually attributed to the SHA. The ADC aperture jitter, unfortunately, is certainly not the only possible source for this error. In a practical ADC, the sampling clock is often phase and amplitude modulated by some unwanted external sources; the sources can be wideband random noise, oscillator phase noise, power line noise, or digital noise due to poor layout, bypassing, and grounding techniques. Phase jitter on the input sinewave produces the same effect as jitter on the sampling clock.

The effects of even small amounts of timing jitter are shown in Figure 13.37, where SNR and ENOB are plotted as a function of fullscale input sinewave frequency for various amounts of rms timing jitter using the above formula. For example, in order to achieve 12 bit SNR (74dB) on a 10MHz fullscale input sinewave, the rms jitter can be no more than 3ps rms.

EFFECTS OF APERTURE JITTER ON SNR AND ENOB

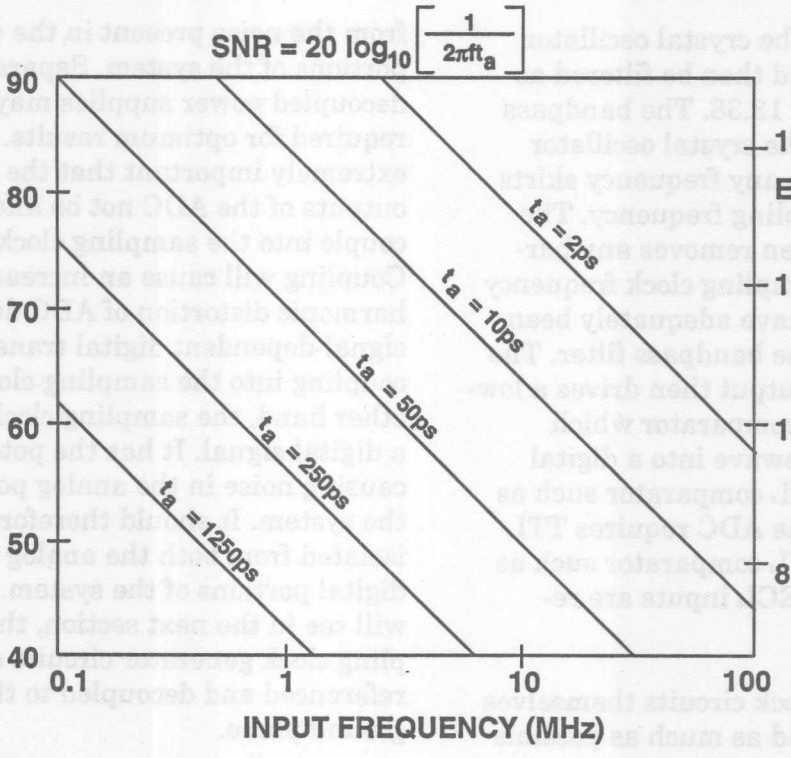


Figure 13.37

The total rms timing jitter will probably consist of two frequency components: narrowband and broadband. The sampling clock oscillator will probably have narrowband phase noise. The effect of narrow-band phase noise centered about the sampling frequency is to produce similar phase noise about the fundamental sinusoid frequency in an FFT of the digitized sinusoid. The high-speed logic circuits in the sampling clock path may introduce broadband noise on the pulse edges which in turn causes broadband jitter due to sample-to-sample variations in the precise times at which the internal logic thresholds are crossed. ECL logic gates have an effective bandwidth greater than 300MHz, and a typical 100K ECL gate has an effective rms timing jitter of approximately 7ps rms.

A detailed mathematical analysis of broadband and narrowband timing jitter is much beyond the scope of this discussion, however their effects may be observed directly in the FFT analysis of a sinusoid. The narrowband phase noise will show up as a widening of the main lobe of the fundamental sinusoid, while the broadband jitter will cause an overall increase in the noise floor.

The sampling clock generator must have low phase noise, therefore RC and relaxation oscillators should be ruled out completely. A crystal oscillator is much preferred. The crystal oscillator should not be constructed out of logic gates, capacitors, and resistors, however, but should be built around discrete bipolar and FET devices in the circuits recommended by the crystal

manufacturer. The crystal oscillator output put should then be filtered as shown in Figure 13.38. The bandpass filter following the crystal oscillator serves to remove any frequency skirts around the sampling frequency. The lowpass filter then removes any harmonics of the sampling clock frequency which may not have adequately been attenuated by the bandpass filter. The pure sinewave output then drives a low-jitter wideband comparator which converts the sinewave into a digital signal. Use a TTL comparator such as the AD9696 if the ADC requires TTL inputs, or an ECL comparator such as the AD96685 if ECL inputs are required.

The sampling clock circuits themselves should be isolated as much as possible from the noise present in the digital portions of the system. Separate decoupled power supplies may also be required for optimum results. It is extremely important that the digital outputs of the ADC not be allowed to couple into the sampling clock signal. Coupling will cause an increase in the harmonic distortion of ADC due to signal-dependent digital transients coupling into the sampling clock. On the other hand, the sampling clock is itself a digital signal. It has the potential for causing noise in the analog portion of the system. It should therefore be isolated from both the analog and digital portions of the system. As we will see in the next section, the sampling clock generator circuits should be referenced and decoupled to the analog ground plane.

GENERATING PRECISION LOW-JITTER ADC SAMPLING CLOCKS

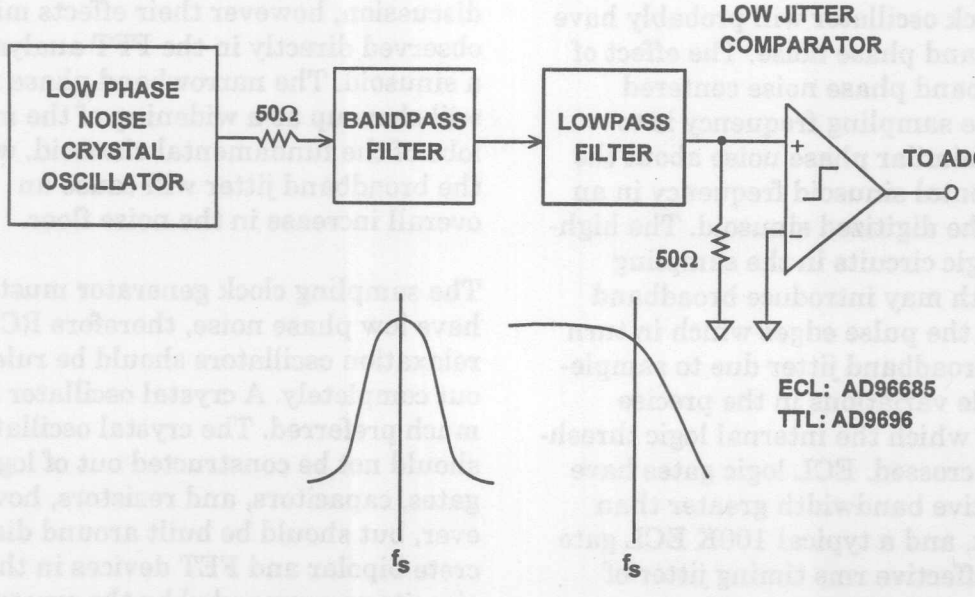


Figure 13.38

POWER SUPPLIES, GROUND PLANES, DECOUPLING, AND LAYOUT

The switching-mode power supply offers low cost, small size, high efficiency, high reliability and the possibility of operating from a wide range of input voltages without adjustment. Unfortunately, these supplies produce noise over a broad band of frequencies, and this noise occurs as conducted noise, radiated noise, and unwanted electric and magnetic fields. When used to supply logic circuits, even more noise is generated on the power supply bus. The noise transients on the output lines of switching supplies are short-duration voltage spikes. Although the actual switching frequencies may range from 10 to 100kHz, these spikes can contain frequency components that extend into the hundreds of megahertz.

Because of the wide variations in the noise characteristics of commercially available switching supplies, they should always be purchased in accordance with a specification-control drawing. Although specifying switching supplies in terms of rms noise is common practice, you should also specify the peak amplitudes of the switching spikes under the output loading conditions you expect in your system. You should also insist that the switching-supply manufacturer inform you of any internal supply design changes that may alter the spike amplitudes, duration, or switching frequency. These changes may require corresponding changes in the external power-supply filtering networks.

SWITCHING-MODE POWER SUPPLIES

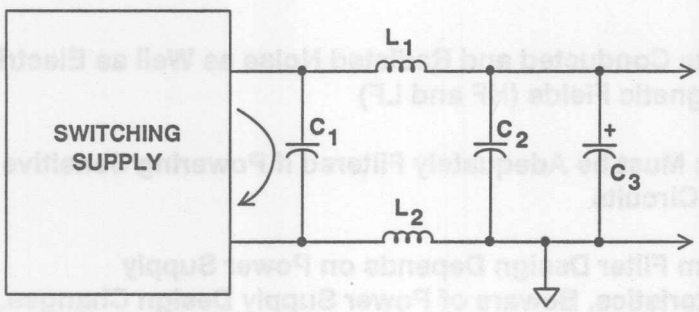
- Generate Conducted and Radiated Noise as Well as Electric and Magnetic Fields (HF and LF)
- Outputs Must be Adequately Filtered if Powering Sensitive Analog Circuits
- Optimum Filter Design Depends on Power Supply Characteristics. Beware of Power Supply Design Changes.
- Use Faraday Shields to Reduce HF Electric and HF Magnetic Fields
- Physically Isolate Supply from Analog Circuits
- Temporarily Replace Switching Supply with Low-Noise Linear Supply or Battery when Suspicious of Switching Supply Noise

Figure 13.39

Filtering switching supply outputs that provide several amps and generate voltage spikes having high frequency components is a challenge. For this reason, you should place the initial filtering burden on the switching supply manufacturer. Even so, external filtering such as shown in Figure 13.40 should be added. The series inductors isolate both the output and common lines from the external circuits. Because the load currents may be large, make sure that the inductors selected do not saturate. Split-core inductors or large ferrite beads make a good choice. Because the switching power supplies generate high and low frequency electric and magnetic fields, they should be physically separated as far as possible from critical analog circuitry. This is especially important in preventing the inductive coupling of low frequency magnetic fields.

Proper power supply decoupling techniques must be used on each PC board in the system. Figure 13.41 shows an arrangement which will ensure minimum problems. The power supply input (usually brought into the PC board on multiple pins) is first decoupled to the large-area low-impedance ground plane with a good quality, low ESL, ESR tantalum electrolytic capacitor. This capacitor bypasses low frequency noise to the ground plane. The ferrite bead reduces high frequency noise to the rest of the circuit. You should then place one low-inductance ceramic capacitor at each power pin on each IC. Ideally, you should use surface-mount chip capacitors for minimum inductance, but if you use leaded ceramics, be sure to minimize the lead lengths by mounting them flush on the PC board. Some ICs may require an additional small tantalum electrolytic capacitor (usually between 1 and 5μF). The data sheets for each IC should provide appropriate recommendations, but when in doubt, put them in!

FILTERING A SWITCHING SUPPLY OUTPUT



- C_1 MUST HAVE LOW INDUCTANCE AND BE CLOSE TO THE SUPPLY TO MINIMIZE HF CURRENT LOOPS AND RESULTANT HF MAGNETIC FIELDS
- C_2 IS ALSO LOW INDUCTANCE, C_3 IS ELECTROLYTIC
- IF THE SWITCHING SUPPLY IS INTERNALLY GROUNDED, L_2 SHOULD BE OMITTED

Figure 13.40

PROPER POWER SUPPLY DECOUPLING AT EACH IC ON THE PC BOARD IS CRITICAL TO achieving GOOD HIGH SPEED SYSTEM PERFORMANCE

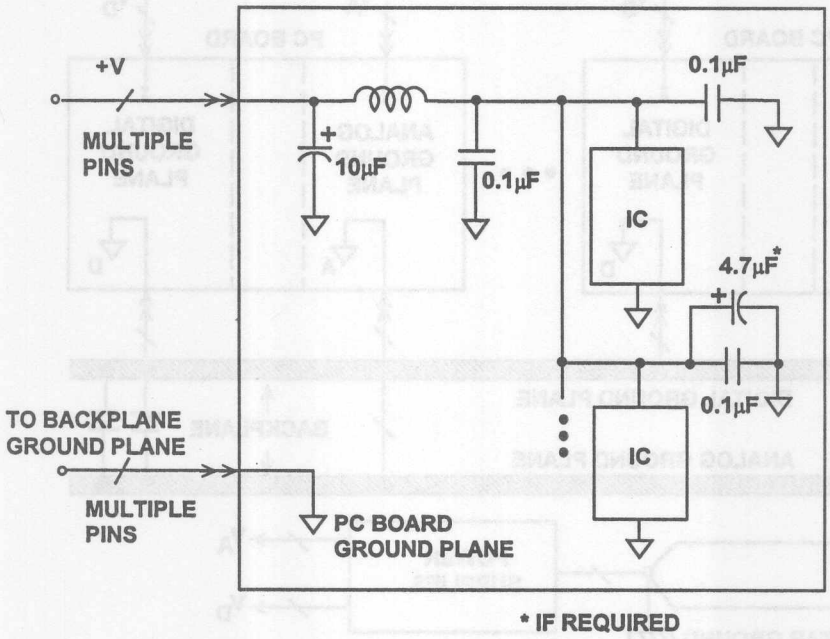


Figure 13.41

If a double-sided PC board is used, one side should be dedicated entirely (at least 75% of the total area) to the ground plane. The ICs are mounted on this side, and connections are made on the opposite side. Because of component interconnections, however, a few breaks in the ground plane are usually unavoidable. As more and more of the ground plane is eaten away for interconnections, its effectiveness diminishes. It is therefore recommended that multilayer PC boards be used where component packing density is high. Dedicate at least one entire layer to the ground plane.

When connecting to the backplane, use a number of pins (30 to 40%) on each PC board connector for ground. This will ensure that the low impedance ground plane is maintained between the various PC boards in a multicard system.

In practically all high speed systems, it is highly desirable to physically separate sensitive analog components from noisy digital components. It is usually a good idea to also establish separate analog and digital ground planes on each PC board as shown in Figure 13.42. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground screens" which are made up of a series of wired interconnections between the connector ground pins. The ground planes are joined together at the system *star ground* , or *single-point ground*, usually located at the common return point for the power supplies. The Schottky diodes are inserted to prevent significant accidental dc voltages from developing between the two ground systems.

SEPARATING ANALOG AND DIGITAL GROUNDS IN A MULTICARD, STAR GROUND SYSTEM

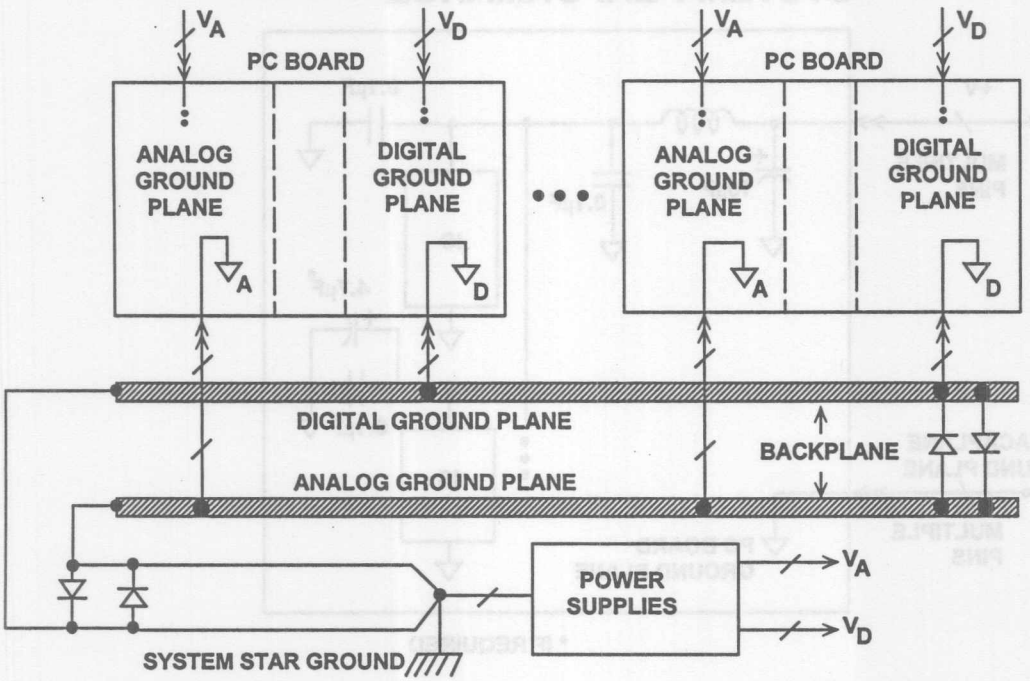


Figure 13.42

PROPER GROUNDING OF ADCs, DACs, AND MIXED SIGNAL ICs

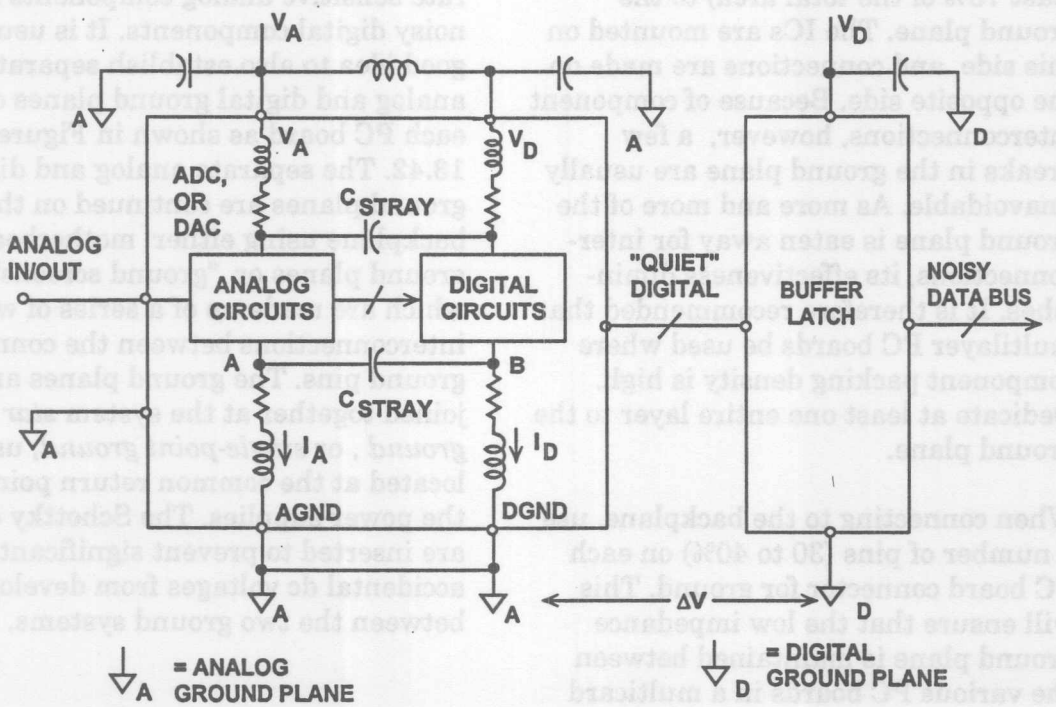


Figure 13.43

Sensitive analog components such as amplifiers and voltage references are referenced and decoupled to the analog ground plane. *The ADCs and DACs (and even some mixed-signal ICs) should be treated as analog circuits and also grounded and decoupled to the analog ground plane.* At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually pins designated as analog ground (AGND) and digital ground (DGND). The diagram shown in Figure 13.43 will help to explain this seeming dilemma.

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 13.43 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the pads on the chip to the package pins except to realize it's there. the rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, C_{STRAY}. In addition, there is approximately 0.2pF unavoidable stray capacitance between every pin of the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance.

It is true that this arrangement will inject a small amount of digital noise on the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter input/or output does not drive a large fanout. Minimizing the fanout on the converter's digital port will also keep the converter logic level transitions relatively free from ringing, and thereby minimize any potential coupling into the analog port of the converter. The logic supply pin (V_D) can be further isolated from the analog supply by the insertion of a small ferrite bead as shown in Figure 13.43. The internal digital currents of the converter will return to ground through the V_D pin decoupling capacitor (mounted as close to the converter as possible) and will not appear in the external ground circuit. It is always a good idea (as shown in Figure 13.43) to place a buffer latch adjacent to the converter to isolate the converter's digital lines from any noise which may be on the data bus. Even though a few high speed converters have three-state outputs/inputs, this isolation latch represents good design practice.

The buffer latch and other digital circuits should be grounded and decoupled to the digital ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter.

POWER SUPPLY, GROUNDING, AND DECOUPLING POINTS

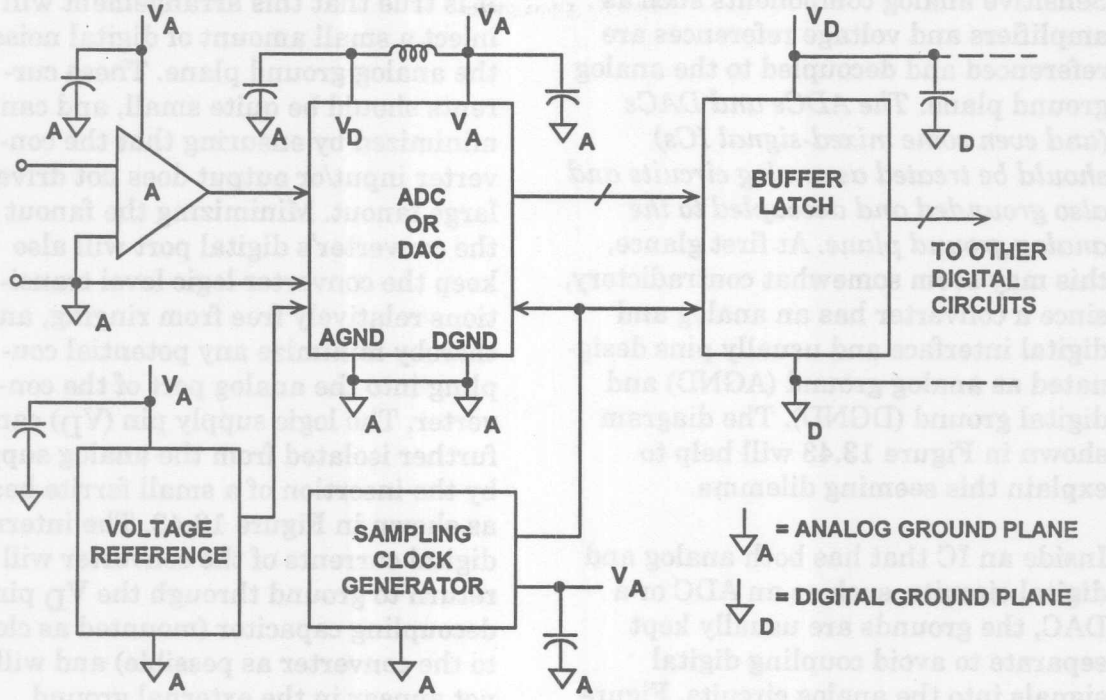


Figure 13.44

The sampling clock generation circuitry should also be grounded and heavily-decoupled to the analog ground plane. As previously discussed, phase noise on the sampling clock produces aperture jitter and a corresponding degradation in system SNR.

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V_D), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious.

A clean, analog-grade supply can be generated from a 5V logic supply using a differential LC filter with separate power supply and return lines as shown in Figure 13.45. The supply output is virtually free of any glitch noise as evident in the scope photo shown in Figure 13.46, which compares the input and output sides of the filter. All capacitors were selected from commonly available types. Lower noise can be attained using low ESR (Equivalent Series Resistance) type electrolytic and tantalum capacitors. The circuit as shown can handle 100mA of load current without the risk of saturating the ferrite core. Higher current capacity can be achieved using larger ferrite cores.

DIFFERENTIAL LC FILTER TURNS NOISY LOGIC SUPPLIES INTO NOISE-FREE ANALOG SUPPLIES

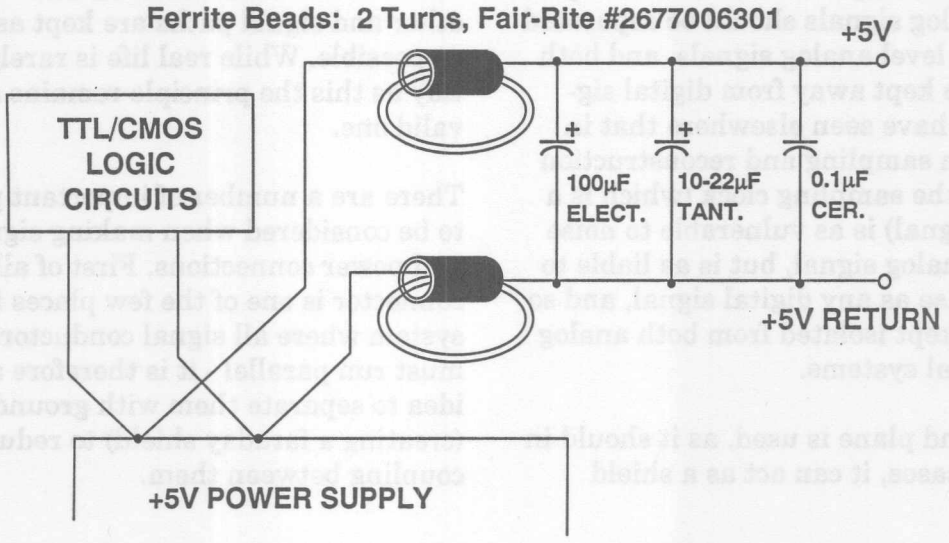
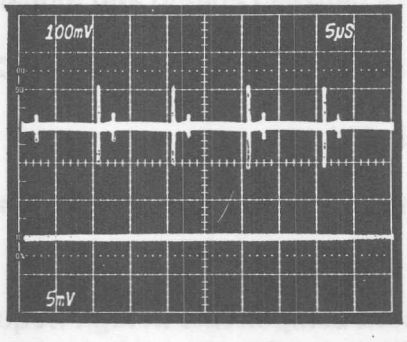


Figure 13.45

LC FILTER VIRTUALLY ELIMINATES ALL GLITCH NOISE



BEFORE FILTER — 100mV / div.

AFTER FILTER — 5mV / div.

HORIZONTAL SCALE: 5µs / div.

Figure 13.46

It is evident that we can minimize noise by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.

If a ground plane is used, as it should in be most cases, it can act as a shield where sensitive signals cross. Figure 13.48 shows a good layout for a data acquisition system where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this the principle remains a valid one.

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run parallel - it is therefore a good idea to separate them with ground pins (creating a faraday shield) to reduce coupling between them.

SIGNAL ROUTING IN MIXED SIGNAL SYSTEMS

- Physically separate analog and digital signals.
- Avoid crossovers between analog and digital signals.
- Be careful with sampling clock and ADC/DAC analog runs.
- Use lots of ground plane.
- Use microstrip techniques at high frequencies for controlled impedances.
- Use surface mount components in high frequency systems to minimize parasitic capacitance and inductance.

Figure 13.47

A PC BOARD LAYOUT SHOWING GOOD SIGNAL ROUTING

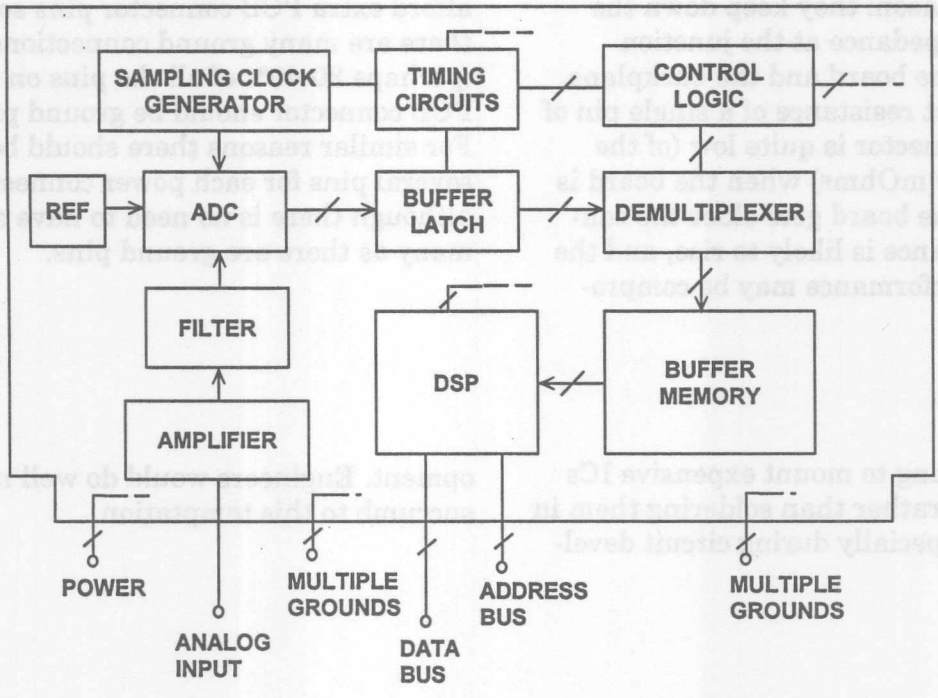


Figure 13.48

13

EDGE CONNECTIONS

- Separate sensitive signal by ground pins.
- Keep down ground impedances with multiple (30-40% of total) ground pins.
- Have several pins for each power line.
- Critical signals such as analog or sampling clocks may require a separate connector (possibly coax), or microstrip techniques.

Figure 13.49

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10 mOhms) when the board is new - as the board gets older the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to afford extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

SOCKETS

It is tempting to mount expensive ICs in sockets rather than soldering them in circuit - especially during circuit development. Engineers would do well not to succumb to this temptation.

USE OF SOCKETS WITH HIGH PERFORMANCE ANALOG CIRCUITS

- **DON'T! (If at all possible)**
- **Use "Pin sockets" or "Cage jacks" such as Amp Part No: 5-330808-3 or 5-330808-6 (Capped & uncapped respectively).**
- **Always test the effect of sockets by comparing system performance with and without the use of sockets.**
- **Do not change the type of socket or manufacturer used without evaluating the effects of the change on performance.**

Figure 13.50

Sockets add resistance, inductance and capacitance to the circuit and may degrade performance to quite unacceptable levels. When this occurs, though, it is always the IC manufacturer who is blamed - not the use of a socket. Even low profile, low insertion force sockets cannot be relied upon to ensure the performance of high performance (high speed or high precision or, worst of all, both) devices. As the socket ages and the board suffers vibration, the contact resistance of low insertion force sockets is very likely to rise. Where a socket must be used the best performance is achieved by using individual pin sockets (sometimes called "cage jacks") to make up a multi-pin socket in the PCB itself.

It really is best not to use IC sockets with high performance analog and mixed signal circuits. If their use can be avoided it should be. However at medium speeds and medium resolutions the trade-off between performance and convenience may fall on the side of convenience. It is very important, when sockets are used, to evaluate circuit performance with and without the socket chosen to ensure that the type of socket chosen really does have minimal effect on the way that the circuit behaves. The effects of a change of socket on the circuit should be evaluated as carefully as a change of IC would be and the drawings should be prepared so that the change procedures for a socket are as rigorous as for an IC - in order to prevent a purchase clerk who knows nothing of electronics from devastating the system performance in order to save five cents on a socket.

PROTOTYPING HIGH PERFORMANCE ANALOG CIRCUITRY

As we have seen, circuit board layout is part of the circuit design of all high performance analog circuits. Prototyping techniques derived from the "node" theory, while ideal for logic breadboarding at low and medium speeds, are quite unsuitable for any analog circuits, or even for very fast digital ones. Vector board and wire wrap prototyping will tell an engineer nothing about the behavior of a properly laid out version of the analog circuit.

The best technique for analog prototyping is to use a prototype of the final PCB - certainly no design is complete until the final PCB layout has been proved to give the required performance. This approach may be a little limiting where a number of different possibilities are to be evaluated, or for a multicard system.

In this case components should be mounted on a board having a continuous copper ground plane (ideally on both sides of the board, though while convenient, this is not essential), with ground connections made to the plane and short point to point wiring made above and below it. The overall component placing and signal routing should be as close as possible to the planned final layout.

As we have already indicated, IC sockets can degrade the performance of analog ICs. While directly soldered components are ideal for prototyping, an IC socket made of pin sockets mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5 mm around each ungrounded pin socket - solder the grounded ones to ground on both sides of the board).

PROTOTYPING MIXED SIGNAL CIRCUITRY

- **NEVER use vector boards or wire-wrap for the analog parts of the system (they can be invaluable for data buses and address lines in the digital part).**
- **Wherever possible avoid the use of sockets for analog ICs.**
- **Use a prototype of your final PCB layout as early as possible.**

Figure 13.51

Allowing wiring to float in the air can be a little tricky. There is a breadboarding system which is conceptually very similar to that described above but which provides adhesive PC pads which stick to the ground plane and allow more rigid component mounting and wiring. This system is manufactured by Wainwright Instruments and is known as "Minimount" in Europe and "Solder Mounts" in the USA. The manufacturer's and distributors' addresses are given in Reference 1 at the end of this section.

Manufacturer's evaluation boards are also useful in system prototyping since they have already been optimized for best performance. Analog Devices offers many evaluation boards for a wide array of products. They offer the designer an excellent starting point for the layout.

When the prototype layout is transferred to a CAD system for PCB layout it is important to disable, or at any rate override where necessary, any automatic routing or component placing software. The criteria used by such software are more closely related to "node" theory and aesthetically pleasing rows of components (which, admittedly, are also easier on automatic component placing machinery) than to optimizing stray inductance and capacitance and minimizing common ground impedances.

ADDITIONAL PROTOTYPING HINTS

- Pay *equal* attention to signal routing, component placing and supply decoupling in *both* the prototype and the final design.
- Verify performance as well as functionality at each stage of the design.
- For "freehand" prototyping use a copper-clad board, mount components to it by their ground pins and wire the remaining connections point-to-point (use Wainwright Instruments' Minimount/Solder Mount adhesive PC pads if aerial point-to-point wiring seems too fraught with peril).

Figure 13.52

REFERENCES

1. Wainwright Instruments, Inc., 7770 Regents Rd., #113, Suite 371, San Diego, CA 92122, Tel. 619-558-1057. Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-2245, Fax: +49-8152-5174.

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SECTION 14

SIGMA-DELTA ADCs AND DACs

- SIGMA-DELTA OVERVIEW
- OVERSAMPLING
- SIGMA-DELTA MODULATORS AND QUANTIZATION NOISE SHAPING
- DIGITAL FILTERING AND DECIMATION
- IDLE TONES IN SIGMA-DELTA ADCs
- HIGHER ORDER MODULATOR LOOPS
- DESCRIPTION OF THE AD776 THIRD-ORDER SIGMA-DELTA ADC
- DESCRIPTION OF AD1879 18 BIT SIGMA-DELTA AUDIO ADC
- SIGMA-DELTA DACs
- THE AD28MSP02 SIGMA-DELTA CODEC
- MULTISTAGE NOISE SHAPING (MASH) SIGMA-DELTA CONVERTERS
- MULTI-BIT SIGMA-DELTA CONVERTERS
- SIGMA-DELTA SUMMARY

SECTION 14

SIGMA-DELTA ADCs AND DACs

Walt Kester, James Bryant

SIGMA-DELTA OVERVIEW

Within the last several years, the sigma-delta architecture for realizing high-resolution ADCs has become available in mixed-signal VLSI processes. Until recently, however, the process technology needed to make these devices commercially viable has not been available. Now that 1 micron and smaller CMOS geometries are manufactureable, sigma-delta converters will become even more prolific in certain types of applications, especially mixed-signal ICs which combine the ADC, DAC, and DSP functions on a single chip.

Conceptually, the sigma-delta architecture is more digital than analog intensive. This does not, however, minimize the importance of the analog portion of the sigma-delta ADC. The analog design of a fifth-order sigma-delta modulator (as in the AD1879 dual 18 bit ADC) is certainly not a trivial matter. The sigma-delta converter is inherently an oversampling converter, although oversampling is just one of the techniques contributing to the overall performance. Basically, a sigma-delta converter digitizes an analog signal with a very low resolution (1 bit) ADC at a very high sampling rate. By using oversampling techniques in conjunction with noise shaping and digital filtering, the effective resolution is increased. Decimation is then used to reduce the effective sampling rate at the ADC output. The sigma-delta ADC exhibits excellent differential and integral linearity due to the linearity of the 1 bit quantizer and DAC, and no trimming is required (unlike other ADC architectures).

The key concepts involved in understanding the operation of sigma-delta converters are *oversampling*, *noise shaping* (using a sigma-delta modulator), *digital filtering*, and *decimation*.

SIGMA-DELTA CONCEPTS

- Ideal Topology for Mixed Signal VLSI Chips
- Oversampling
- Noise-Spectrum Shaping Using Sigma-Delta Modulator
- Digital Filtering
- Decimation
- 16 Bits and Higher Resolution Possible Using One-Bit Quantizer

Figure 14.1

OVERSAMPLING

A major advantage of oversampling an analog signal is the resulting simplification in the analog antialiasing filter requirements. The disadvantage of simple oversampling is that it also increases the ADC output data rate which increases the required size of the buffer memory; and in real-time DSP applications, there is less time between samples to perform calculations. An attractive alternative to simple oversampling makes use of both analog *and* digital filtering techniques and a process called *decimation* (Figure 14.2).

The top portion of the figure shows the case of traditional Nyquist sampling. In the lower portion of the diagram, the sampling rate has been increased by a factor of K (the oversampling ratio). Note the resulting relaxation of the requirement on the analog antialiasing filter. The analog signal is sampled at rate equal to Kf_s, and the new Nyquist bandwidth is $Kf_s/2$. Although the filter requirement is relaxed, the ADC output data rate is correspondingly higher.

If we apply the ADC data to a digital filter (as shown in the bottom portion of Figure 14.2), the energy falling between $f_s - f_a$ and Kf_s can be removed. Digital filters having sharp cutoff characteristics with good phase response are much more easily implemented than their corresponding analog counterparts (assuming sufficient speed in the DSP). Finite Impulse Response (FIR) filters can easily be designed with linear phase characteristics. Since the bandwidth has been reduced to $f_s/2$ by the digital antialiasing filter, the data coming out of the digital filter actually contains redundant information, and there is no need to use every sample. In fact, it is only necessary to look at every Kth

sample. This process is called *decimation*. The actual decimation can be performed by the FIR filter itself by computing a single output sample for every K input samples. Figure 14.3 illustrates the differences in traditional Nyquist sampling and oversampling with digital filtering.

EFFECT OF OVERSAMPLING ON ANTIALIASING FILTER REQUIREMENTS

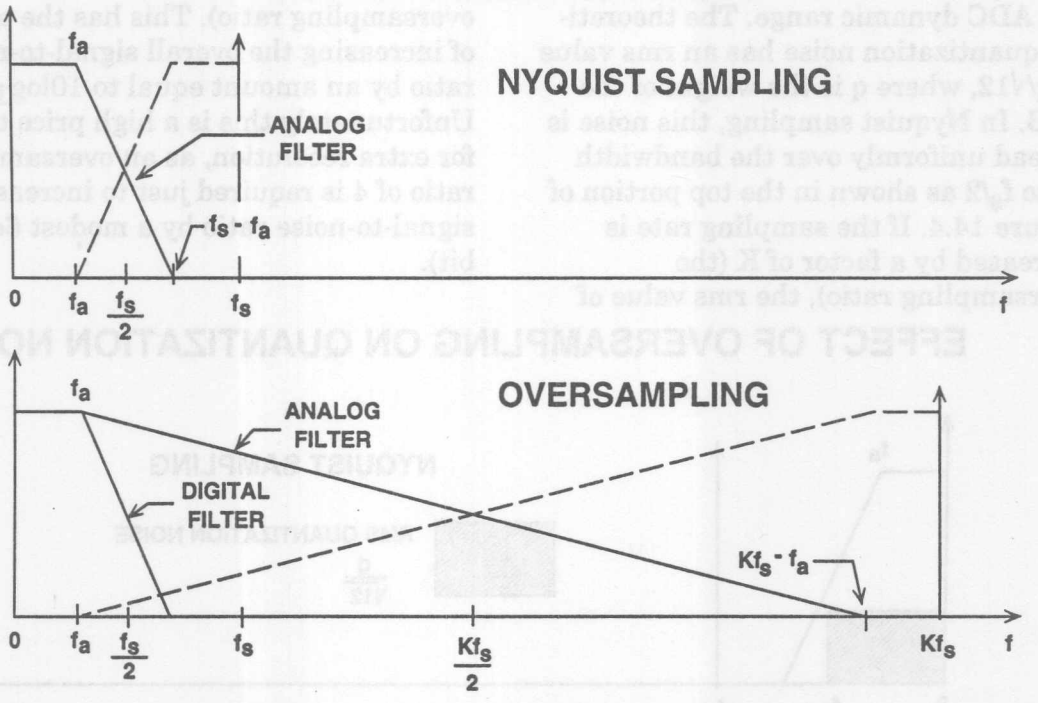


Figure 14.2

NYQUIST SAMPLING VERSUS OVERSAMPLING SYSTEMS

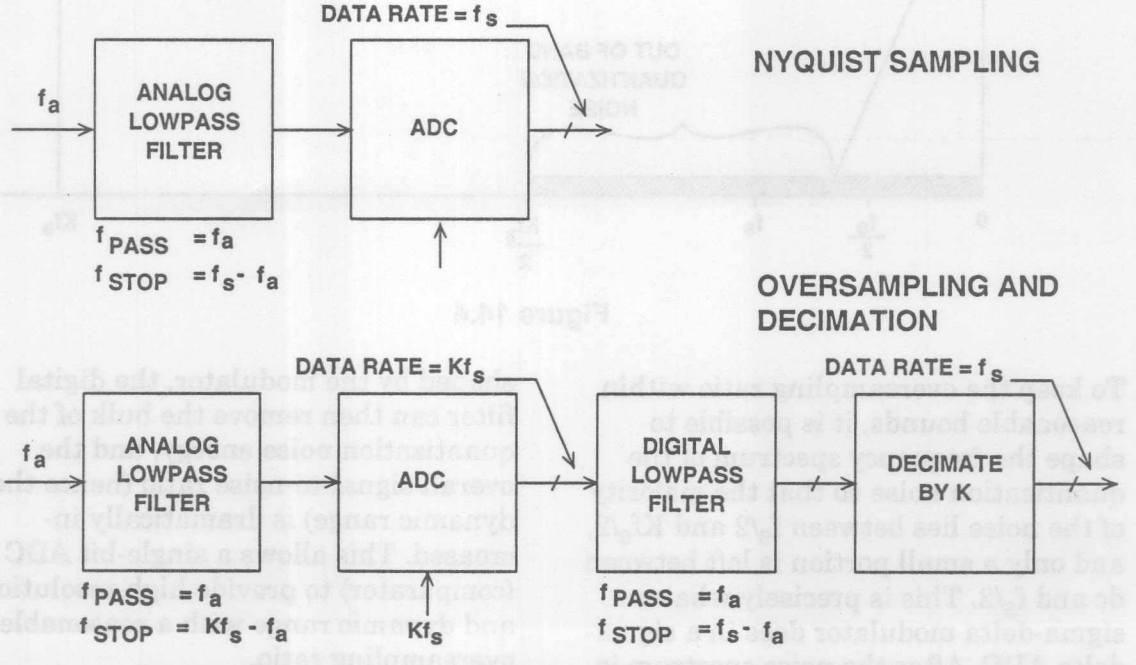


Figure 14.3

As discussed above, one significant benefit of oversampling is that the rolloff requirements on the analog antialiasing filter are relaxed. There is an additional benefit which relates to the quantization noise spectrum and the ADC dynamic range. The theoretical quantization noise has an rms value of $q/\sqrt{12}$, where q is the weight of the LSB. In Nyquist sampling, this noise is spread uniformly over the bandwidth dc to $f_S/2$ as shown in the top portion of Figure 14.4. If the sampling rate is increased by a factor of K (the oversampling ratio), the rms value of the quantization noise remains the same, but it is now spread out over a bandwidth dc to $Kf_S/2$ (see the bottom portion of Figure 14.4). The noise which falls between $f_S/2$ and $Kf_S/2$ is removed by the digital filter (K is the oversampling ratio). This has the effect of increasing the overall signal-to-noise ratio by an amount equal to $10\log_{10}(K)$. Unfortunately this is a high price to pay for extra resolution, as an oversampling ratio of 4 is required just to increase the signal-to-noise ratio by a modest 6dB (1 bit).

EFFECT OF OVERSAMPLING ON QUANTIZATION NOISE

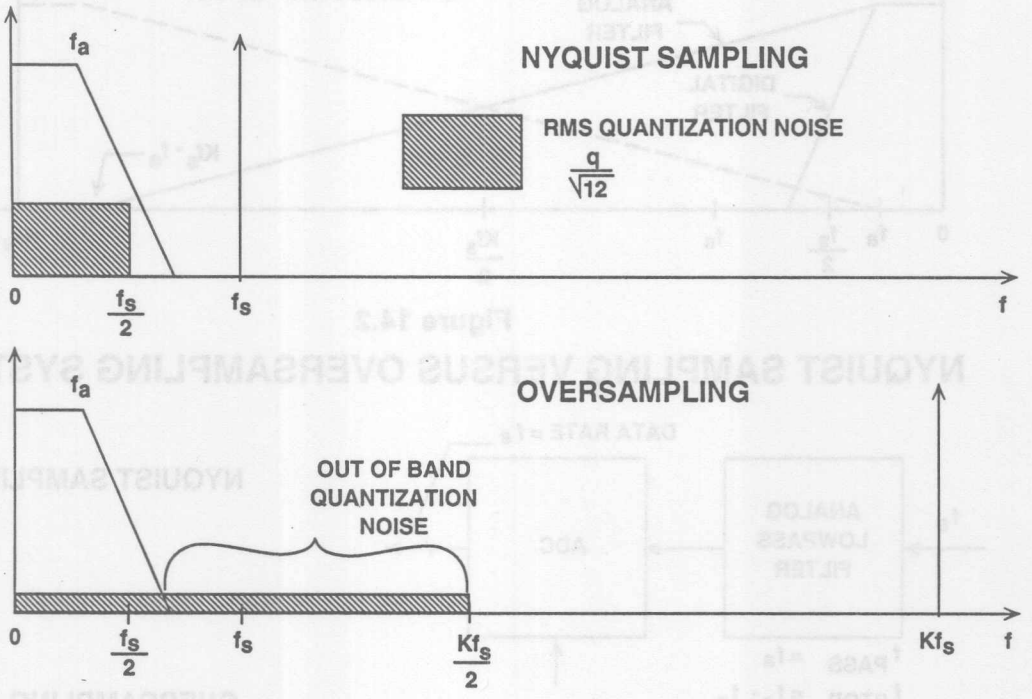


Figure 14.4

To keep the oversampling ratio within reasonable bounds, it is possible to shape the frequency spectrum of the quantization noise so that the majority of the noise lies between $f_S/2$ and $Kf_S/2$, and only a small portion is left between dc and $f_S/2$. This is precisely what a sigma-delta modulator does in a sigma-delta ADC. After the noise spectrum is shaped by the modulator, the digital filter can then remove the bulk of the quantization noise energy, and the overall signal-to-noise ratio (hence the dynamic range) is dramatically increased. This allows a single-bit ADC (comparator) to provide high resolution and dynamic range with a reasonable oversampling ratio.

SIGMA-DELTA MODULATORS AND QUANTIZATION NOISE SHAPING

A block diagram of a first-order sigma-delta ADC is shown in Figure 14.5. The first part of the converter is the sigma-delta modulator which converts the input signal into a continuous serial stream of 1's and 0's at a rate determined by the sampling clock frequency, Kf_S. The 1-bit DAC is driven by the serial output data stream, and the DAC output is subtracted from the input signal. Feedback control theory tells us that the average value of the DAC output (hence the serial bit stream) must approach that of the input signal if the loop has enough gain. The integrator can be represented in the frequency domain by a filter whose amplitude response is proportional to 1/f, where f is the input frequency. Since the chopper-like action of the clocked, latched comparator converts the input signal to a high-frequency ac signal, varying about the average value of the input, the effective quantization noise at low frequencies is greatly reduced (the integrator looks like a high-pass filter to quantization noise). The exact frequency spectrum of the resulting noise depends on the sampling rate, the integrator time constant, and the precise span of the voltage fed back.

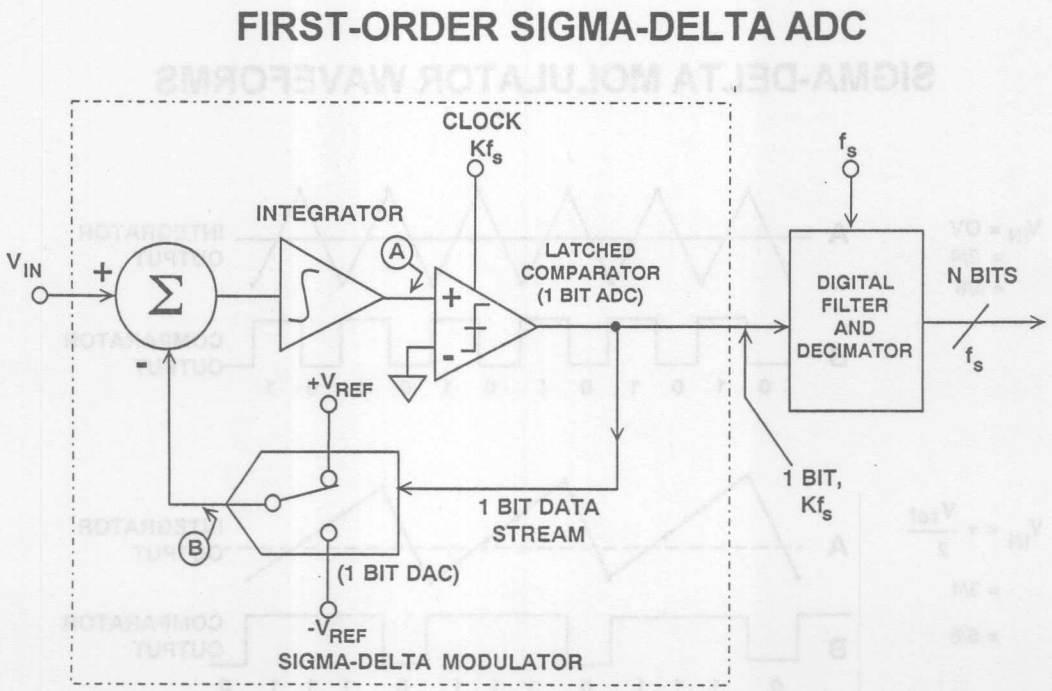


Figure 14.5

For any given input value in a single sampling interval, the data from the 1-bit ADC is meaningless. Only when a large number of samples is averaged will a meaningful value result. The sigma-delta modulator is difficult to analyze in the time domain because of this apparent randomness of the single-bit data output. If the input signal is near positive fullscale, it is clear that there will be more 1's than 0's in the bit stream. Likewise, for signals near negative fullscale, there will be more 0's than 1's in the bit stream. For signals near midscale, there will be approximately equal numbers of 1's and 0's. Figure 14.6 shows the output of the integrator for two input conditions. The first is for an input of zero (midscale). To decode the output, pass the output samples through a simple digital lowpass filter that averages every four samples. The output of the filter is 2/4. This value represents bipolar zero. If more samples are averaged, more dynamic range is achieved. For example, averaging 4 samples gives 2 bits of resolution, while averaging 8 samples yields 4/8, or 3 bits of resolution. In the bottom waveform of Figure 14.6, the average obtained for 4 samples is 3/4, and the average for 8 samples is 6/8.

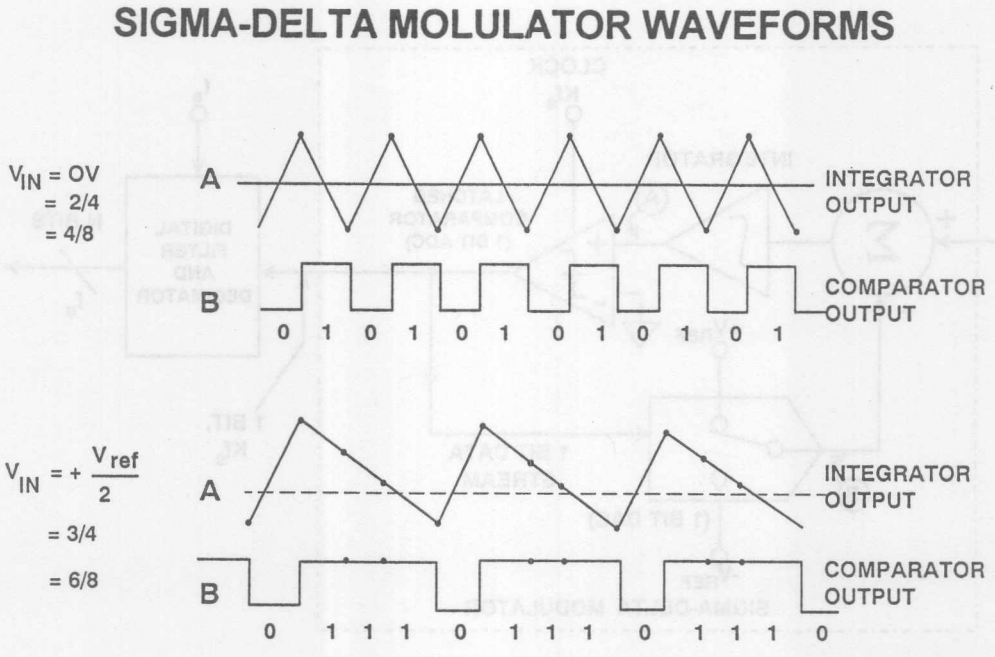


Figure 14.6

But the sigma-delta ADC cannot just be viewed as a synchronous voltage-to-frequency converter followed by a counter. True, if the number of 1's in the output data stream is counted over a sufficient number of samples, the counter output will represent the digital value of the input. But a simple VFC followed by a counter must double its sampling interval for each bit's increase in resolution (i.e. a 20-bit ADC using such an architecture must sample for at least a million clock cycles). The value of the ΣΔ ADC is that it requires a much lower over-sampling ratio. while the purpose of this seminar is to show *what* happens, rather than give a detailed description of *why* it happens, a brief description of the operation of a ΣΔ ADC in the frequency domain is appropriate at this point. Consider the linear model in Figure 14.7.

FREQUENCY DOMAIN LINEARIZED MODEL OF A SIGMA-DELTA MODULATOR

$$y = \frac{x}{f+1} + \frac{Qf}{f+1}$$

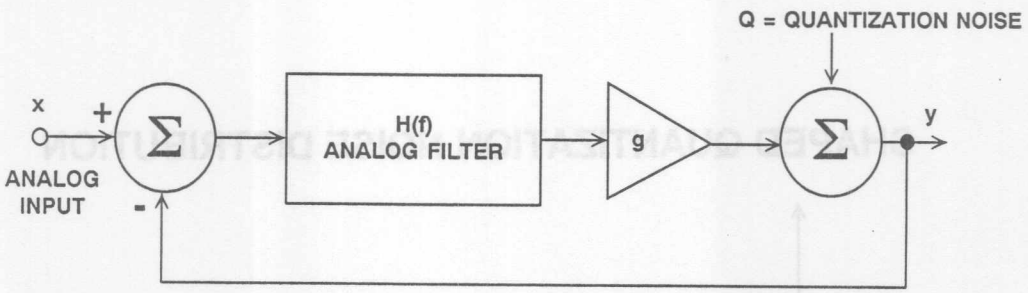


Figure 14.7

The integrator is represented as an analog filter with a transfer function H(f). This transfer function has an amplitude response which is inversely proportional to the input frequency. The quantizer is modeled as a gain stage and is followed by the addition of quantization noise. If we set the gain to 1, and the transfer function is represented as 1/f, the following mathematical relationship results:

$$y = \frac{x - y}{f} + Q \text{ , or by rearranging,}$$

$$y = \frac{x}{f+1} + \frac{Qf}{f+1}.$$

Note that as frequency f approaches zero, the output approaches x with no noise component. At higher frequencies, the value of x is reduced, and the value of the noise component is increased. At high frequency, the output consists primarily of quantization noise. In essence, the analog filter has a low pass effect on the signal and a high pass effect on the quantization noise. The analog filter of the modulator can thus be viewed as a noise shaping filter (Figure 14.8).

With analog filters in general, higher order filters offer better performance. This is also true of the sigma-delta modulator, provided certain precautions are taken. A second order sigma-delta modulator is shown in Figure 14.9, and a comparison between the noise shaping functions is shown in Figure 14.10. Figure 14.11 shows a plot of the in-band signal-to-noise ratio (dynamic range) as a function of the oversampling ratio for first, second, and third order modulators. Note that the first order transfer function has a slope of 9dB per octave, while each succeeding increase in order yields an additional 6dB/octave. Loops of third order or greater, although yielding even lower oversampling ratios, are potentially unstable, and must be designed with great care. Fortunately there is so much computation inherent in an FIR filter that it is generally possible to use spare resources in the "computer" in the FIR filter to recognize the onset of instability and take steps to damp it - but the design of such a system may not be a trivial task.

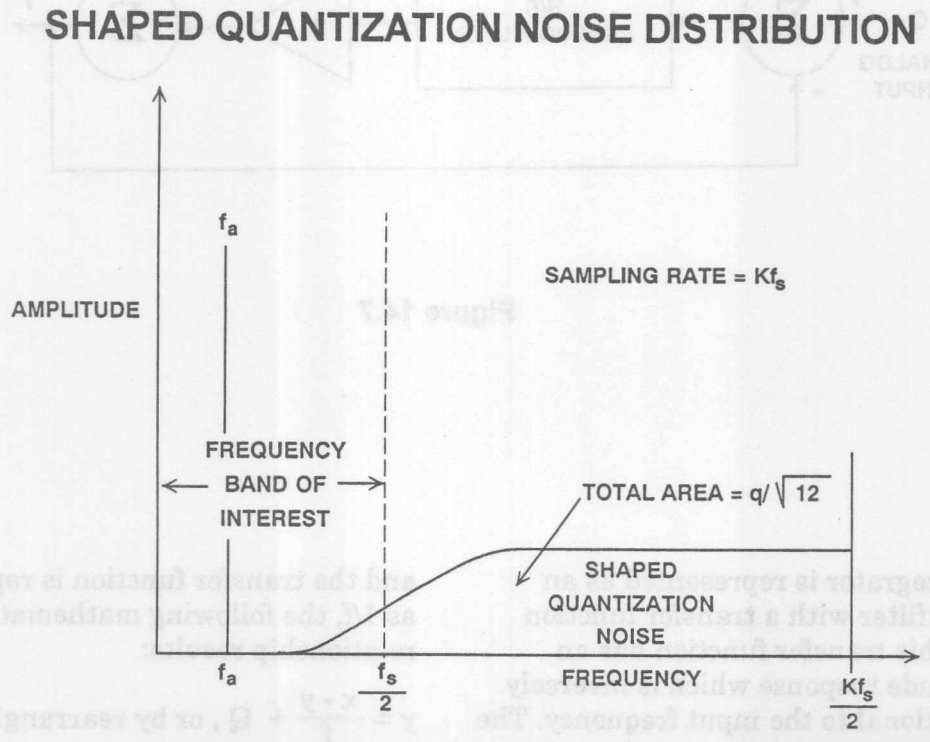


Figure 14.8

SECOND-ORDER SIGMA-DELTA MODULATOR

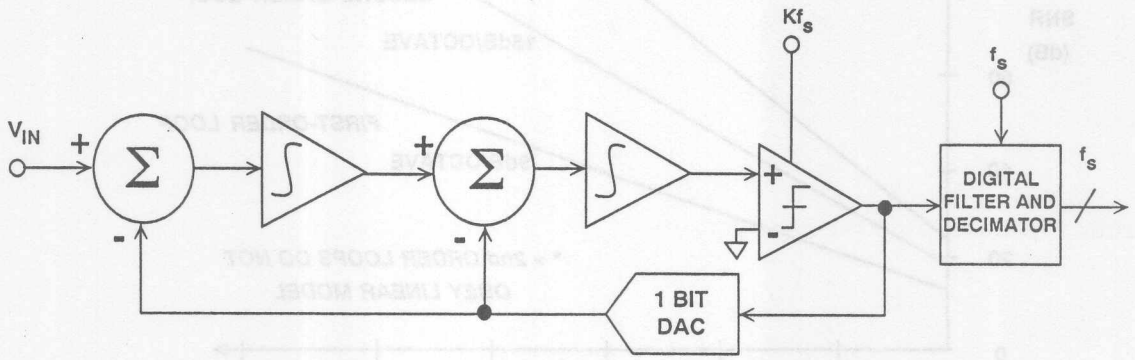


Figure 14.9

FIRST AND SECOND-ORDER NOISE SHAPING FUNCTIONS

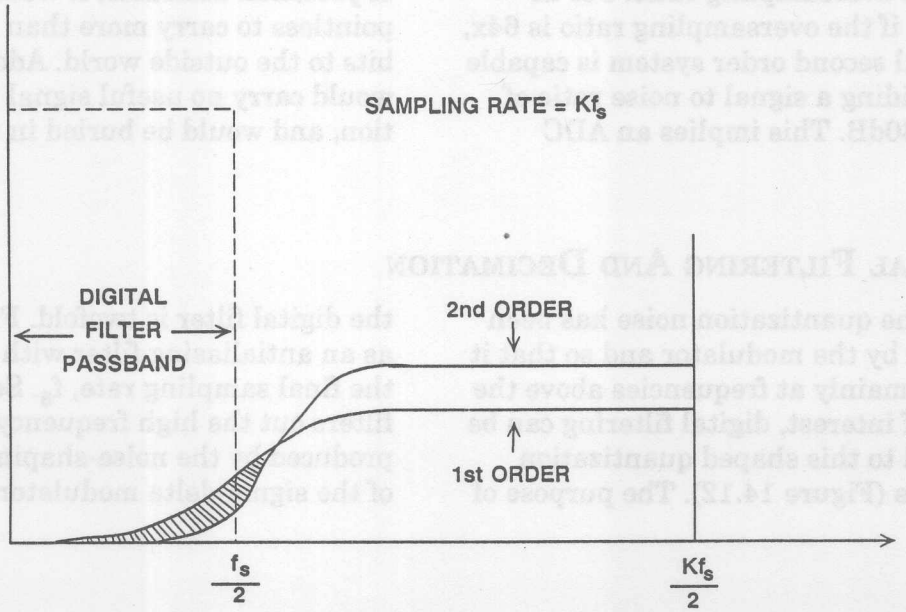


Figure 14.10

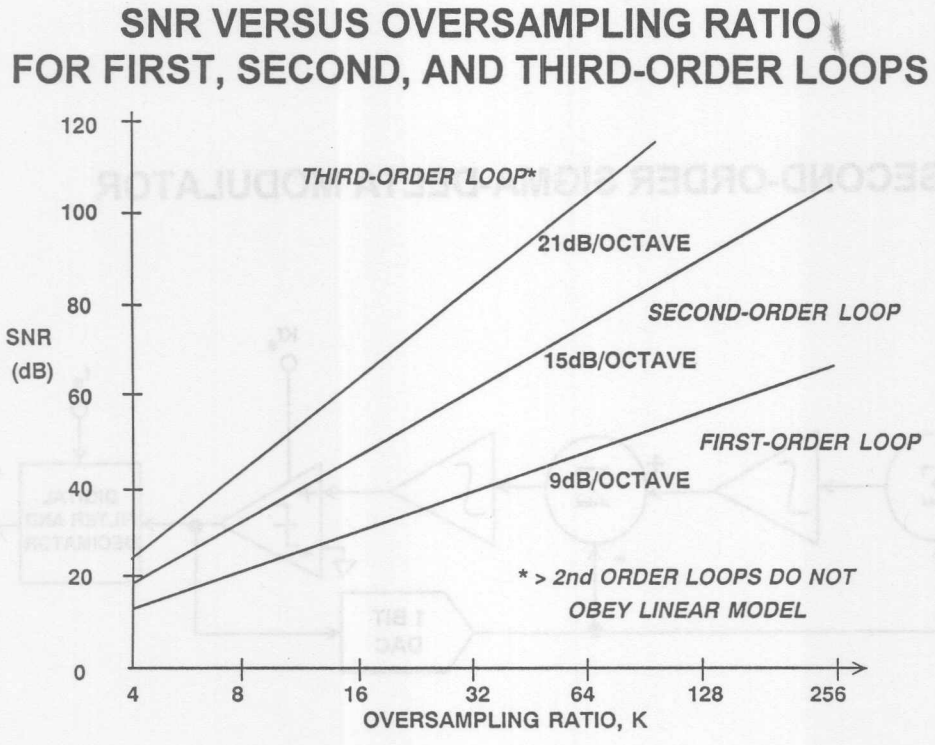


Figure 14.11

The curves in Figure 14.11 can be used to determine the approximate ADC resolution, given the modulator order and the oversampling ratio. For instance, if the oversampling ratio is 64x, an ideal second order system is capable of providing a signal to noise ratio of about 80dB. This implies an ADC resolution of approximately 13 bits. Although the filtering done by the digital filter can be done to any degree of precision desirable, it would be pointless to carry more than 13 binary bits to the outside world. Additional bits would carry no useful signal information, and would be buried in noise.

DIGITAL FILTERING AND DECIMATION

After the quantization noise has been shaped by the modulator and so that it occurs mainly at frequencies above the band of interest, digital filtering can be applied to this shaped quantization noise as (Figure 14.12). The purpose of the digital filter is twofold. First, it acts as an antialiasing filter with respect to the final sampling rate, f_S. Second, it filters out the high frequency noise produced by the noise-shaping process of the sigma-delta modulator.

EFFECTS OF DIGITAL FILTERING ON SHAPED QUANTIZATION NOISE

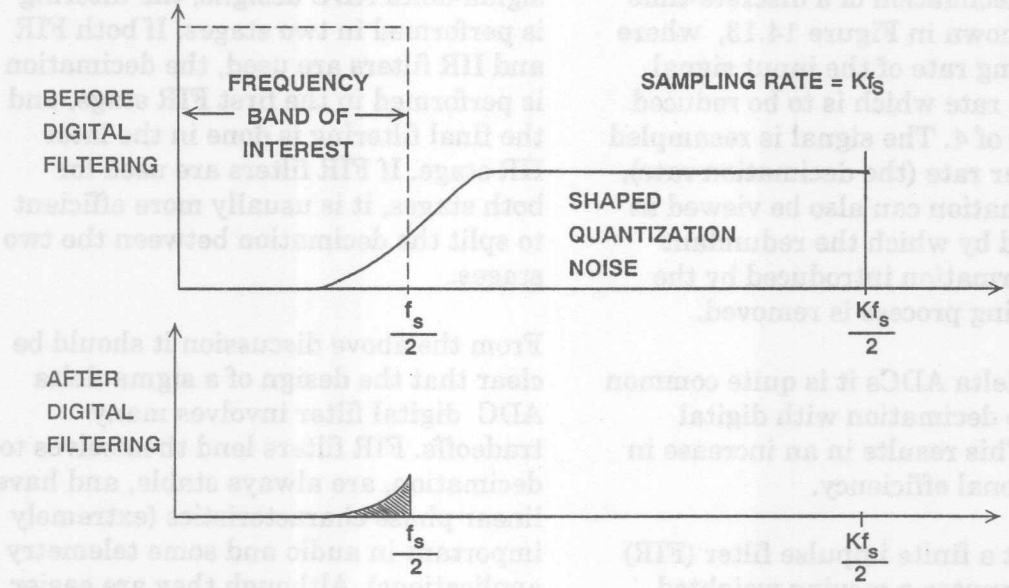


Figure 14.12

DECIMATION OF A DISCRETE-TIME SIGNAL

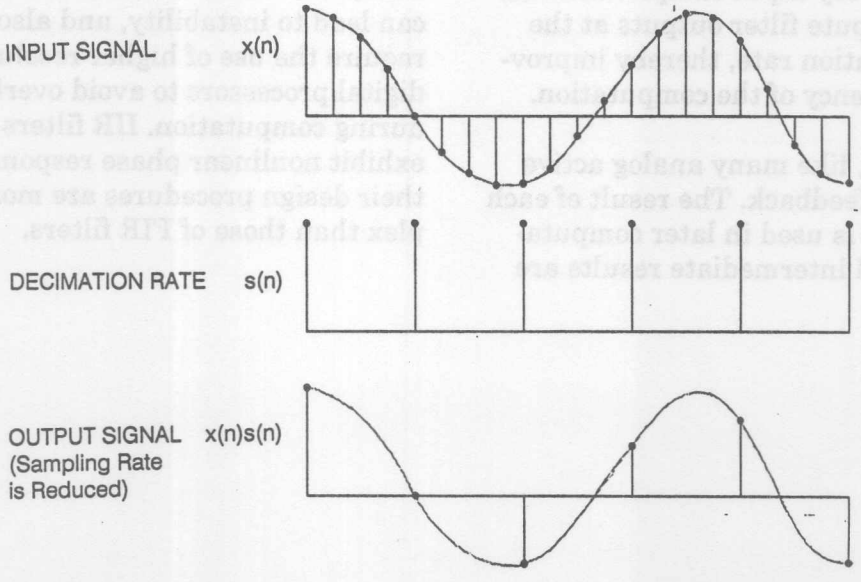


Figure 14.13

The final data rate reduction is performed by resampling the filtered output using a process called decimation. The decimation of a discrete-time signal is shown in Figure 14.13, where the sampling rate of the input signal x(n) is at a rate which is to be reduced by a factor of 4. The signal is resampled at the lower rate (the decimation rate), s(n). Decimation can also be viewed as the method by which the redundant signal information introduced by the oversampling process is removed.

In sigma-delta ADCs it is quite common to combine decimation with digital filtering. This results in an increase in computational efficiency.

Recall that a finite impulse filter (FIR) simply computes a moving weighted average (the weighting being determined by the individual filter coefficients) of the input samples. Normally, there is one filter output for every input sample. If, however, we wish to decimate the filter output by digitally resampling at a lower rate, it is no longer necessary to compute a filter output for every input sample. Instead, we only compute filter outputs at the lower decimation rate, thereby improving the efficiency of the computation.

An IIR filter, like many analog active filters, uses feedback. The result of each computation is used in later computations, and all intermediate results are used. It is therefore impossible to perform decimation as part of the filtering process in an IIR filter. In some sigma-delta ADC designs, the filtering is performed in two stages. If both FIR and IIR filters are used, the decimation is performed in the first FIR stage, and the final filtering is done in the later IIR stage. If FIR filters are used for both stages, it is usually more efficient to split the decimation between the two stages.

From the above discussion it should be clear that the design of a sigma-delta ADC digital filter involves many tradeoffs. FIR filters lend themselves to decimation, are always stable, and have linear phase characteristics (extremely important in audio and some telemetry applications). Although they are easier to design, they generally require more stages to realize a given transfer characteristic than an IIR filter. On the other hand, the IIR filter employs feedback which eliminates the possibility of decimation within the filter, but makes the filter more efficient (better filter performance with fewer calculations). The feedback used in IIR filters can lead to instability, and also may require the use of higher resolution digital processors to avoid overflow during computation. IIR filters often exhibit nonlinear phase response, and their design procedures are more complex than those of FIR filters.

SIGMA-DELTA ADC DIGITAL FILTERING AND DECIMATION

FIR Filters:
- Easy to Design
- Easy to Incorporate Decimation
- Linear Phase Response
- Large Number of Coefficients May Be Required

IIR Filters:
- Stability, Overflow Considerations
- Cannot Decimate Internally Due to Feedback
- More Efficient than FIR Filters
- Non-Linear Phase Response

Combinations:
- 2-Stage FIR Filters
- FIR Filter Followed by IIR Filter
- 2-Stage IIR Filters

Figure 14.14

IDLE TONES IN SIGMA-DELTA ADCs

In our discussion of sigma-delta ADCs up to this point, we have made the assumption that the quantization noise produced by the sigma-delta modulator is random and uncorrelated with the input signal. Unfortunately, this is not entirely the case, especially for the low-order modulators. Consider the case where we are averaging 16 samples of the modulator output in a 4 bit sigma-delta ADC. Figure 14.15 shows the bit pattern for two input signal conditions: an input signal having the value 8/16, and an input signal having the value 9/16. In the case of the 9/16 signal, the modulator output bit pattern has an extra "1" every 16th output. This will produce energy at $f_S/16$, which translates into an unwanted tone which is known as an *idle* tone. If the oversampling ratio is less than 16, this tone will fall into the passband. Figure 14.16 shows the correlated idling pattern behavior for a first order sigma-delta modulator, and Figure 14.17 shows the less correlated pattern for a second-order modulator. The higher the order of a ΣΔ ADC the less the problem of idle tones, although even the highest order devices are not always entirely free of them. For this reason, and because of their relatively poor (i.e. large) oversampling ratio, first order ΣΔ ADCs are not often used.

REPETITIVE BIT PATTERN IN SIGMA-DELTA MODULATOR OUTPUT

16 SAMPLES OF SIGMA-DELTA MODULATOR DATA OUTPUT STREAM		BINARY EQUIVALENT
1010101010101010... 8/16	=	1000
1010101010101011... 9/16	=	1001

REPEATS EVERY 16 SAMPLES

Figure 14.15

IDLING PATTERNS FOR FIRST-ORDER SIGMA-DELTA MODULATOR (INTEGRATOR OUTPUT)

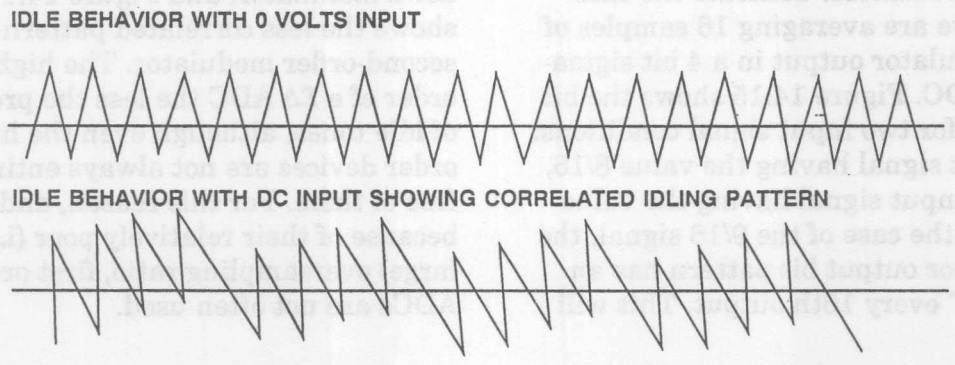


Figure 14.16

IDLING PATTERNS FOR SECOND-ORDER SIGMA-DELTA MODULATOR (SECOND INTEGRATOR OUTPUT)

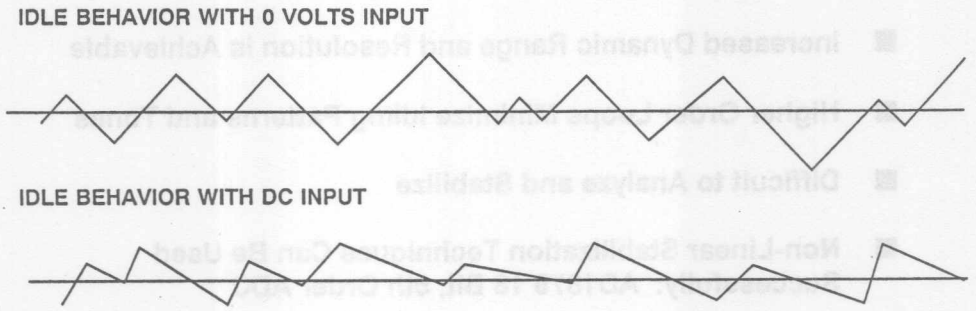


Figure 14.17

HIGHER ORDER MODULATOR LOOPS

In order to achieve wide dynamic range, sigma-delta modulator loops greater than second-order are necessary, but present real design challenges. First of all, the simple linear models previously discussed are no longer fully accurate. Loops of order greater than two are generally not unconditionally stable under all input conditions. The instability arises because the comparator is a non-linear element whose effective "gain" varies inversely with the input level. This mechanism for instability causes the following behavior: if the loop is operating normally, and a large signal is applied to the input that overloads the loop, the average gain of the comparator is reduced. The reduction in comparator gain causes loop instability, which persists even when the signal that caused it is removed. In practice, such a circuit would normally oscillate on power-up due to turn-on transients.

HIGHER ORDER LOOP CONSIDERATIONS (>2)

- Increased Dynamic Range and Resolution is Achievable
- Higher Order Loops Minimize Idling Patterns and Tones
- Difficult to Analyze and Stabilize
- Non-Linear Stabilization Techniques Can Be Used Successfully: AD1879 18 Bit, 5th Order ADC

Figure 14.18

Instability in the AD1879 fifth-order modulator is sensed by counting the number of consecutive ones or zeros in the modulator bit stream. A sufficiently long string of either ones or zeros indicates modulator instability. This triggers circuitry which resets the integrators to restore stability.

DESCRIPTION OF THE AD776 THIRD-ORDER SIGMA-DELTA ADC

The AD776 is a general purpose 16 bit, 100kSPS sigma-delta ADC designed for DSP applications. A block diagram is shown in Figure 14.19 and key specifications are summarized in Figure 14.20.

In the AD776, the output of the one-bit quantizer (6.4MHz data rate) is first passed through a 16-tap comb filter whose output is decimated by a factor of 16. The comb filter is a simple moving average filter and has the response shown in Figure 14.21. In the 400kSPS mode, the output of the comb filter provides the conversion data. In this mode, the dynamic range is equivalent to approximately 72dB, or 12 bits.

AD776 SIGMA-DELTA ADC GIVES 16-BIT, 100kSPS OUTPUT FROM FIR FILTER AND 12-BIT, 400kSPS OUTPUT FROM COMB FILTER

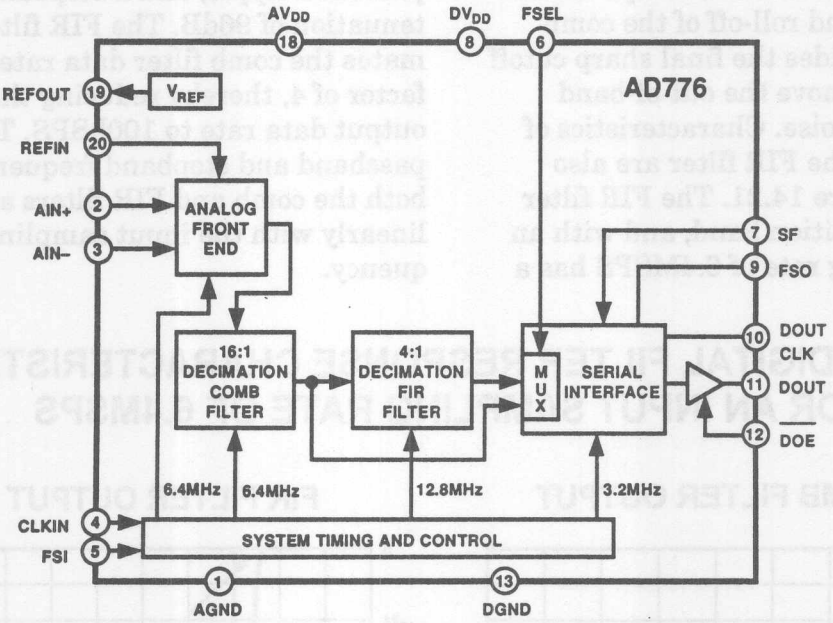


Figure 14.19

AD776 SIGMA-DELTA ADC KEY SPECIFICATIONS

14

- 16 Bits @ 100kSPS or 12 Bits @ 400kSPS Output Rates
- 64X Oversampling
- Third-Order Noise Shaping
- 90dB SNR, –100dBc Distortion For Up To 45kHz Inputs
- Single +5V Supply, 350mW Power Dissipation

Figure 14.20

In the 16 bit, 100kSPS mode, the comb filter serves as the input to the 255-tap FIR filter. The FIR filter compensates for the passband roll-off of the comb filter and provides the final sharp cutoff required to remove the out-of-band quantization noise. Characteristics of the output of the FIR filter are also shown in Figure 14.21. The FIR filter has a 9% transition band, and with an input sampling rate of 6.4MSPS has a 45.5kHz passband cutoff frequency, 50kHz stopband frequency, 0.003dB passband ripple, and a stopband attenuation of 96dB. The FIR filter decimates the comb filter data rate by a factor of 4, thereby reducing the final output data rate to 100kSPS. The passband and stopband frequencies of both the comb and FIR filters scale linearly with the input sampling frequency.

AD776 DIGITAL FILTER RESPONSE CHARACTERISTICS FOR AN INPUT SAMPLING RATE OF 6.4MSPS

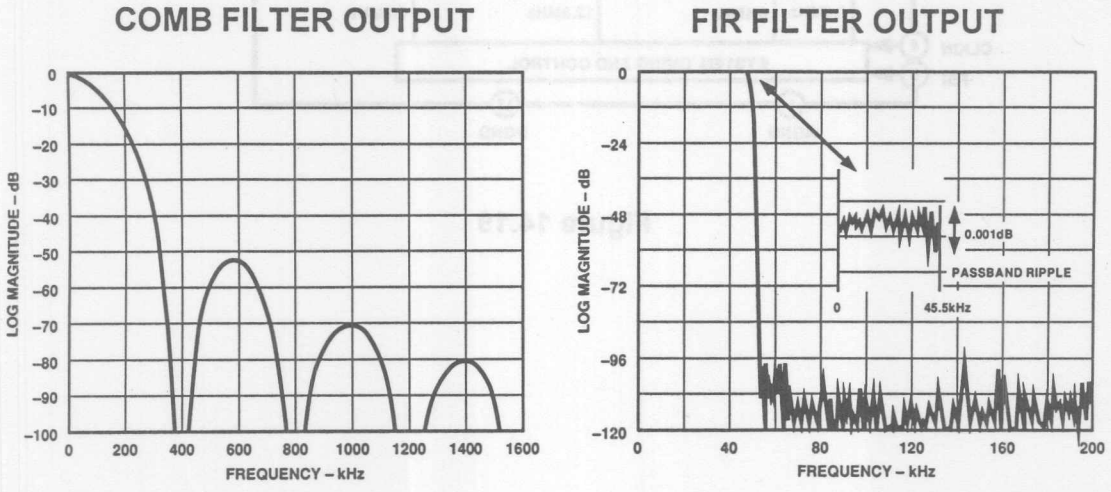


Figure 14.21

The internal digital filters in sigma-delta ADCs often limit their usefulness in applications requiring a multiplexed analog input. Figure 14.22 shows measured group delay and the settling time of the AD776 comb filter and FIR filter outputs. When a multiplexer switches between adjacent channels, it may present a fullscale step-function input to the ADC. For the AD776 FIR filter output, 680µs is required for the ADC to settle from a step-function input. This limits the maximum switching rate of the multiplexer to 1/680µs = 1.47kHz (neglecting the settling time of the multiplexer itself).

For data acquisition systems using analog multiplexers in front of the ADC, faster switching speeds can be obtained using non-sigma-delta ADCs with wide bandwidth front ends such as the AD7884/AD7885, or the AD676/AD677. These converters use traditional architectures, and their settling time is not limited by a built-in digital filter.

AD776 SIGMA-DELTA ADC DIGITAL FILTER GROUP DELAY AND SETTLING TIME CHARACTERISTICS

	Group Delay	Settling Time
Comb Filter Output	13.5µs	17µs
FIR Filter Output	340µs	680µs

Figure 14.22

The AD776 analog front-end sigma-delta modulators use a switched-capacitor architecture on both the signal and the reference inputs. In order to understand the implications on the input drive circuits, Figure 14.23 shows the basic circuit for a single-ended switched capacitor integrator. The capacitor is switched at the oversampling frequency, f_S, and acts as a resistor having a resistance equal to $1/Cf_S$. The integrator time constant is therefore determined by capacitance *ratios* which can be accurately controlled in a CMOS process. The resistance value is inversely proportional to the oversampling frequency. The switched capacitor is implemented in CMOS using the T-switch circuit shown in Figure 14.24. Because the input signal to the switch modulates the FET bias voltages, the charge injected into the drive amplifier (external to the ADC) is signal-dependent.

SINGLE-ENDED SWITCHED CAPACITOR INTEGRATOR

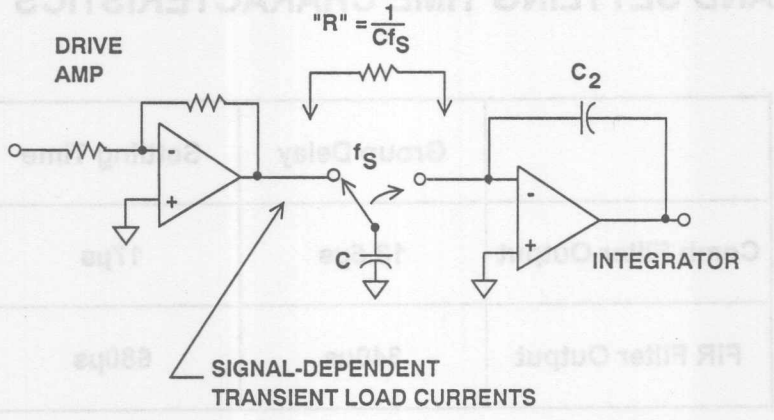


Figure 14.23

CMOS IMPLEMENTATION OF SWITCHED CAPACITOR

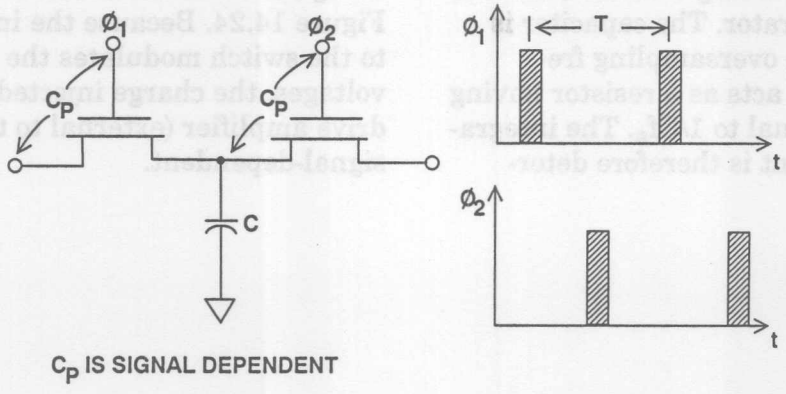


Figure 14.24

Care must therefore be taken in driving both the Analog Input of the AD776 and the Reference Input. Best performance is obtained when the Analog Input of the AD776 is driven differentially (Figure 14.25). The AD712 op amp has low distortion as well as fast settling time and low output impedance at high frequencies. The fast settling time and low output impedance is required because of the charge injection due to the switched capacitors. The nominal input voltage range of the AD776 is ±0.875V (differential) centered around a common-mode voltage of +2.5V.

The AD780 2.5V reference is used to supply the +2.5V bias voltage to the AD712s as well as provide an external reference to the AD776. While the AD776 internal reference is adequate for most applications (simply connect REFOUT to REFIN), power supply rejection and overall regulation may be improved by using an external reference such as the AD780. In either case, the REFIN pin should be bypassed to a low-impedance ground plane with a 100µF capacitor to absorb the transients produced by the internal switched capacitors.

SINGLE-ENDED TO DIFFERENTIAL DRIVE CIRCUIT FOR THE AD776 SIGMA-DELTA ADC

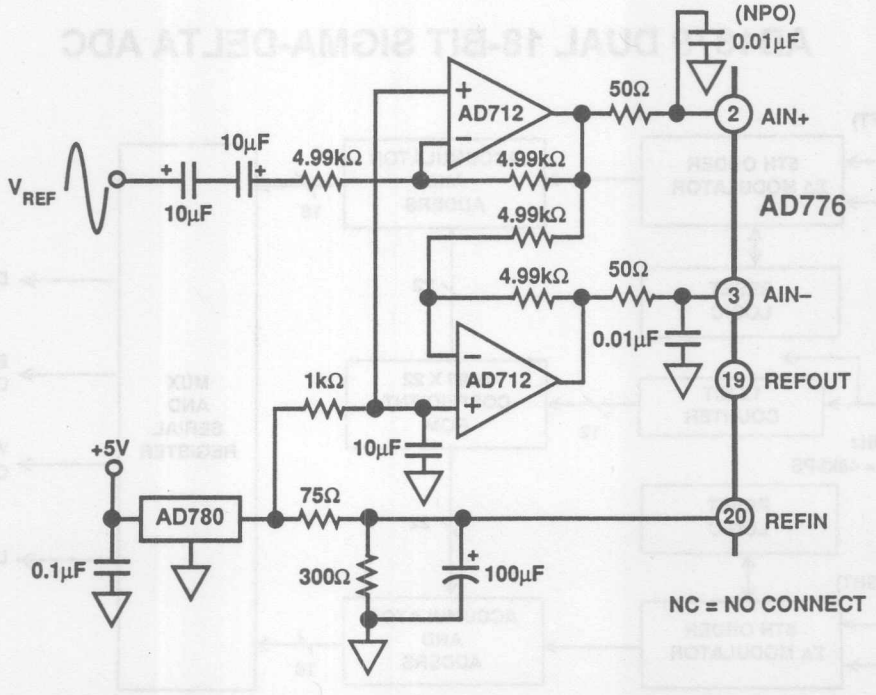


Figure 14.25

DESCRIPTION OF AD1879 18 BIT SIGMA-DELTA AUDIO ADC

The AD1879 is a dual 18 bit sigma-delta ADC designed for professional digital audio. A block diagram of the device is shown in Figure 14.26, and performance specifications are given in Figure 14.27. The modulator is a fifth-order switched capacitor design which shapes the noise spectrum as shown in Figure 14.28. The oversampling ratio is 64x, which places the oversampling frequency at 3.072MHz for the standard audio sampling rate of 48kHz. Because of the high oversampling ratio, a single-pole analog antialiasing filter is sufficient at the input of the ADC.

For audio ADCs such as the AD1879, the digital lowpass filter cannot be implemented using standard multiply-accumulate structures. For example, we require a filter which operates at a sample rate of 3.072MHz (64 x 48kHz), is flat to 20kHz and has a stopband attenuation of over 115dB starting at 26.2kHz. If we evaluate these requirements in a standard FIR equiripple design program, the number of coefficients required is 4096. At an output sample rate of 48kHz, we would require a multiply-accumulate time of 5.1ns. This is too fast for a standard FIR filter structure to implement because of semiconductor process limitations. For this reason, we must use either a parallel processing approach where more than one multiply-accumulate is being executed at any one time, or a multi-rate approach where the decimation is done in more than one step. For the AD1879, a parallel processing approach was chosen (Reference 1). The characteristics of this filter are given in Figure 14.29, and the amplitude response in Figure 14.30.

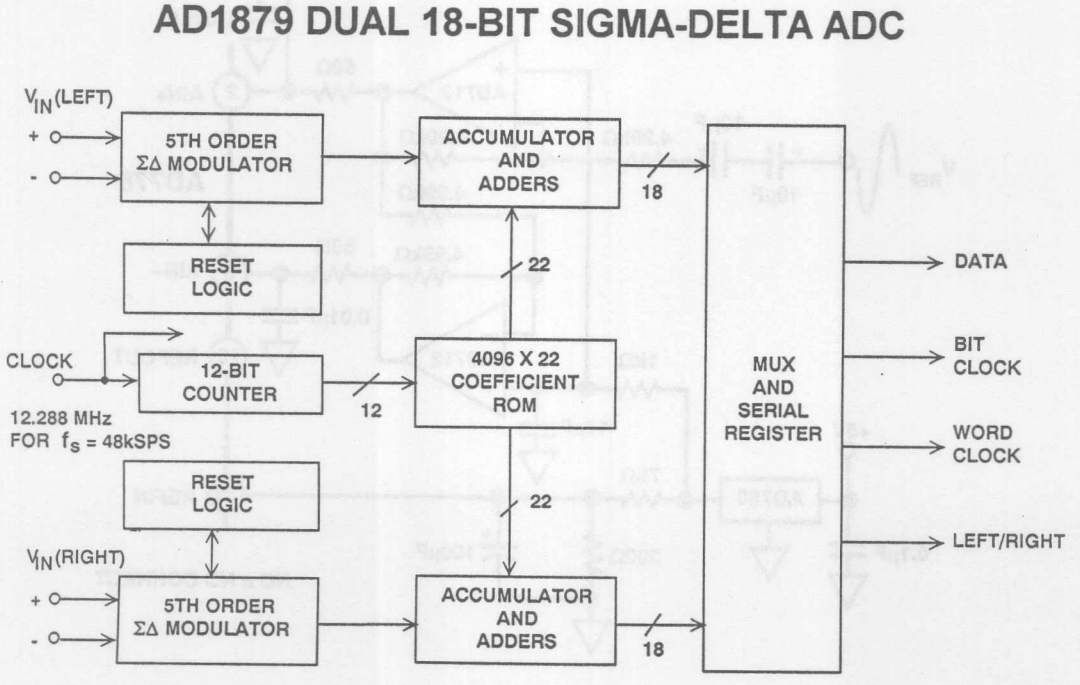


Figure 14.26

AD1879 18 BIT SIGMA-DELTA ADC KEY SPECIFICATIONS

- Two 18 Bit Channels for Stereo Digital Audio
- Interchannel Crosstalk: -105dB at 1kHz
- SNR: 103dB
- THD + N: 98dB
- Oversampling Ratio: 64x
- Output Word Rate: 55kHz Maximum
- Linear Phase Digital Filter
- Power: 900mW
- 28 Pin, 600-mil Plastic Package

Figure 14.27

AD1879 NOISE SHAPING FUNCTION

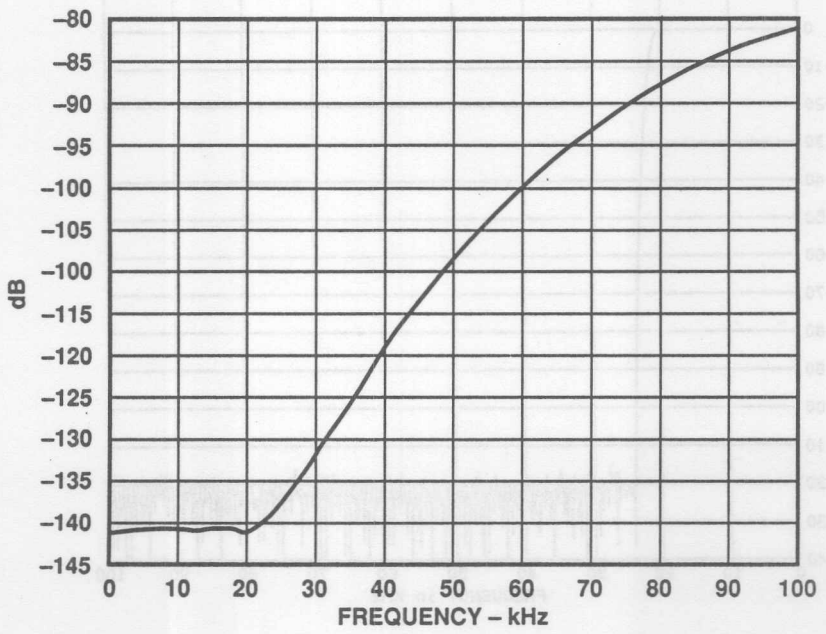


Figure 14.28

AD1879 DIGITAL FILTER CHARACTERISTICS

- Stopband Attenuation: 118dB
- Passband Ripple: 0.0004dB
- Cutoff Frequency (48kHz output rate): 21.7kHz
- Stopband Frequency (48kHz output rate): 26.2kHz
- Number of Parallel Accumulators: 64 27-bit accumulators
- Coefficient Wordlength: 22bits
- Equivalent Number of Taps: 4096

Figure 14.29

AD1879 DIGITAL FILTER RESPONSE

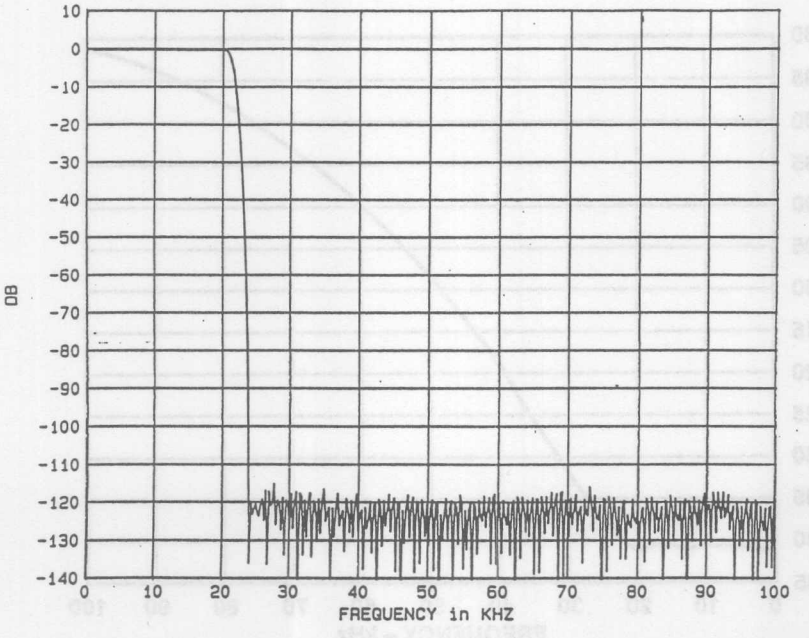


Figure 14.30

The AD1879 ADC is a compound monolithic IC. This means that the package contains two monolithic chips but no other components. One chip performs the sigma-delta modulation function, while the second chip performs the digital filtering.

The sigma-delta modulator in the AD1879 is fully differential and each channel has the equivalent input circuit shown in Figure 14.31. For optimum common mode rejection of transient load currents, the input should be driven differentially. The differentially connected 0.0047μF capacitor supplies most of the differential-mode transient currents, while the 0.01μF capacitors connected to ground absorb spike currents which are common mode. The 51Ω series resistors isolate the remaining transient current from the drive amplifiers as well as isolating the capacitive loads from the op amp outputs. These resistors must be small, however, in order to avoid distortion from the signal-dependent transients caused by charge injection. The OP-275 (dual) op amp is recommended as a precision low-distortion drive amplifier.

DIFFERENTIAL DRIVER (ONE CHANNEL) FOR THE AD1879 SIGMA-DELTA AUDIO ADC

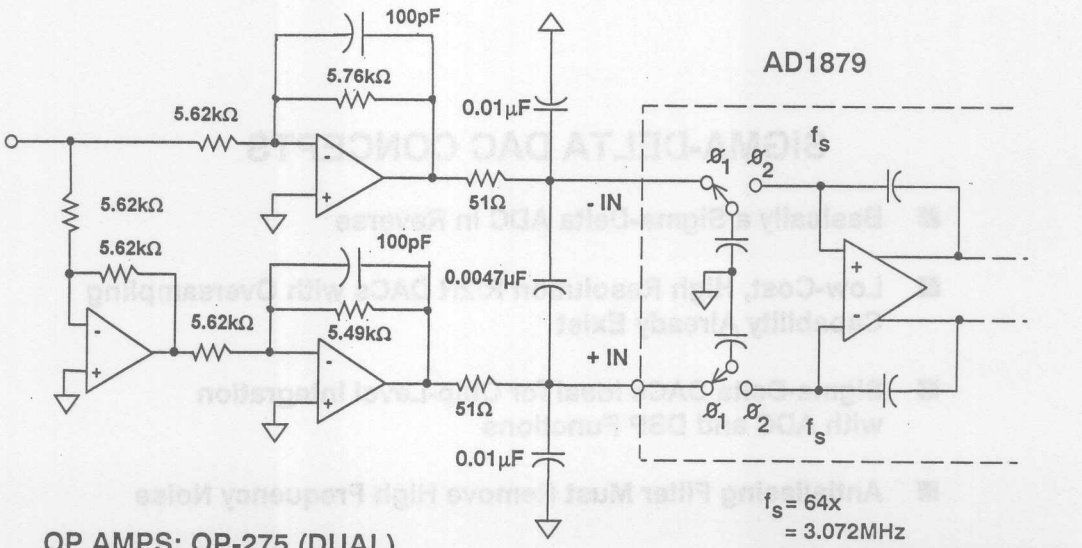


Figure 14.31

SIGMA-DELTA DACs

Sigma-delta D/A conversion can generally be thought of as the A/D conversion process in the reverse order, where all the basic functions of the digital filter and sigma-delta modulator previously discussed are the same. Sigma-delta DACs offer essentially the same advantages as sigma-delta ADCs. Because of the large oversampling ratio, the requirements on the antialiasing reconstruction filter are greatly relaxed. However, care must be taken to make sure the high frequency noise components contained in the one-bit DAC output are filtered sufficiently. If a higher order filter is required to reduce this noise, then some of the advantages of the sigma-delta DAC architecture are lost.

Accurate, low-cost, high resolution laser wafer trimmed DACs are readily available, and for this reason there has been little pressure to fully exploit sigma-delta DACs at the component level. The incentive for developing the sigma-delta DAC technology is because it is ideal for mixed-signal ICs which require the chip-level integration of ADC, DAC, and DSP functions.

SIGMA-DELTA DAC CONCEPTS

- Basically a Sigma-Delta ADC in Reverse
- Low-Cost, High Resolution R/2R DACs with Oversampling Capability Already Exist
- Sigma-Delta DACs Ideal for Chip-Level Integration with ADC and DSP Functions
- Antialiasing Filter Must Remove High Frequency Noise

Figure 14.32

The traditional approach to achieving high performance and wide dynamic range using R/2R-based DACs is shown in Figure 14.33. Due to the binary nature of the internal DAC switches, code-dependent transients, or glitches, typically produce some amount of non-filterable in-band harmonic distortion in the output spectrum. As discussed previously in the DAC section of this seminar, a technique called segmentation can greatly minimize these effects. For the ultimate in spectral purity, the remaining glitches can be removed with a sample-and-hold circuit which isolates the DAC output voltage for the duration of the glitch. This technique can eliminate the code-dependent glitches (hence harmonic distortion) at the expense of introducing some additional energy at the sampling frequency, which is filterable. A lowpass, or smoothing filter is required at the output of the SHA to prevent aliasing as well as eliminate the energy at the sampling rate. The same basic considerations used to define the antialiasing filter used ahead of an ADC apply to the smoothing filter which follows the DAC. For this reason, oversampling relaxes the smoothing filter rolloff requirements in a similar manner. In fact, 2×, 4×, and 8× oversampling techniques are currently in widespread use in compact disk players which use conventional R/2R 16, 18, and 20 bit DACs.

CONVENTIONAL DAC DEGLITCHING USING A SHA

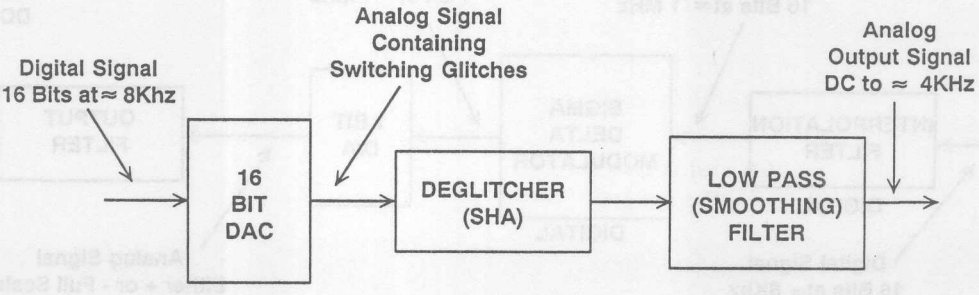


Figure 14.33

The main elements used to implement a sigma-delta DAC are shown in Figure 14.34. The example shown here is for a 16 bit DAC which is updated at an 8kHz rate to produce a voiceband output signal having a bandwidth of 4kHz. The 16 bit digital word is fed to a digital interpolation filter where the sampling rate is increased to 1.024MHz, corresponding to an oversampling ratio of 128. This process can be viewed as the reconstruction of a new, higher rate digital signal from an older, lower rate digital signal. Figure 14.35 shows the interpolation of a discrete time signal by a factor of 4. The input signal x(m) is expanded by inserting three zero-valued samples between data samples. The resulting signal w(m) is lowpass filtered to produce y(m) whose sample rate is increased by a factor of 4. This process may be thought of as *undecimation.*

The digital-input sigma-delta modulator noise-shapes the 16-bit 1.024MHz data stream and reduces the sample width to one bit. Unlike the sigma-delta modulator in a sigma-delta ADC, this modulator is all digital. The transfer function is implemented in the digital domain with an IIR filter. This digital filter performs the same modulator function as in the ADC, where the input signal is effectively lowpass filtered, and the quantization noise is high-pass filtered.

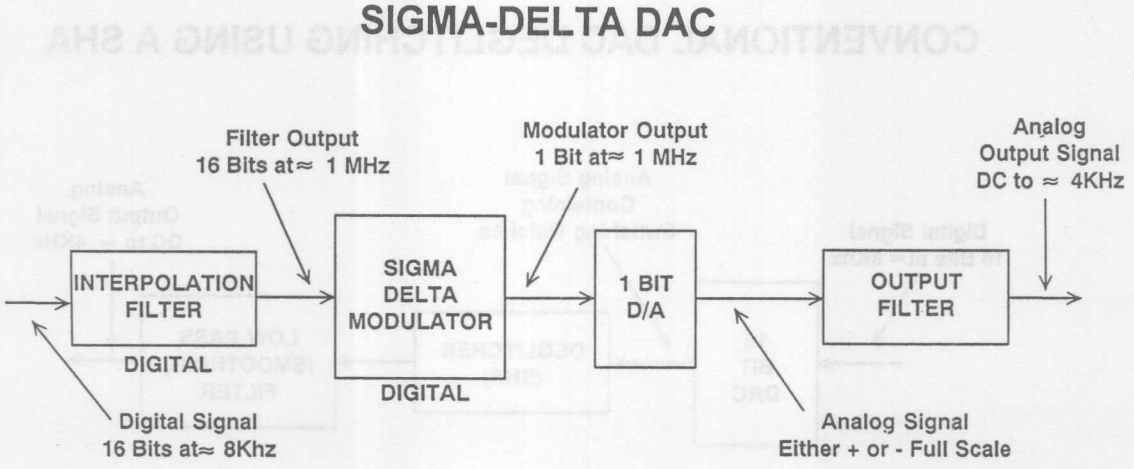


Figure 14.34

As in the case of a sigma-delta ADC, the 1 bit DAC output is useless until it is averaged in some manner. Also, there is a need to remove the shaped quantization noise present in the upper frequency area. There is also a need to reject any images above the output Nyquist rate. The analog smoothing filter performs these functions, usually in several stages. It is important for the design of this filter that the filter characteristics match the requirements of the overall system. For example, an audio system would need to have its phase and amplitude response preserved while the output filter also provides the appropriate rejection of higher frequency components. If the smoothing filter is an active filter, care must be taken that the op amps used do not introduce distortion products in the final output due to slewrate limiting and noise.

INTERPOLATION OF A DISCRETE-TIME SIGNAL

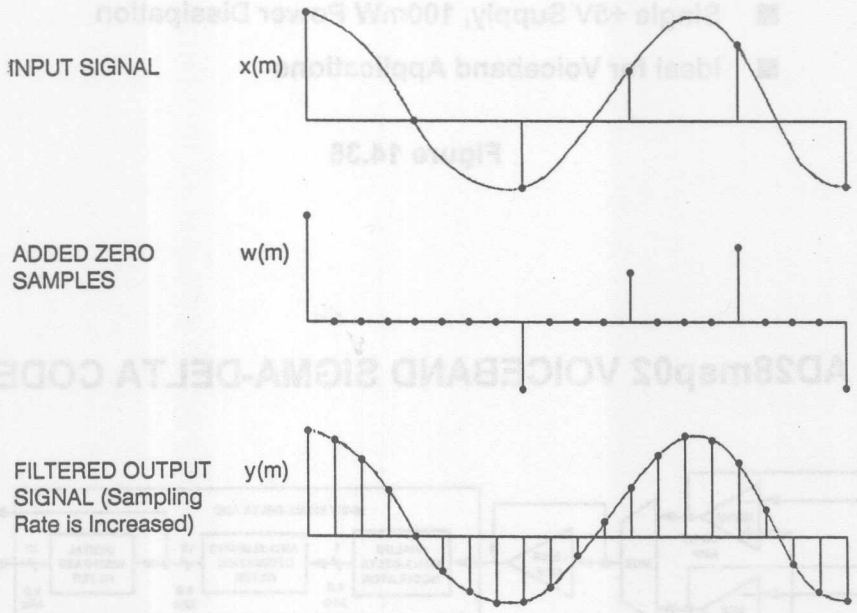


Figure 14.35

THE AD28MSP02 SIGMA-DELTA CODEC

The AD28msp02 is a mixed-signal peripheral device available based on sigma-delta design. The device is a linear codec with a 16-bit sigma-delta ADC and DAC, thereby providing a complete analog front end and back end for high performance voiceband DSP applications. Key features of the IC are summarized in Figure 14.36 and a functional block diagram is shown in Figure 14.37.

KEY FEATURES OF THE AD28msp02 SIGMA-DELTA CODEC

- 16 bit Sigma-Delta ADC
- 16 bit Sigma-Delta DAC
- On-Chip Antialiasing and Smoothing Filters
- 8kSPS Sampling Rate, 128x Oversampling Ratio
- On-Chip Voltage Reference
- 65dB SNR and THD
- Easy Interface to DSP Chips
- 24-pin DIP/SOIC Package
- Single +5V Supply, 100mW Power Dissipation
- Ideal for Voiceband Applications

Figure 14.36

AD28msp02 VOICEBAND SIGMA-DELTA CODEC

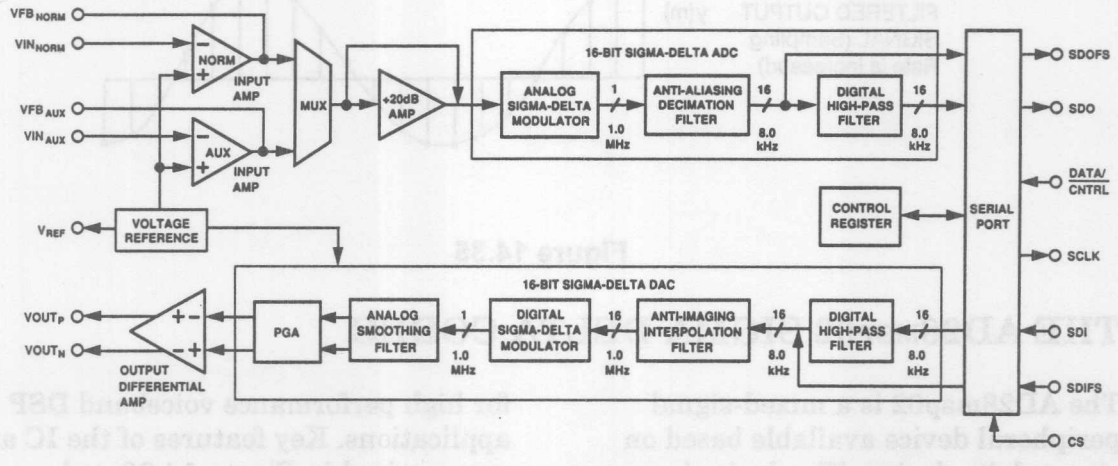


Figure 14.37

Compared to traditional μ-law and A-law codecs, the AD28msp02's linear coded ADC and DAC maintain wide dynamic range throughout the transfer function. An effective sampling rate of 8kSPS coupled with 65dB SNR and THD performance make the device attractive in many telecommunications applications such as digital cellular telephones. The part is packaged in a 24-pin DIP/SOIC package ensuring a highly integrated and compact solution to voiceband analog processing requirements. The AD28msp02 easily interfaces to the ADSP-2101, ADSP-2105, ADSP-2111, MC56001 and TMS320C25 DSP processors via its serial I/O port (SPORT).

The encoder side of the AD28msp02 consists of two selectable analog input amplifiers and a sigma-delta ADC. The gain of the input amplifiers can be adjusted with the use of external resistors from -12dB to +26dB. An optional 20dB preamplifier can be inserted before the modulator. The preamplifier and the multiplexer are configured by bits in the control register. The sigma-delta ADC consists of a sigma-delta modulator, an antialiasing decimation filter, and a digital high pass filter. The modulator noise-shapes the signal and produces 1-bit samples at 1.024MHz. This bit stream, representing the analog input, is fed to an antialiasing decimation filter which consists of two lowpass filter stages. The first stage reduces the sampling rate to 40kHz and increases the sample width to 16 bits; the second further reduces the sampling rate to 8kSPS. Each resulting sample is then loaded into the SPORT for transmission.

The decoder consists of a sigma-delta DAC and a differential output amplifier. The DAC reads 16-bit samples at an 8kHz rate from the SPORT. The samples are low- and high-pass filtered by the digital anti-imaging and high pass filters. The anti-imaging filter interpolates the sampling rate in two stages, first to 40kHz, and then to 1.024MHz. The resulting 16-bit samples are processed by the digital sigma-delta modulator which reduces the sample width to 1 bit. This bit stream is fed to an analog smoothing filter which converts the data to an analog voltage. The gain of the smoothing filter can be adjusted via the control register from -15dB to +6dB is 3dB steps.

MULTISTAGE NOISE SHAPING (MASH) SIGMA-DELTA CONVERTERS

Non-linear stabilization techniques have been successfully used to design a fifth-order sigma-delta loop in the AD1879 audio ADC. An alternative approach, called multistage noise shaping (MASH) utilizes cascaded stable first-order loops. Figure 14.38 shows a block diagram of a three-stage MASH ADC. The output of the first integrator is subtracted from the first DAC output to yield the first stage quantization noise, Q1. Q1 is then quantized by the second stage. The output of the second integrator is subtracted from the second DAC output to yield the second stage quantization noise which is in turn quantized by the third stage.

MULTI-STAGE NOISE SHAPING SIGMA-DELTA ADC (MASH)

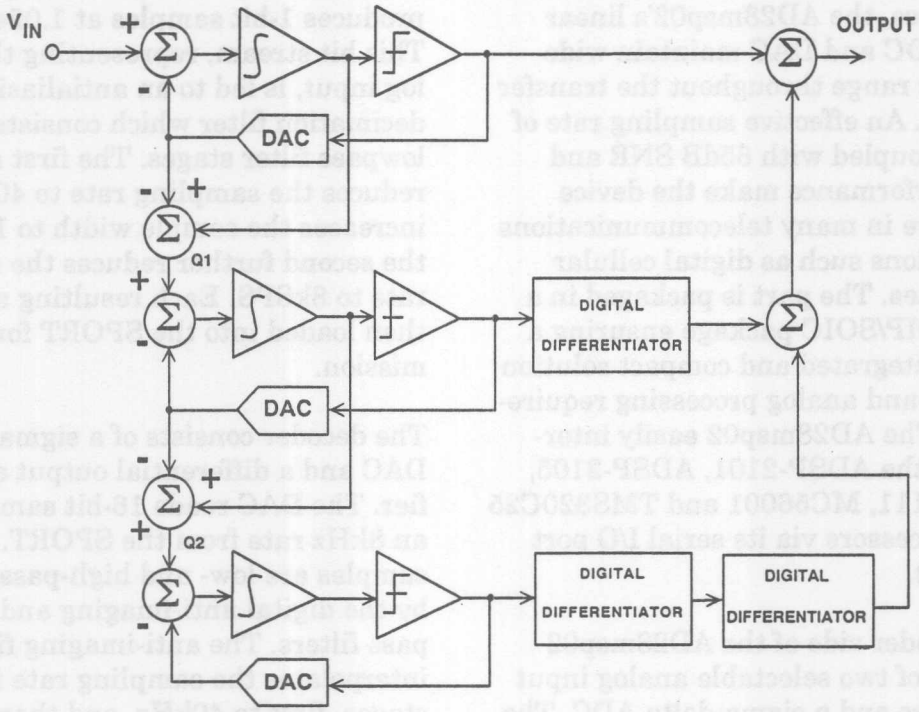


Figure 14.38

MASH TOPOLOGY VERSUS HIGHER-ORDER LOOP SIGMA-DELTA CONVERTERS

- MASH Cascades Single-Order Loops, therefore Easy to Stabilize
- Gain and Phase Matching Critical in MASH Converters for Errors to Cancel
- MASH Digital Differentiators Must Match Analog Integrators
- Single-Loop Higher Order Modulators Less Subject to Idling Patterns
- Single-Loop Higher Order Modulators More Difficult to Understand, Analyze, and Stabilize, But Can Be Done Using Non-Linear Techniques as in AD1879 (5th Order Modulator)

Figure 14.39

The output of the first stage is summed with a single digital differentiation of the second stage output and a double differentiation of the third stage output to yield the final output. The result is that the quantization noise Q1 is suppressed by the second stage, and the quantization noise Q2 is suppressed by the third stage yielding the same suppression as a third-order loop. Since this result is obtained using three first-order loops, stable operation is assured. A comparison of the MASH architecture with the higher-order single-loop architecture is given in Figure 14.39.

MULTI-BIT SIGMA-DELTA CONVERTERS

So far we have considered only sigma-delta converters which contain a single-bit ADC (comparator) and a single-bit DAC (switch). The block diagram of Figure 14.40 shows a multi-bit sigma-delta ADC which uses an n-bit flash ADC and an n-bit DAC. Obviously, this architecture will give a higher dynamic range for a given oversampling ratio and order of loop filter. Stabilization is easier, since second-order and higher loops can be used. Idling patterns tend to be more random thereby minimizing tonal effects.

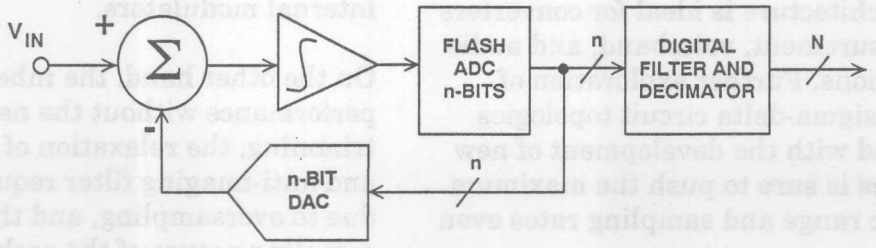


Figure 14.40

The real disadvantage of this technique is that the linearity depends on the DAC linearity, and thin film laser trimming is required to approach 16-bit performance levels. This makes the multi-bit architecture extremely impractical to implement on mixed-signal ICs. A comparison of the multi-bit versus single-bit sigma-delta converter is given in Figure 14.41.

MULTI-BIT VERSUS SINGLE-BIT SIGMA-DELTA CONVERTERS

Multi-Bit:

- Higher Dynamic Range for Given Oversampling Ratio and Loop Filter Order
- Higher Order Systems Easier to Stabilize
- Fewer Tonal Effects due to Idling Patterns
- Linearity Depends on DAC
- Thin Film Laser Trimming Required

Single-Bit:

- Perfect Linearity, no Strict Matching Requirements
- No Laser Trimming Required
- Perfect Topology for Mixed-Signal VLSI
- Non-Linear Techniques Required to Stabilize Higher Order Loops (AD1879)

Figure 14.41

SIGMA-DELTA SUMMARY

Although the concepts used in sigma-delta converters are not new by any means, their recent proliferation has been primarily driven by the need for converters which are compatible with mixed-signal VLSI chips. The sigma-delta architecture is ideal for converters for measurement, voiceband, and audio applications. Further exploration of various sigma-delta circuit topologies combined with the development of new processes is sure to push the maximum dynamic range and sampling rates even higher.

It is clear that the sigma-delta converter is not the answer to all data acquisition requirements at the present time. Upper sampling frequency is limited, thereby excluding video applications, fast multiplexing of inputs is difficult due to the settling time of the internal digital filter, and out-of-range signals may cause saturation of the internal modulators.

On the other hand, the inherently good performance without the need for laser trimming, the relaxation of antialiasing and anti-imaging filter requirements due to oversampling, and the basic sampling nature of the architecture without the need for a SHA will keep sigma-delta development moving at a rapid pace as mixed-signal ICs proliferate.

SIGMA-DELTA SUMMARY

- Inherently Excellent Linearity
- Ideal for Mixed-Signal IC Processes, no Trimming
- No SHA Required
- Upper Sampling Rate Currently Limits Applications to Measurement, Voiceband, and Audio - But Bandpass Sigma-Delta Techniques Will Change This
- Out-of-Range Signals May Cause Modulator Saturation
- Analog Multiplexing Applications Limited by Internal Filter: Use one Sigma-Delta ADC per Channel!

Figure 14.42

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SECTION 15

WIDE DYNAMIC RANGE ADC APPLICATIONS

- ACHIEVING WIDE DYNAMIC RANGE IN DIGITAL SPECTRAL ANALYSIS
- USE OF DITHER SIGNALS TO INCREASE ADC DYNAMIC RANGE
- DIRECT IF TO DIGITAL CONVERSION APPLICATIONS USING UNDERSAMPLING TECHNIQUES
- BANDPASS SIGMA-DELTA TECHNIQUES FOR DIRECT IF-TO-DIGITAL CONVERSION
- ACHIEVING WIDE DYNAMIC RANGE USING VARIABLE GAIN AMPLIFIERS
- WIDE DYNAMIC RANGE ULTRASOUND SYSTEMS

SECTION 15

WIDE DYNAMIC RANGE ADC APPLICATIONS

Walt Kester, Allen Hill, James Bryant

Many modern signal processing applications require ADCs with extremely wide dynamic range. The ADC is often the limiting factor in the performance of digital spectrum analyzers. In direct IF-to-digital receivers, the ADC must accurately digitize narrowband signals with a center frequency much greater than the Nyquist frequency of one-half the sampling rate. This is called *undersampling*, and often requires that a high-performance sample-and-hold be placed in front of the ADC to increase the dynamic range. The traditional sigma-delta architecture can be modified to yield a bandpass rather than a lowpass transfer function, thereby allowing it to be used to process IF signals well above 1MHz. Finally, variable gain, high speed, low distortion amplifiers may extend system dynamic range as in the case of ultrasound systems.

ACHIEVING WIDE DYNAMIC RANGE IN DIGITAL SPECTRAL ANALYSIS

Walt Kester, Allen Hill

Digital techniques are common in modern signal intelligence (SIGINT) and other high performance radios. The information is extracted from the signals using fast FFTs, digital filtering, and other powerful DSP techniques. One of the important and often limiting characteristics of such receivers is the inherent spectral purity and noise of the ADC. Digital spectral analysis is another application where the spectral purity and noise of the ADC may be the performance-limiting factor. In this section, we will examine the tradeoffs and illustrate some techniques which may be used to improve ADC performance.

High resolution, fast ADCs such as the AD9014 (see Figure 15.1) were designed to assist in spectral analysis by means of 14-bit digitization. The primary concern in spectral analysis applications is the spurious-free-dynamic-range (SFDR) of the ADC. The actual resolution (i.e., the number of bits) and the broadband rms noise level of the converter is often a secondary consideration. By using deep FFTs and averaging the results of a number of FFTs, the broadband random noise floor can be reduced, just as narrowing the bandwidth of an analog spectrum analyzer (usually at the expense of slower sweep rates) reduces the noise floor and allows small signals to be observed which were previously buried in the noise. For an M-point FFT, the level of the average noise component in each frequency bin ($\Delta f = f_S/M$) is $10\log_{10}(M/2)$ dB below the rms value of the random noise in the bandwidth dc to $f_S/2$.

AD9014 14-BIT, 10MSPS ADC BLOCK DIAGRAM

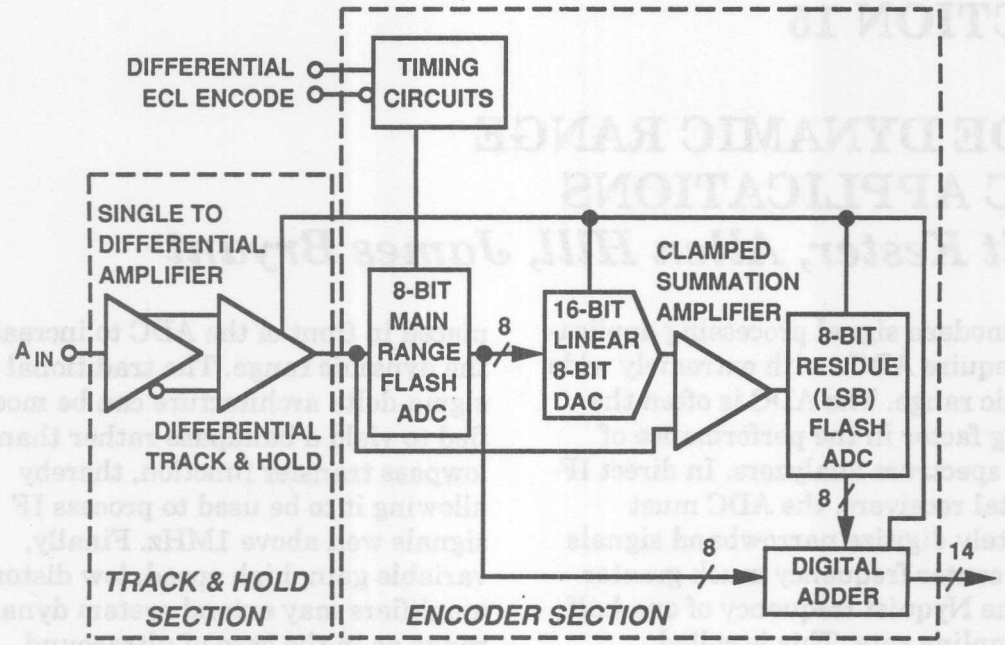


Figure 15.1

The SNR and SFDR of the AD9014 operating at 10, 12, and 14 bits is shown in Figure 15.2. Notice that the SFDR is relatively independent of the actual number of bits used, but the SNR drops to only 60dB at the 10-bit level. When selecting an ADC for spectral analysis applications, adding more bits does not always ensure better SFDR. On the other hand, there should be a sufficient number of bits present to ensure that samples from the ADC are not correlated to the input signal. There may still be correlation if the input frequency is an even sub-multiple of the sampling rate, which causes the quantization noise to be concentrated in the harmonics of the fundamental input signal frequency rather than being spread uniformly over the Nyquist bandwidth.

AD9014 SFDR AND SNR VERSUS FREQUENCY FOR 14, 12, AND 10 ACTIVE BITS

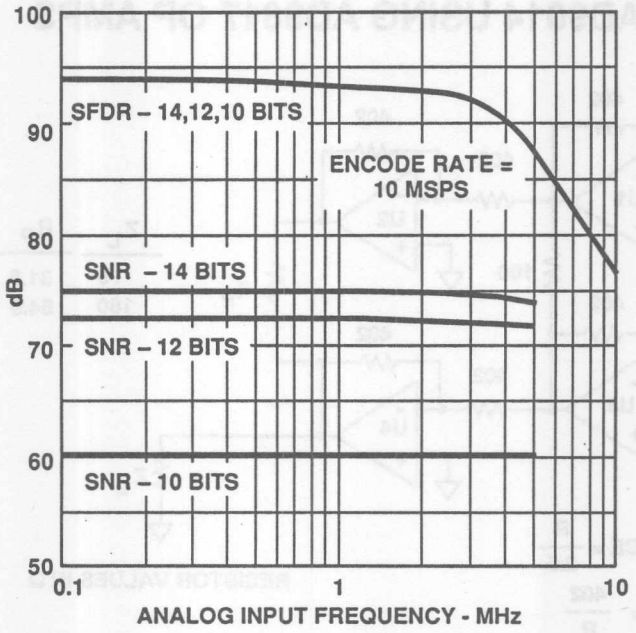


Figure 15.2

Achieving high SFDR with an ADC such as the AD9014 requires special attention to the drive amplifier. The circuit shown in Figure 15.3 is recommended in order to give ultra-low distortion levels. This circuit works well for analog input frequencies through 10MHz without degrading the AD9014's dynamic range. At 2.3MHz and 2V p-p output, all spurs are less than –100dBc. The signal path is through U3 and U4, which are set up in a series inverting configuration to cancel even-order harmonics that are generated as the loop gain diminishes with frequency. U1 and U2 supply the drive current for the outputs of U3 and U4, respectively. The closed-loop gain of U1 is 1.5 that of the closed-loop gain of U3. This gain, in conjunction with the 100Ω resistor ensures that U3 has to supply no dc output current. The value of R_p is chosen (depending on the load resistance) to ensure that U2 supplies all the output drive current of U4. The net effect is that the output stages of U3 and U4 are unloaded which minimizes their odd-harmonics. The overall gain of the driver circuit is +402Ω/R, and the input impedance is R/2.5. The output of the amplifier circuit is set up to drive either 2V p-p into 75Ω or 4V p-p into 150Ω by selecting R_p.

LOW DISTORTION DRIVE CIRCUIT (>100dBc) FOR AD9014 USING AD9617 OP AMPS

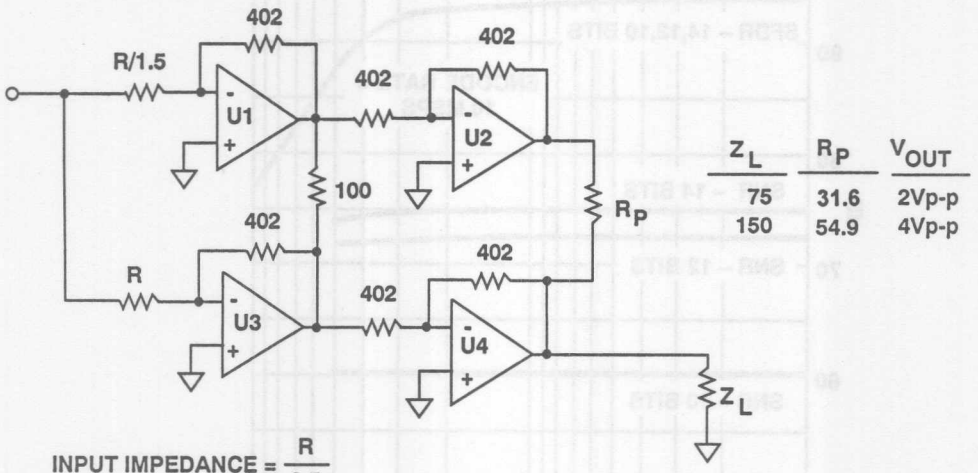
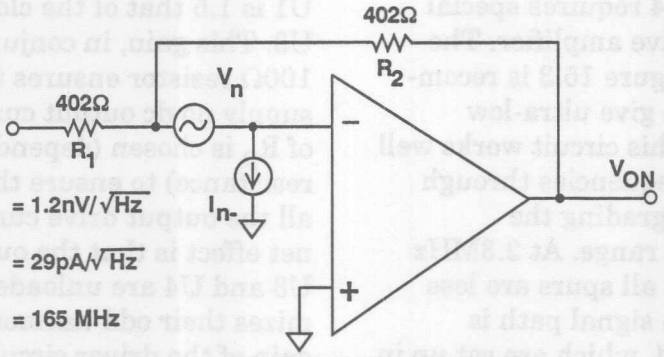


Figure 15.3

AD9617 OUTPUT NOISE SPECTRAL DENSITY



$$V_{ON} = \sqrt{BW}\sqrt{V_n^2\left[1+\frac{R_2}{R_1}\right]^2 I_{n-}^2 R_2^2}$$

$$V_{ON} = \sqrt{BW}\sqrt{(1.2\times10^{-9})^2(2)^2 + (29\times10^{-12})^2(402)^2}$$

$$V_{ON} = \sqrt{BW}\sqrt{5.76\times10^{-18} + 136\times10^{-18}}$$

$$V_{ON} = \sqrt{BW}\,(11.9nV/\sqrt{Hz})$$

Figure 15.4

The output voltage noise spectral density calculations for a single AD9617 op amp is shown in Figure 15.4. Notice that the inverting input current noise dominates the output noise.

The approximate voltage noise spectral density for the four-amplifier driver circuit is twice that of a single AD9617, or 23.6nV/√Hz. Figure 15.5 shows the driver interfaced to the AD9014. If there is no filtering, the driver voltage noise must be integrated over the entire 60MHz input bandwidth of the AD9014. This yields an input noise of 230μV rms. However, an LSB at the input to the AD9014 is only 125μV. The 230μV rms input noise corresponds to a signal-to-noise ratio of 69.8dB for a 2V p-p input signal. The SNR specification of the AD9014 is 75dB, so the driver has become the limiting factor with respect to overall SNR performance.

REDUCING QUAD DRIVER NOISE USING AN ANTIALIASING FILTER

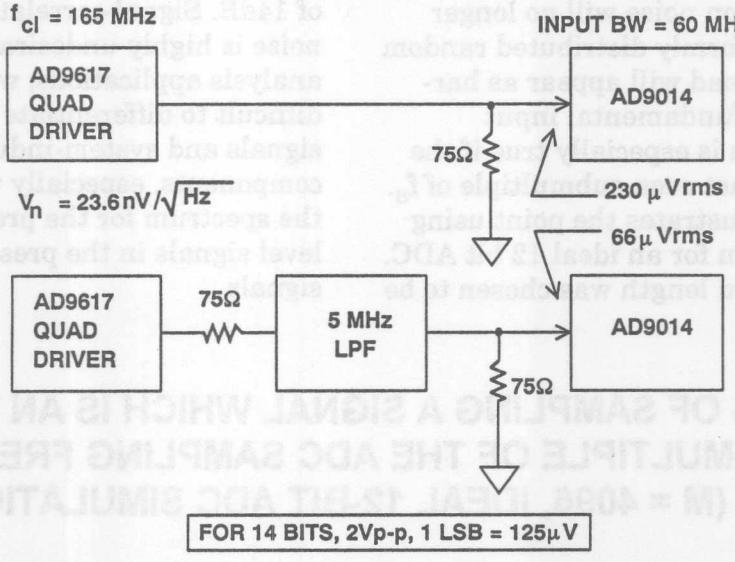


Figure 15.5

The noise contribution of the driver circuit can be significantly reduced by placing a 75Ω antialiasing filter between the driver and the AD9014 as shown in the lower half of Figure 15.5. the gain of the driver circuit must be increased by a factor of two to account for the attenuation of the filter series- and load-terminations. If the antialiasing filter is single-pole, and the cutoff frequency is 5MHz, the output noise of the AD9617 quad driver circuit is reduced to 66μV rms. This corresponds to a signal-to-noise ratio of 80.6dB, compared to a signal-to-noise ratio of 69.8dB with no filtering. Since 80.6dB > 75dB, the AD9014 is now the limiting noise contributor.

This example illustrates the significant noise reduction advantages of placing the antialiasing filter between the final driver stage and the ADC input rather than ahead of the ADC driver. This principle applies to most wide dynamic ADCs where the input bandwidth is significantly higher than the Nyquist frequency. If the extra bandwidth is not needed in the system, use the filter to reduce the high frequency noise output of the wideband drive amplifier.

USE OF DITHER SIGNALS TO INCREASE ADC DYNAMIC RANGE

Walt Kester

In the development of classical ADC quantization noise theory, the assumption is usually made that the quantization error signal is uncorrelated with the ADC input signal. If this is true, then the quantization noise appears as random noise spread uniformly over the Nyquist bandwidth, dc to $f_S/2$, and it has an rms value equal to $q/\sqrt{12}$. If, however, the input signal is locked to an non-prime integer sub-multiple of f_S, the quantization noise will no longer appear as uniformly distributed random noise, but instead will appear as harmonics of the fundamental input sinewave. This is especially true if the input is an exact even submultiple of f_S. Figure 15.6 illustrates the point using FFT simulation for an ideal 12 bit ADC. The FFT record length was chosen to be 4096. The spectrum on the left shows the FFT output when the input signal is an exact even submultiple (1/32) of the sampling frequency (the frequency was chosen so that there were exactly 128 cycles per record). The SFDR is approximately 78dBc. The spectrum on the right shows the output when the input signal is such that there are exactly 127 cycles per record. The SFDR is now about 92dBc which is an improvement of 14dB. Signal-correlated quantization noise is highly undesirable in spectral analysis applications, where it becomes difficult to differentiate between real signals and system-induced spurious components, especially when searching the spectrum for the presence of low-level signals in the presence of large signals.

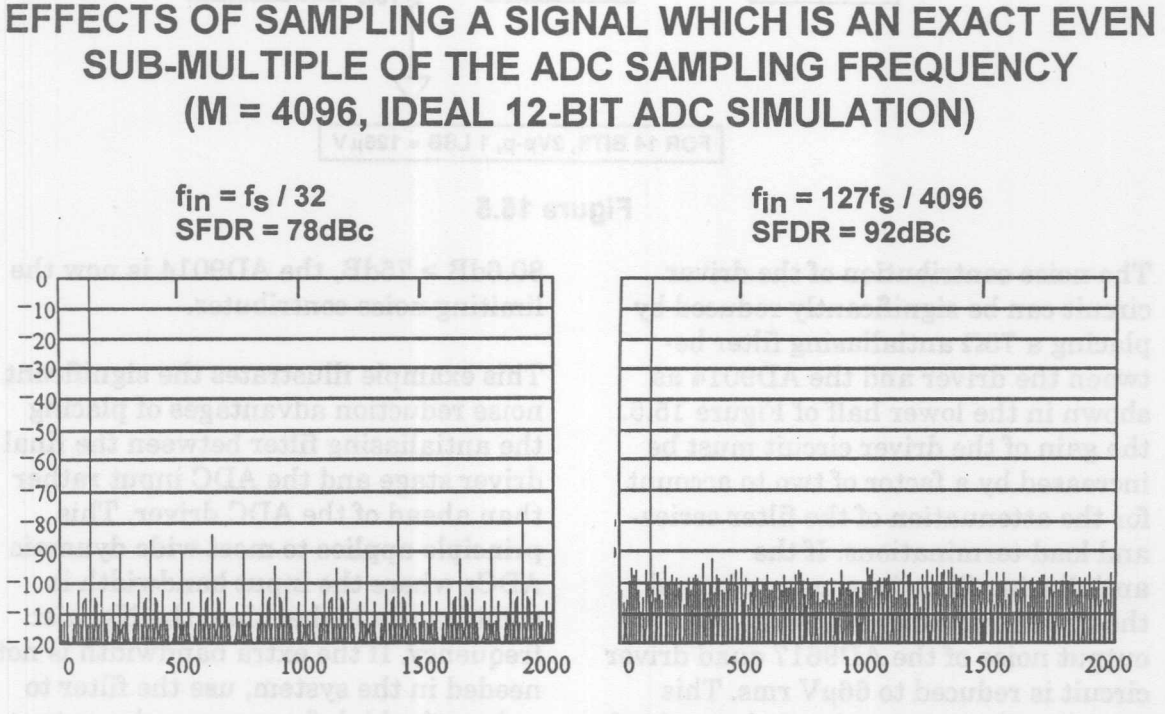


Figure 15.6

There are a number of ways to reduce this problem, but the easiest way is to add a small amount of broadband rms noise to the ADC input signal as shown in Figure 15.7. The rms value of this noise should be equal to about 1/2 LSB. The effect of this is to randomize the quantization noise and eliminate its possible signal-dependence. In many systems, there is usually enough random noise on the input signal and the sampling clock so that this happens automatically. This is especially likely when using high speed ADCs which have 12 or more bits of resolution and a relatively small input range of 2V p-p.

THE ADDITION OF GAUSSIAN WIDEBAND NOISE TO THE ADC INPUT RANDOMIZES QUANTIZATION NOISE AND REMOVES INPUT SIGNAL DEPENDENCE

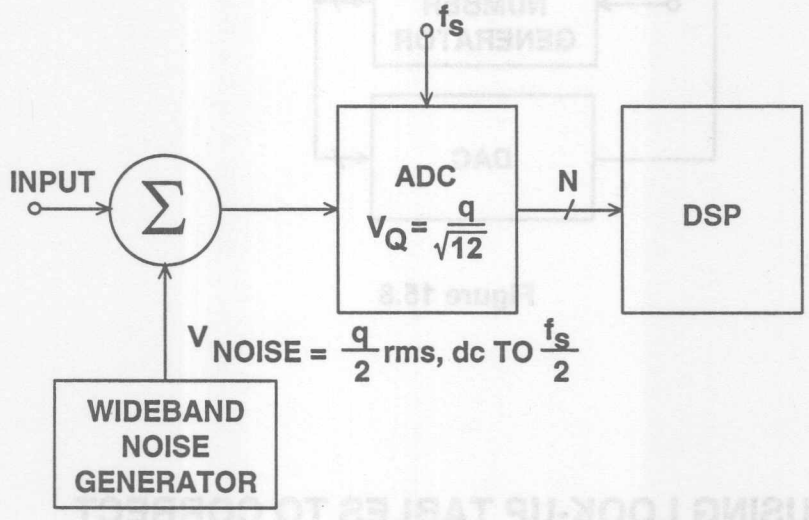


Figure 15.7

Another technique to achieve wider dynamic range in ADCs is the use of large-scale dithering as shown in Figure 15.8. This method serves to randomly distribute the ADC encoder static errors. A random number generator (RNG) provides a pseudo-random code which is loaded into a DAC and subtracted from the analog input signal. After the ADC processing is complete, the digital word is added to the resultant ADC digital word. The greater the randomization over the analog input range, the more linear the encoder becomes. However, this dynamic-range-expansion method also has its drawbacks. The encoder's SNR decreases as the linearization range increases, due to the reduced input levels. This is because the input signal level must now be chosen so that when the noise is added, the total signal never exceeds the ADC input range. The noise-generating DAC linearity also affects harmonics if the pseudo-random period is too small. In addition, this method requires the addition of several components with a resultant increase in system complexity.

USE OF LARGE-SCALE DIGITALLY-GENERATED DITHER SIGNAL TO ENHANCE ADC DYNAMIC RANGE

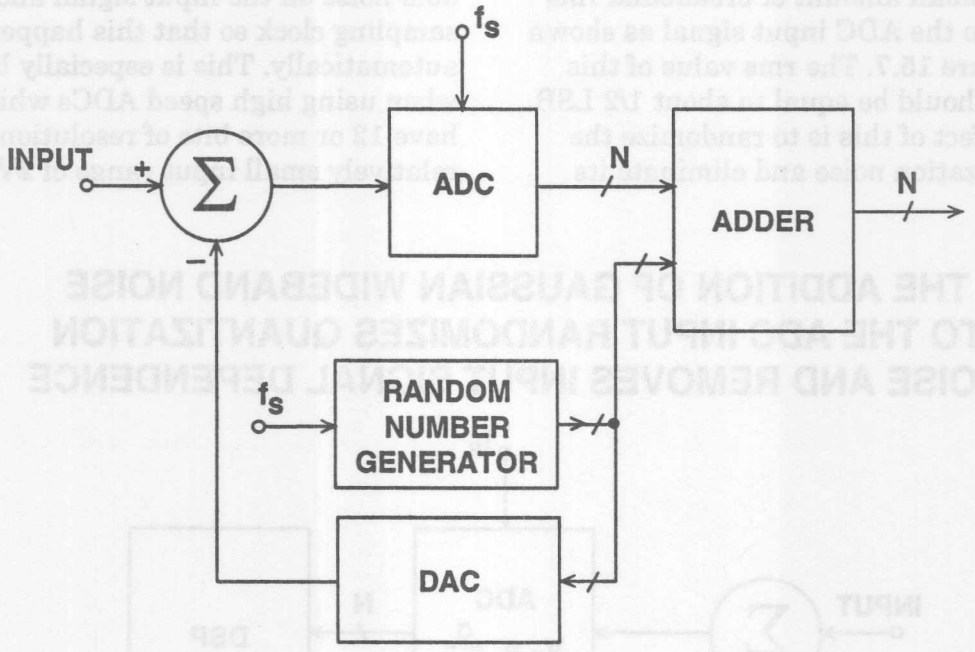


Figure 15.8

USING LOOK-UP TABLES TO CORRECT FOR ADC DYNAMIC ERRORS

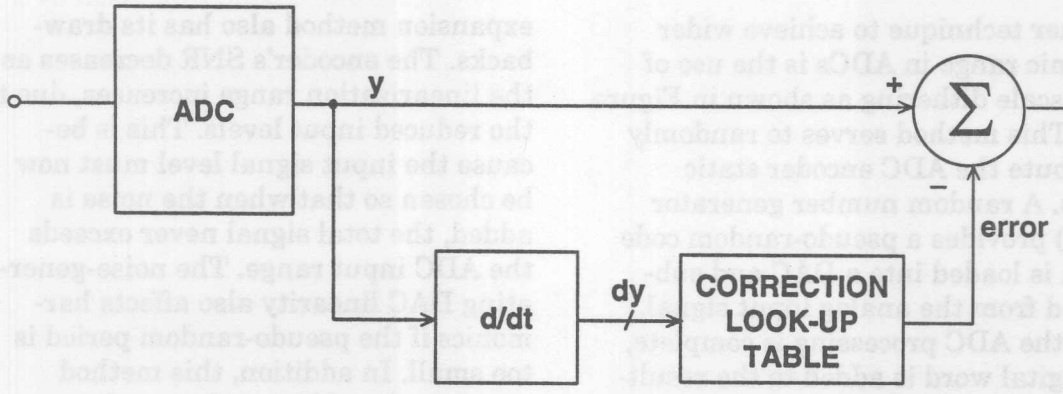


Figure 15.9

Some ADC users (see References 13, 14) have employed look-up tables (LUTs) to obtain higher performance from a given ADC. The technique consists of constructing a two-dimensional error correction table whereby the slewrate of the analog input signal serves as one axis of the table and the magnitude serves as the other axis (see Figure 15.9). Each address location holds the corrected digital output word. Once the LUT is constructed, a dedicated algorithm is applied to each digital word and to an address in the LUT to generate the corrected digital output word. This technique suffers several limitations. LUTs must be generated before data can be processed, which can be time consuming. Sources of nonlinearities within an ADC change as a function of temperature, requiring a new LUT when the temperature changes. Additional hardware, software, and circuit-board real estate to accommodate an LUT can be costly.

A final method for increasing dynamic range in ADCs for spectral analysis is the use of statistically-based continuous autocalibration techniques. The techniques involves a combination of a digitally-generated noise for error randomization and the use of continuously-updated LUTs to correct for internal encoder errors (see Reference 14). Obviously, this method involves a significant amount of additional digital circuitry and is impractical in a monolithic IC using current process technology.

DIRECT IF TO DIGITAL CONVERSION APPLICATIONS USING UNDERSAMPLING TECHNIQUES

Walt Kester, Allen Hill

Digital techniques have become widespread in radar receivers, broadband communications receivers, and mobile radio. A simplified block diagram of a traditional digital receiver using baseband sampling is shown in Figure 15.10. The mixer in the RF section of the receiver mixes the signal from the antenna with the RF frequency of the first local oscillator, LO1. The desired information is contained in relatively small bandwidth of frequencies Δf. In actual receivers, Δf may be as high as a few megahertz. The LO1 frequency is chosen such that the Δf band is centered about the IF frequency at the bandpass filter output. Popular IF frequencies are generally between 30 and 100MHz. The IF mixer then translates the Δf frequency band down to baseband where it is filtered and processed by a baseband ADC. Actual receivers generally have several stages of RF and IF processing, but the simple diagram serves to illustrate the concepts.

SIMPLIFIED DIGITAL RECEIVER USING BASEBAND SAMPLING

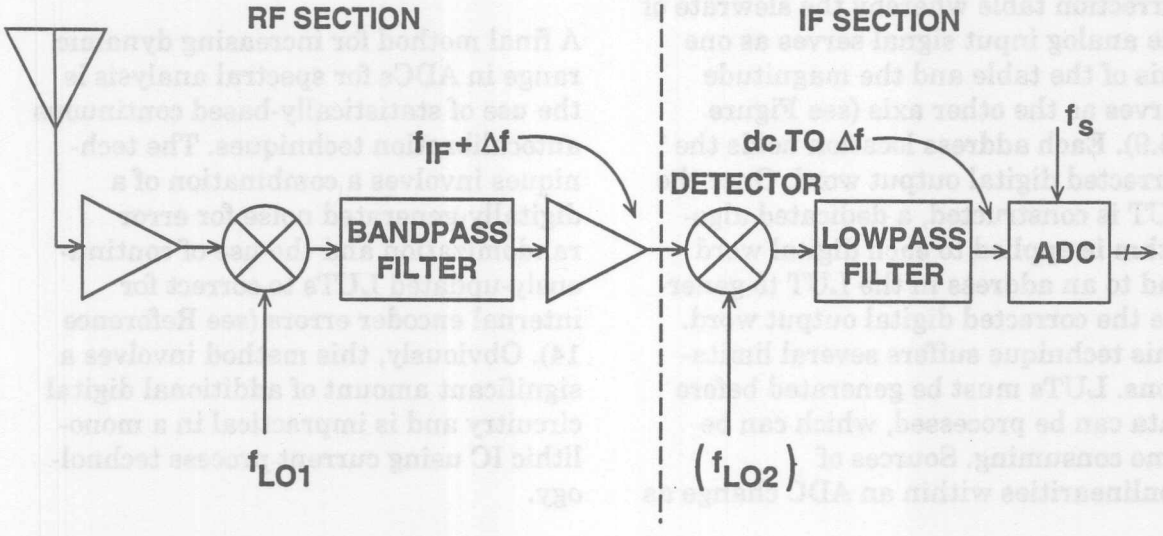


Figure 15.10

In a receiver which uses direct IF-to-digital techniques (IF sampling), the IF signal is applied directly to a wide bandwidth ADC as shown in Figure 15.11. The ADC sampling rate is chosen to be at least 2Δf. The process of sampling the IF frequency at the proper rate causes one of the aliased components of Δf to appear in the dc to $f_S/2$ Nyquist bandwidth of the ADC output. DSP techniques can now be used to process the digital baseband signal. This approach may yield an improvement in overall signal-to-noise ratio by eliminating the detector stage. There is also more flexibility in the DSP because the ADC sampling rate can be shifted to tune the exact position of the Δf signal within the baseband. The obvious problem with this approach is that the ADC must now be able to accurately digitize signals which are well outside the dc to $f_S/2$ Nyquist bandwidth which most ADCs were designed to handle. Special techniques are available, however, which can extend the dynamic range of modern ADCs to include IF frequencies. Before examining the ADC problem, we will first look at the basic theory behind undersampling.

Figure 15.12 shows four cases where a signal having about a 1MHz bandwidth is located at different portions of the frequency spectrum. The minimum sampling rate required for no aliasing is also shown. In general, the sampling frequency must be at least twice the signal bandwidth, and the sampled signal must not cross an integer multiple of $f_S/2$.

SIMPLIFIED DIGITAL RECEIVER USING IF SAMPLING

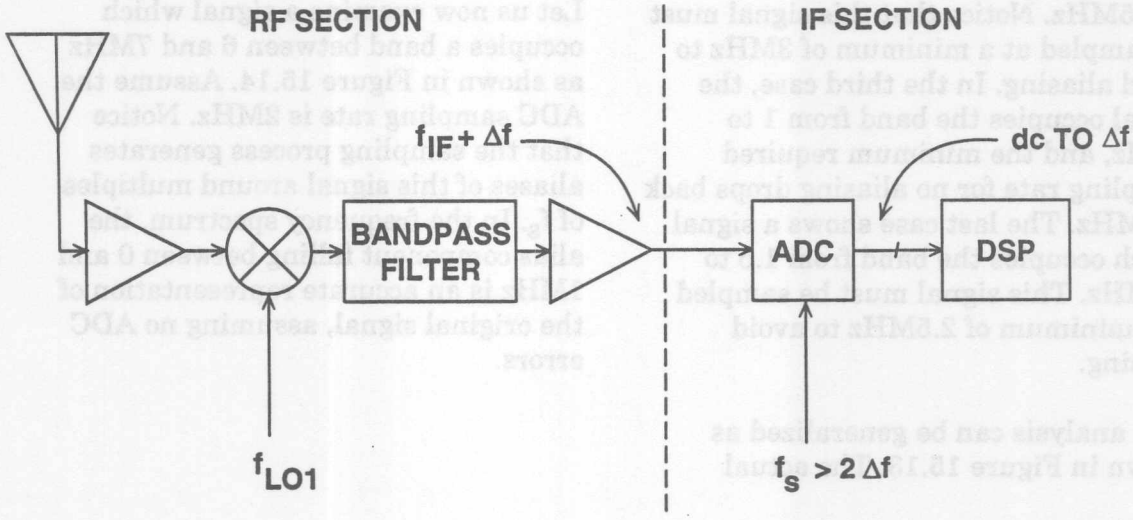


Figure 15.11

MINIMUM SAMPLING RATE REQUIRED FOR NO ALIASING OF A 1MHz BANDWIDTH SIGNAL

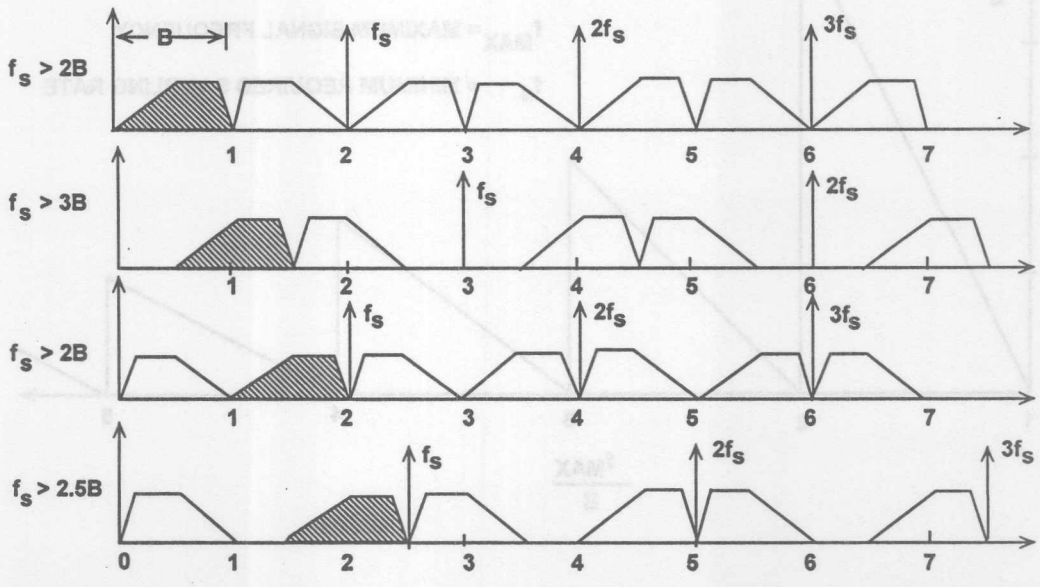


Figure 15.12

In the first case, the signal occupies a band from dc to 1MHz, and therefore must be sampled at greater than 2MSPS. The second case shows a 1MHz signal which occupies the band from 0.5 to 1.5MHz. Notice that this signal must be sampled at a minimum of 3MHz to avoid aliasing. In the third case, the signal occupies the band from 1 to 2MHz, and the minimum required sampling rate for no aliasing drops back to 2MHz. The last case shows a signal which occupies the band from 1.5 to 2.5MHz. This signal must be sampled at a minimum of 2.5MHz to avoid aliasing.

This analysis can be generalized as shown in Figure 15.13. The actual minimum required sampling rate is a function of the ratio of the highest frequency component to the total signal bandwidth.

Let us now examine a signal which occupies a band between 6 and 7MHz as shown in Figure 15.14. Assume the ADC sampling rate is 2MHz. Notice that the sampling process generates aliases of this signal around multiples of f_S. In the frequency spectrum, the alias component falling between 0 and 1MHz is an accurate representation of the original signal, assuming no ADC errors.

MINIMUM REQUIRED SAMPLING RATE AS A FUNCTION OF THE RATIO OF THE HIGHEST FREQUENCY COMPONENT TO THE TOTAL SIGNAL BANDWIDTH

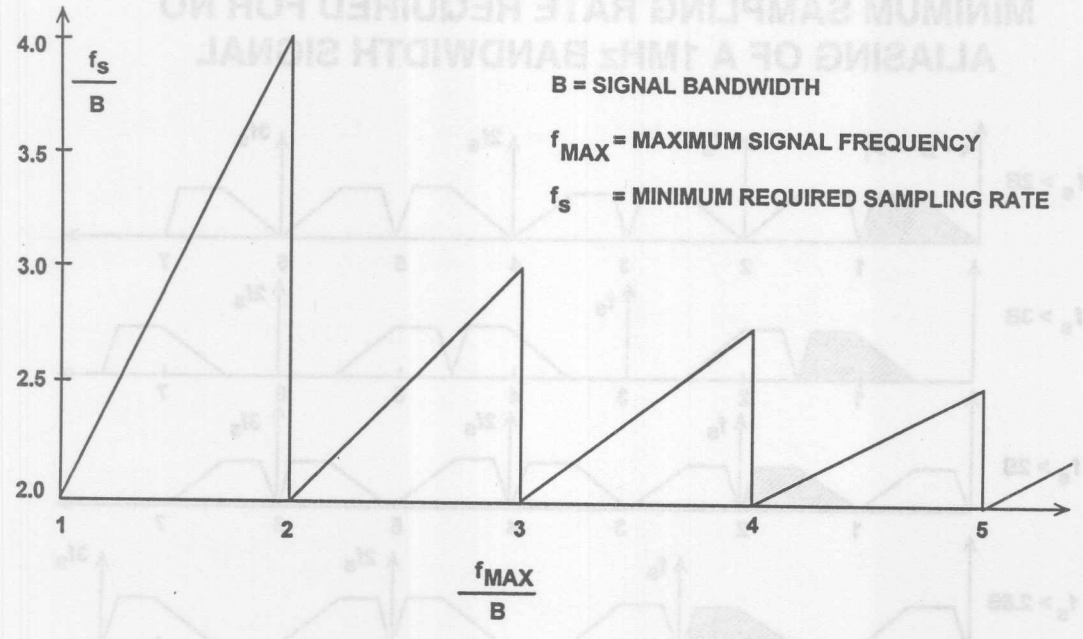


Figure 15.13

INTERMEDIATE FREQUENCY (IF) SIGNAL BETWEEN 6 AND 7 MHz IS ALIASED BETWEEN DC AND 1 MHz BY SAMPLING AT 2MSPS

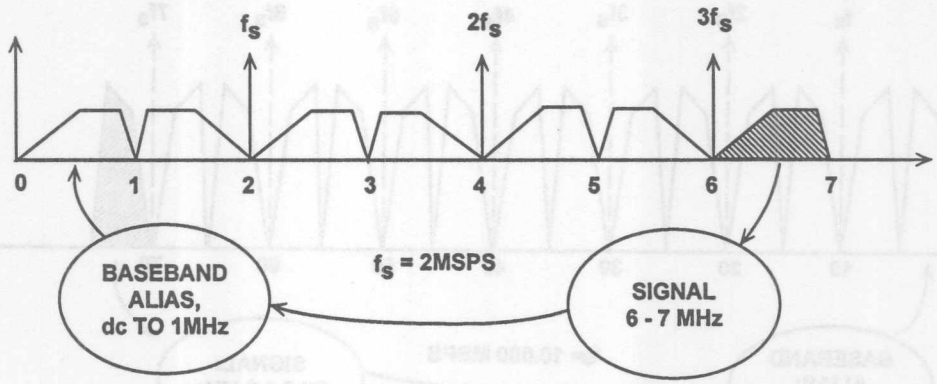


Figure 15.14

The above discussions show that although the concept of direct IF sampling is relatively straightforward, the implications for the ADC dynamic performance characteristics are significant.

Let us consider a typical example, where the IF frequency is 72.5MHz, and the desired signal occupies a bandwidth of 4MHz (B=4MHz), centered on the IF frequency (see Figure 15.15). We know from the previous discussion that the minimum sampling rate must be greater than 8MHz, probably on the order of 10MHz in order to prevent dynamic range limitations due to aliasing. If we place the sampling frequency at the lower band-edge of 70MHz (72.5–2.5), we will definitely recover the aliased component of the signal in the dc to 5MHz baseband. There is, however, no need to sample at this high rate, so we may choose any sampling frequency 10MHz or greater which is an integer sub-multiple of 70MHz, i.e, 70÷2 = 35.000MHz, 70÷3 = 23.333MHz, 70÷4 = 17.500MHz, 70÷5 = 14.000MHz, 70÷6 = 11.667MHz, or 70÷7 = 10.000MHz. We will therefore choose the lowest possible sampling rate of 10.000MHz (70÷7).

INTERMEDIATE FREQUENCY (IF) SIGNAL AT 72.5MHz (±2MHz) IS ALIASED BETWEEN DC AND 5MHz BY SAMPLING AT 10MSPS

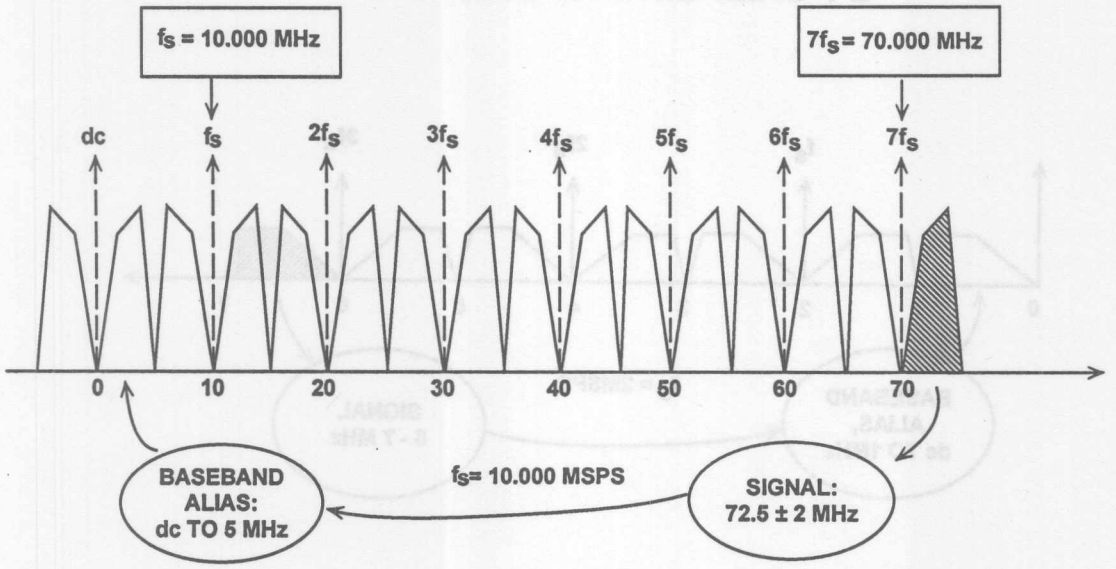


Figure 15.15

SPURIOUS FREE DYNAMIC RANGE OF THE AD9022 12-BIT, 20MSPS ADC FOR f_S = 10MSPS

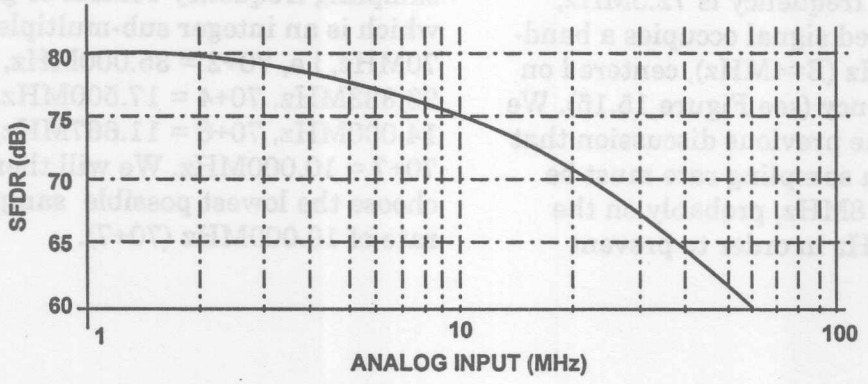


Figure 15.16

There is an advantage in choosing a sampling frequency which is an *odd* sub-multiple of the lower band-edge in that there is no frequency inversion in the baseband alias as would be the case for a sampling frequency equal to an *even* sub-multiple of the lower band-edge. (Frequency inversion can be easily dealt with in the DSP software should it occur, so the issue is not very important.)

The next step is to select an ADC which has sufficient dynamic range with a 70 to 75MHz input to meet our system requirement. In most radar receivers, a SFDR of 60 to 80dB is desirable. Unfortunately, this requirement will not be met with standard Nyquist-sampling ADCs due to degradations which occur at high input frequencies. Figure 15.16 shows the SFDR of the AD9022 12 bit, 20MSPS ADC, which represents one of the best monolithic designs available. Note that at 1MHz the SFDR is 80dB, but at the IF frequency of 70MHz, the SFDR of the device is less than 60dB.

Meeting this performance requirement of 80dB SFDR requires the addition of an external wide-bandwidth, low distortion sample-and-hold, such as the AD9100 as shown in Figure 15.17. The external SHA serves to hold the signal constant during the ADC conversion cycle. The ADC sees a dc value during the hold-time of the external SHA. The process of optimizing the design for the best SFDR is not simple, and involves many tradeoffs.

THE ADDITION OF AN EXTERNAL WIDEBAND LOW DISTORTION SHA EXTENDS THE LOW FREQUENCY PERFORMANCE OF THE ADC TO HIGHER FREQUENCIES

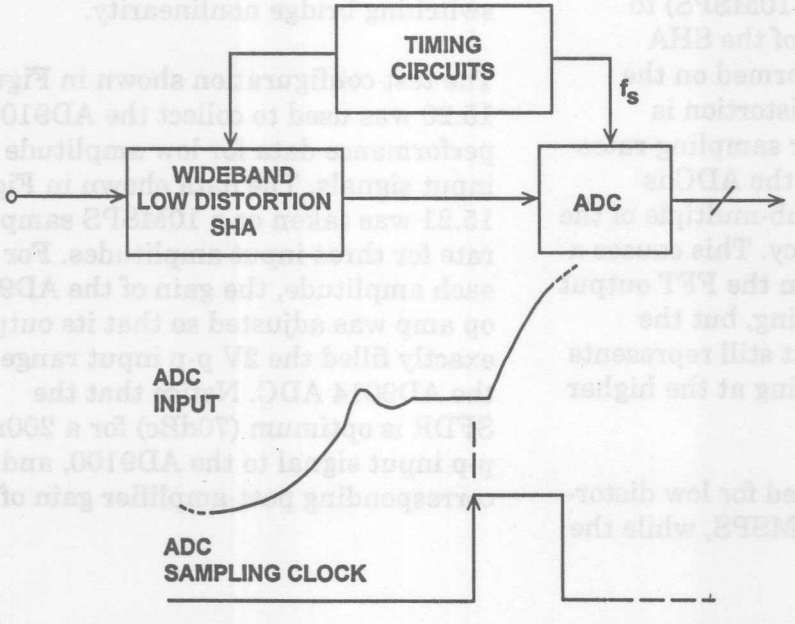


Figure 15.17

The first step in the process is to select an ADC which has sufficient SFDR at low frequencies. The low frequency distortion of an ADC is an indicator of the inherent non-linearity in the dc transfer function. The addition of an ideal external SHA will do nothing to improve on this basic performance. The best you can expect the SHA to do is to extend the low frequency performance of the ADC to higher frequencies. Because of its excellent low frequency distortion (–80dBc @ 1MHz), the AD9022 is good choice.

The next step is to select a low distortion SHA which will maintain sufficient dynamic performance at the IF frequency. Most SHAs are specified for distortion when operating in the track mode. What is of real interest, however, is the signal distortion in the hold mode when the SHA is operating dynamically. The AD9100 and AD9101 are ultra-fast SHAs and are specified in terms of hold-mode distortion. The measurement is done using a high performance low distortion ADC (such as the AD9014 14-bit, 10MSPS) to digitize the held value of the SHA output. An FFT is performed on the ADC output, and the distortion is measured digitally. For sampling rates greater than 10MSPS, the ADC is clocked at an integer sub-multiple of the SHA sampling frequency. This causes a frequency translation in the FFT output because of undersampling, but the distortion measurement still represents that of the SHA operating at the higher sampling rate.

The AD9100 is optimized for low distortion operation up to 30MSPS, while the AD9101 will provide low distortion performance up to a sampling rate of 125MSPS.
A block diagram of the AD9100 track-and-hold is shown in Figure 15.18. The switching bridge is integrated into the first stage closed-loop input amplifier. This innovation provides error (distortion) correction for both the switch and amplifier, while still achieving slewrates representative of a more traditional open-loop design. The device has a 250MHz input bandwidth and a 16ns acquisition time to 0.01%. Hold-mode distortion performance versus analog input frequency for a sampling rate of 30MSPS and a 2V p-p output is shown in Figure 15.19.

The hold-mode distortion shown in Figure 15.19 is clearly not good enough for the 70MHz IF application we are considering. However, the distortion performance of the AD9100 can be greatly improved by reducing the input signal level. This will decrease the signal-to-noise ratio, but will also reduce the distortion produced by the switching bridge nonlinearity.

The test configuration shown in Figure 15.20 was used to collect the AD9100 performance data for low amplitude input signals. The data shown in Figure 15.21 was taken at a 10MSPS sampling rate for three input amplitudes. For each amplitude, the gain of the AD9618 op amp was adjusted so that its output exactly filled the 2V p-p input range of the AD9014 ADC. Notice that the SFDR is optimum (70dBc) for a 200mV p-p input signal to the AD9100, and a corresponding post-amplifier gain of 10.

AD9100 MONOLITHIC 30MSPS TRACK-AND-HOLD

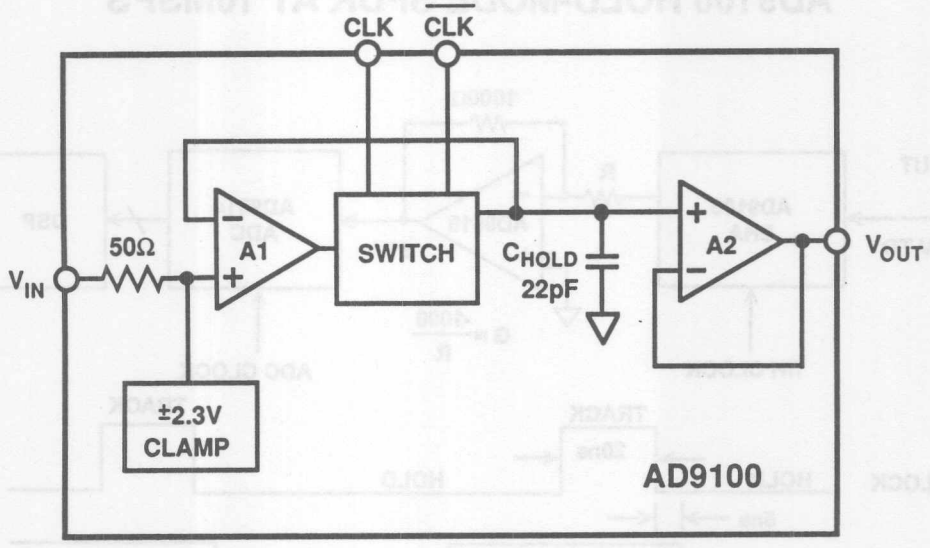


Figure 15.18

AD9100 HOLD-MODE SFDR VERSUS INPUT FREQUENCY FOR 30MSPS SAMPLING RATE, 2V P-P OUTPUT

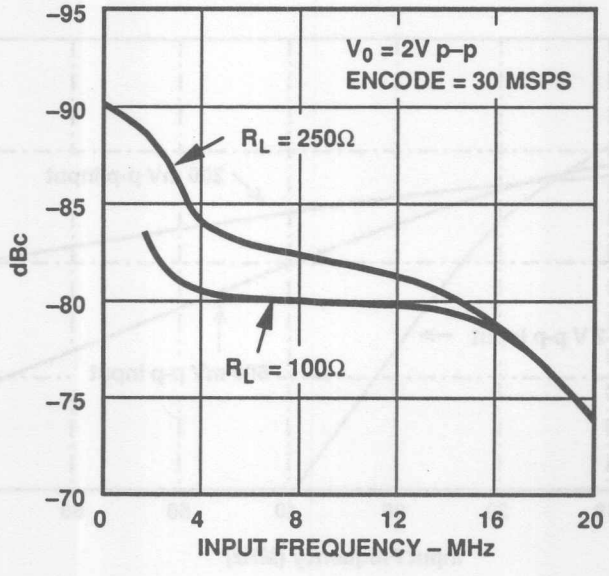


Figure 15.19

TEST CONFIGURATION AND TIMING FOR MEASURING AD9100 HOLD-MODE SFDR AT 10MSPS

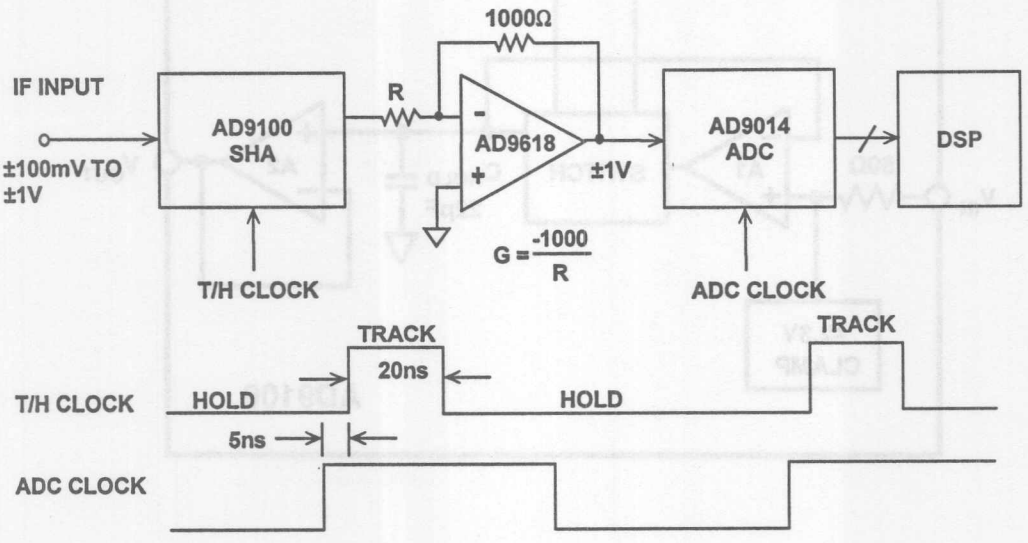


Figure 15.20

AD9100 HOLD-MODE SFDR MEASURED WITH AD9014 ADC SAMPLING AT 10MSPS

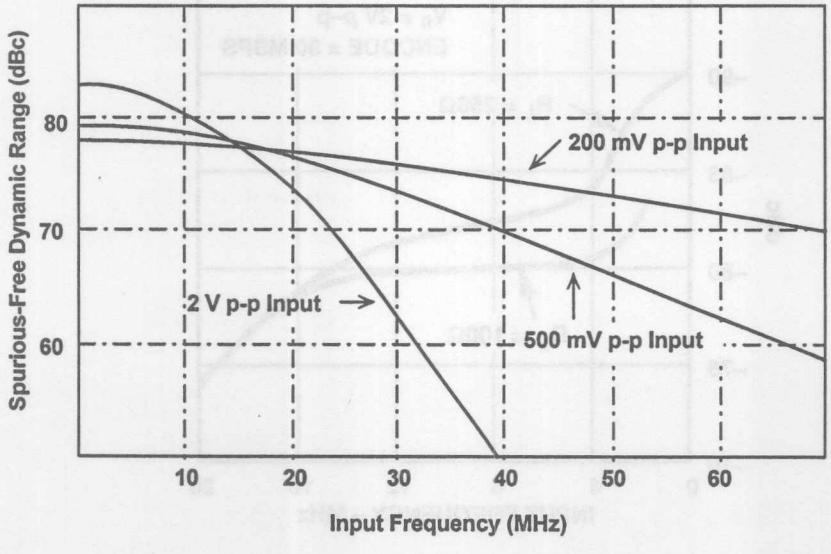


Figure 15.21

The performance of the AD9100 driving the AD9022 under identical conditions yielded the FFT spectrum shown in Figure 15.22. The 72MHz SFDR is greater than 70dBc, and the measured SNR is 62dB.

The tradeoff in optimizing the circuit for the best SFDR is the increase in overall noise resulting from the high-gain post-amplifier amplifying the hold-mode noise of the AD9100.

The other part of a successful wide-dynamic range design involves the optimization of the timing between the SHA and the ADC. This involves even more tradeoffs. The SHA acquisition time should be long enough to achieve the desired accuracy, but short enough to allow sufficient hold-time for the ADC front-end to settle and yield a low-distortion conversion. For the example above, the optimum performance was achieved using an acquisition time of 20ns and a track time of 80ns. As shown in Figure 15.20, the ADC is clocked close to the end of the SHA's hold time. Best performance in designs such as these is always achieved by optimizing the timing in the actual circuit.

Similar dynamic range improvements can be achieved with high speed flash converters at higher sampling rates using the AD9101 SHA whose block diagram is shown in Figure 15.23. The AD9101 is a track-and-hold with an internal post-amplifier. This configuration allows the front end sampler to operate at relatively low signal amplitudes, resulting in dramatic improvement in hold-mode distortion at high input frequencies and sampling rates up to 125MSPS. The AD9101 has an input bandwidth of 350MHz and an acquisition time of 7ns to 0.1% and 11ns to 0.01%.

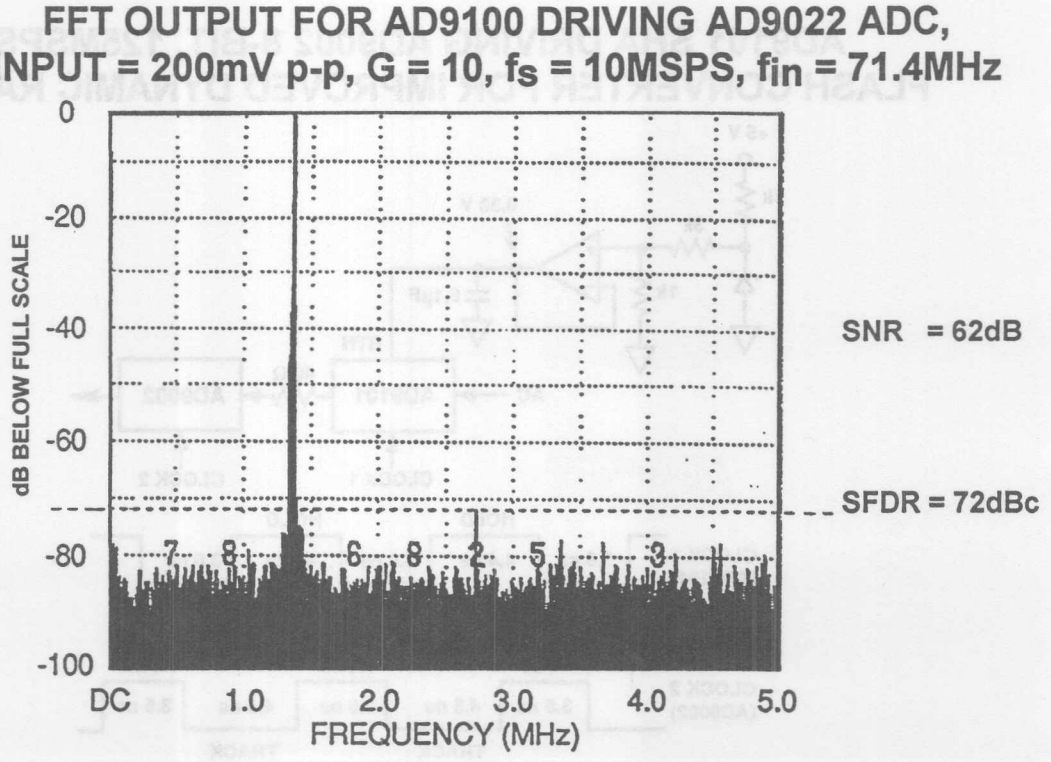


Figure 15.22

AD9101 125MSPS SAMPLING AMPLIFIER

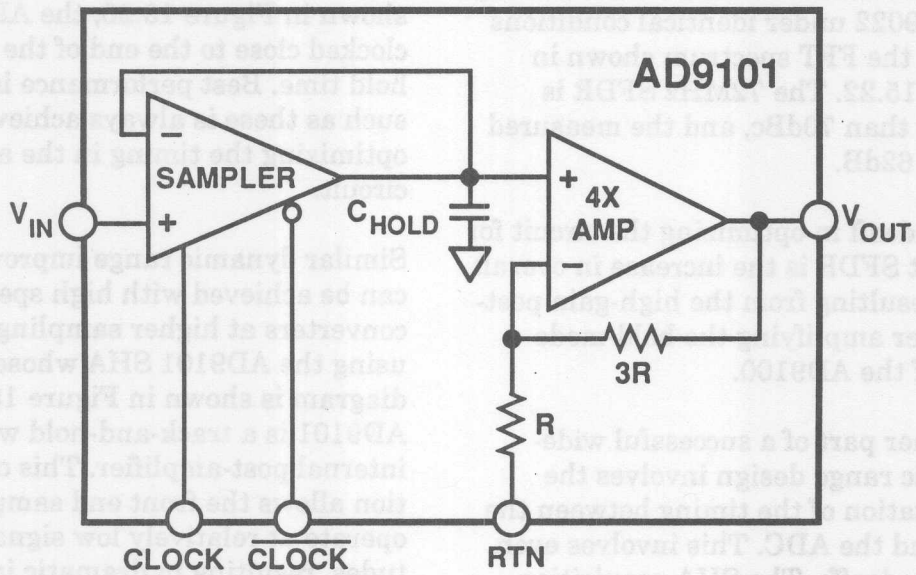


Figure 15.23

A block diagram and a timing diagram is shown for the AD9101 driving the AD9002 8 bit flash converter at 125MSPS (see Figure 15.24). The corresponding dynamic range with and without the AD9101 is shown in Figure 15.25.

AD9101 SHA DRIVING AD9002 8-BIT, 125MSPS FLASH CONVERTER FOR IMPROVED DYNAMIC RANGE

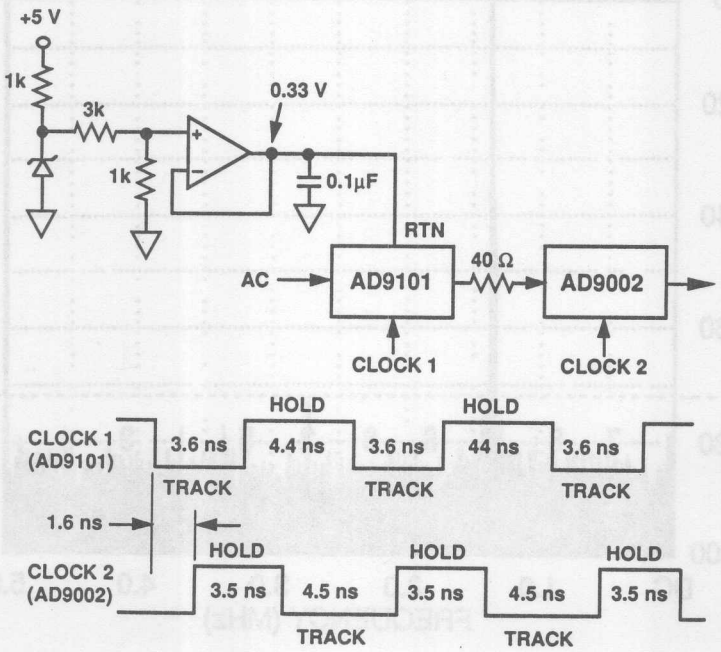


Figure 15.24

AD9002 DYNAMIC PERFORMANCE WITH AND WITHOUT AD9101

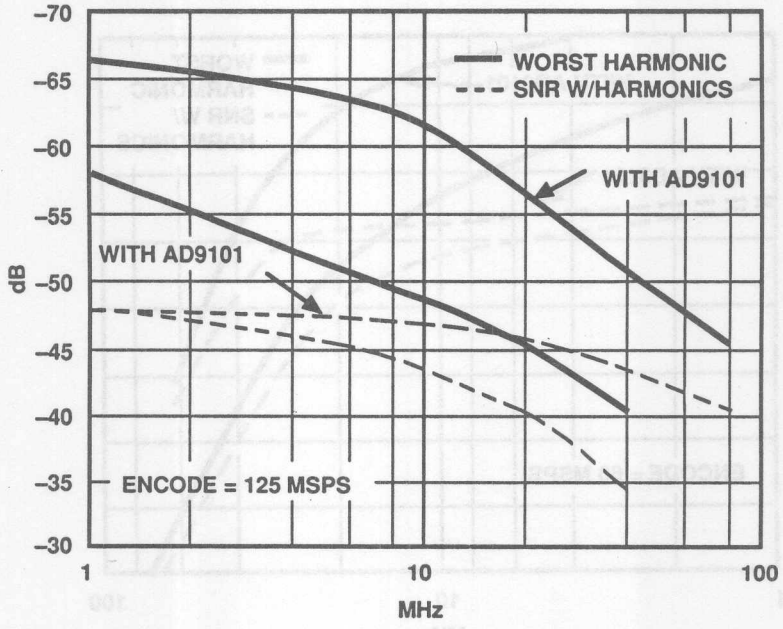


Figure 15.25

The increase in performance is also dramatic for the AD9060 10 bit flash converter. The block diagram and timing is shown in Figure 15.26, and the corresponding performance comparison in Figure 15.27.

AD9101 SHA DRIVING AD9060 10-BIT FLASH CONVERTER AT 60MSPS

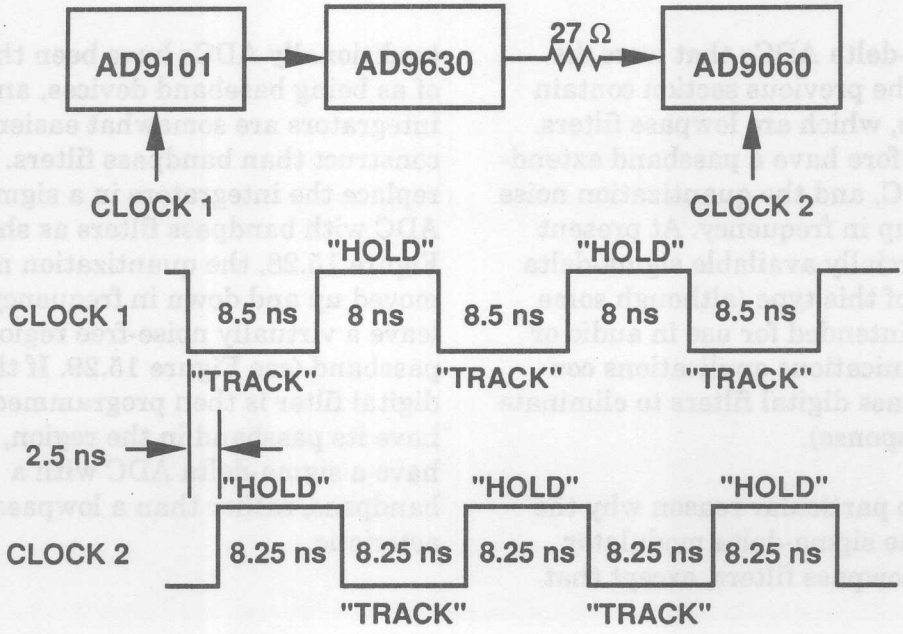


Figure 15.26

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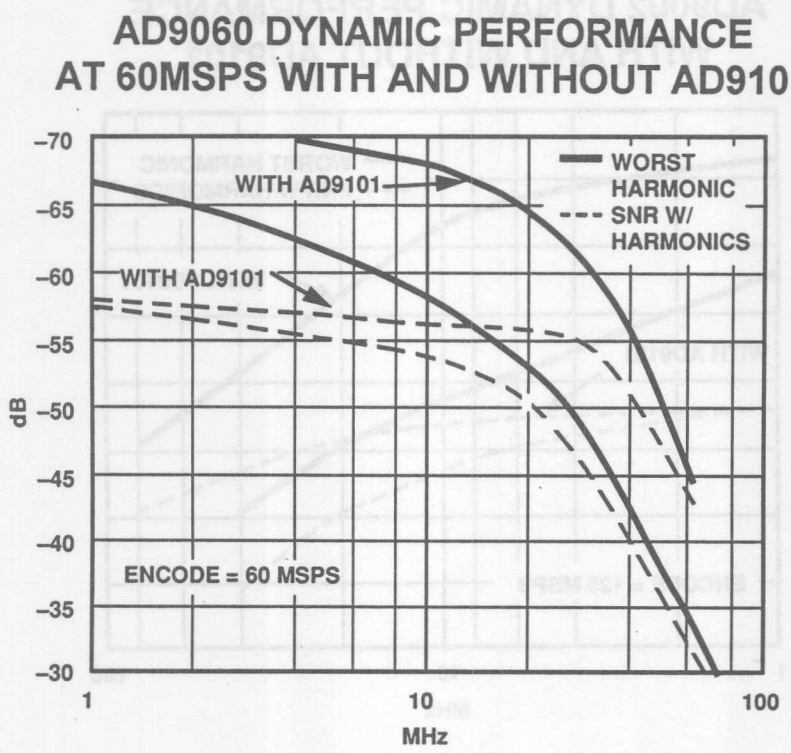


Figure 15.27

BANDPASS SIGMA-DELTA TECHNIQUES FOR DIRECT IF-TO-DIGITAL CONVERSION

James Bryant

The sigma-delta ADCs that were discussed in the previous section contain integrators, which are lowpass filters. They therefore have a passband extending from DC, and the quantization noise is pushed up in frequency. At present all commercially available sigma-delta ADCs are of this type (although some which are intended for use in audio or telecommunications applications contain bandpass digital filters to eliminate any DC response).

There is no particular reason why the filters of the sigma-delta modulator should be lowpass filters, except that traditionally ADCs have been thought of as being baseband devices, and that integrators are somewhat easier to construct than bandpass filters. If we replace the integrators in a sigma-delta ADC with bandpass filters as shown in Figure 15.28, the quantization noise is moved up and down in frequency to leave a virtually noise-free region in the passband (see Figure 15.29. If the digital filter is then programmed to have its passband in the region, we have a sigma-delta ADC with a bandpass, rather than a lowpass characteristic.

REPLACING INTEGRATORS WITH RESONATORS GIVES A BANDPASS SIGMA-DELTA ADC

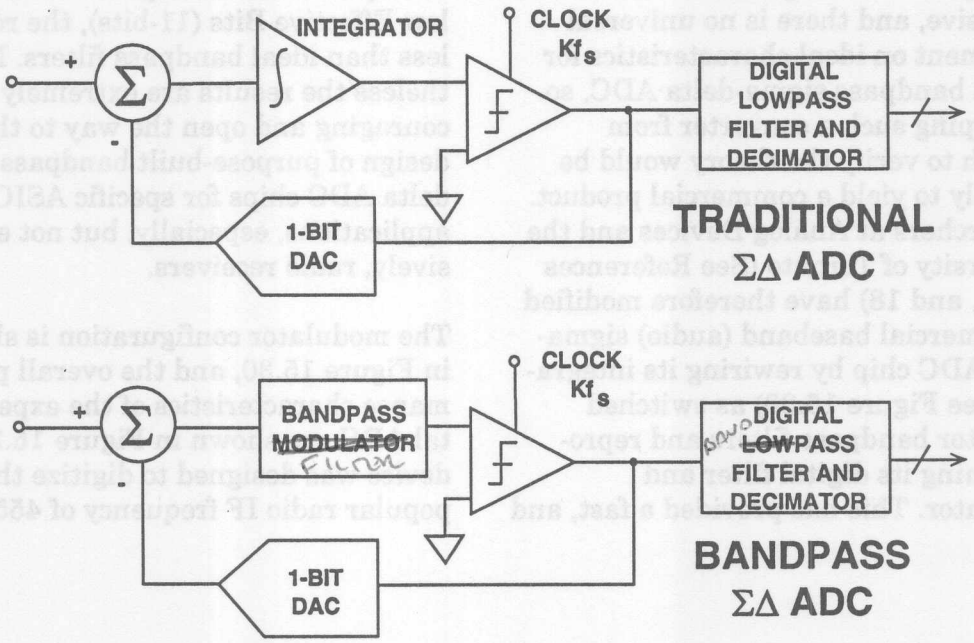


Figure 15.28

NOISE SHAPING FUNCTIONS FOR TRADITIONAL AND BANDPASS SIGMA-DELTA ADCs

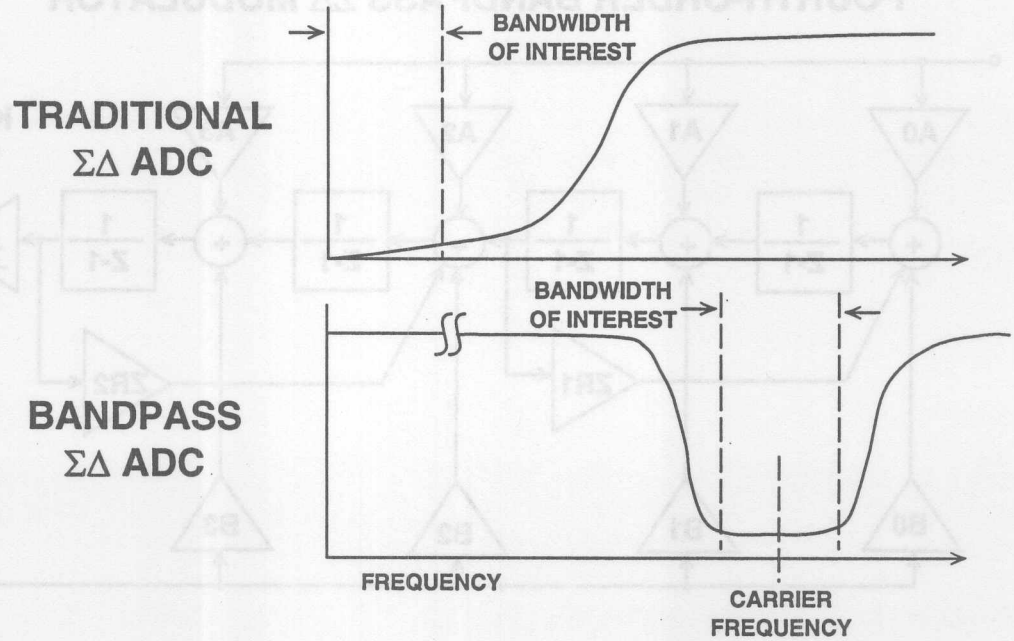


Figure 15.29

The theory is straightforward, but the development of a sigma-delta ADC is expensive, and there is no universal agreement on ideal characteristics for such a bandpass sigma-delta ADC, so developing such a converter from scratch to verify the theory would be unlikely to yield a commercial product. Researchers at Analog Devices and the University of Toronto (See References 16, 17, and 18) have therefore modified a commercial baseband (audio) sigma-delta ADC chip by rewiring its integrators (see Figure 15.30) as switched capacitor bandpass filters and reprogramming its digital filter and decimator. This has provided a fast, and comparatively inexpensive, proof of the concept, but at the expense of relative low Effective Bits (11-bits), the result of less than ideal bandpass filters. Nevertheless the results are extremely encouraging and open the way to the design of purpose-built bandpass sigma-delta ADC chips for specific ASIC applications, especially, but not exclusively, radio receivers.

The modulator configuration is shown in Figure 15.30, and the overall performance characteristics of the experimental ADC are shown in Figure 15.31. The device was designed to digitize the popular radio IF frequency of 455kHz.

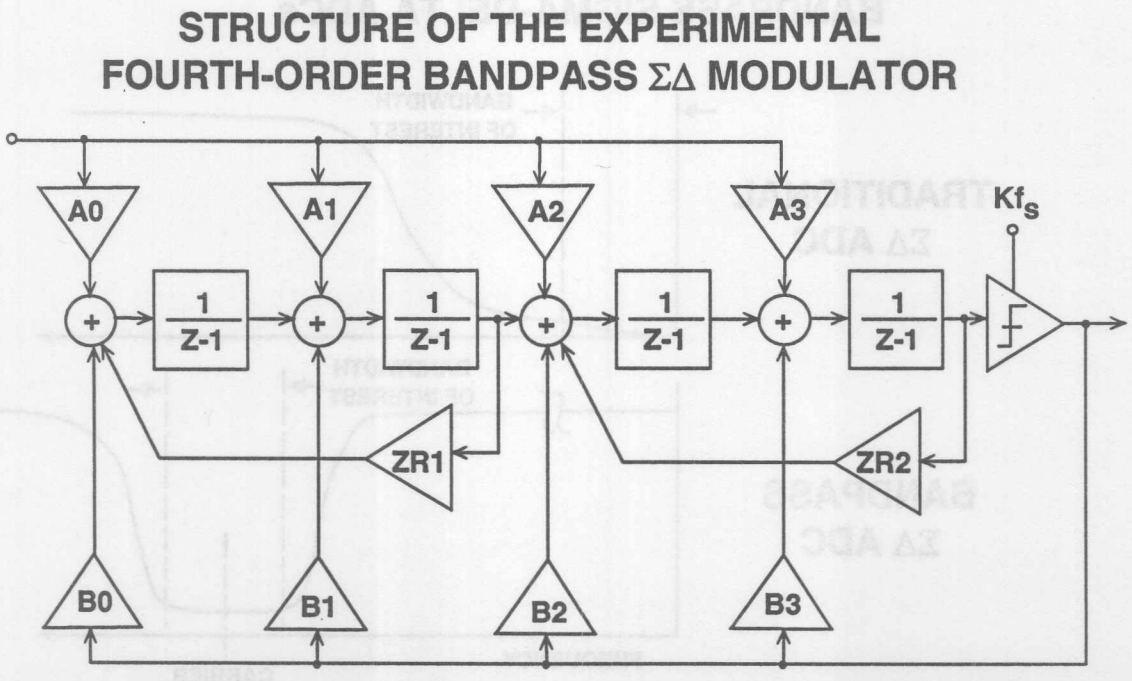


Figure 15.30

SUMMARY OF RESULTS FOR EXPERIMENTAL BANDPASS SIGMA-DELTA ADC

- **Center Frequency:** 455kHz
- **Bandwidth:** 10kHz
- **Sampling Rate:** 1.852MSPS
- **Oversampling Ratio:** 91
- **SNR in Specified Band:** 65dB
- **Supply: ±5V,** **Power: 750mW**
- **Process: 3µm CMOS,** **Active Area: 1.8 x 3.4mm**

Figure 15.31

In the future it may be possible to have such bandpass sigma-delta ADCs with user-programmable digital filter coefficients, so that the passband of a receiver could be modified during operation in response to the characteristics of the signal (and the interference!) being received. Such a function is very attractive, but difficult to implement, since it would involve loading, and storing, several hundreds or even thousands of 16-22 bit filter coefficients, and would considerably increase the size, and cost, of the converter.

A feature which could be added comparatively easily to a sigma-delta ADC is a more complex digital filter with separate reference (I) and quadrature (Q) outputs. Such a feature would be most valuable in many types of radio receivers.

ACHIEVING WIDE DYNAMIC RANGE USING VARIABLE GAIN AMPLIFIERS

Walt Kester, Barrie Gilbert, Bob Clarke

Another method to extend the dynamic range in a system is to precede the ADC with a wide bandwidth, variable gain amplifier (VGA). There are many ways to make VGAs, and some relatively good ones can be built using analog multipliers such as the AD834, 500MHz 4-quadrant multiplier shown in Figure 15.32. A diagram of a 90MHz voltage controlled amplifier (VCA) is shown in Figure 15.33, and the corresponding frequency response in Figure 15.34. The signal is applied to the Y input of the AD834, and the control voltage to the X input. The AD811 transimpedance amplifier level-shifts the differential outputs of the AD834 to a single-ended signal and acts as a current-to-voltage converter.

SIMPLIFIED BLOCK DIAGRAM OF THE AD834 500MHz 4-QUADRANT ANALOG MULTIPLIER

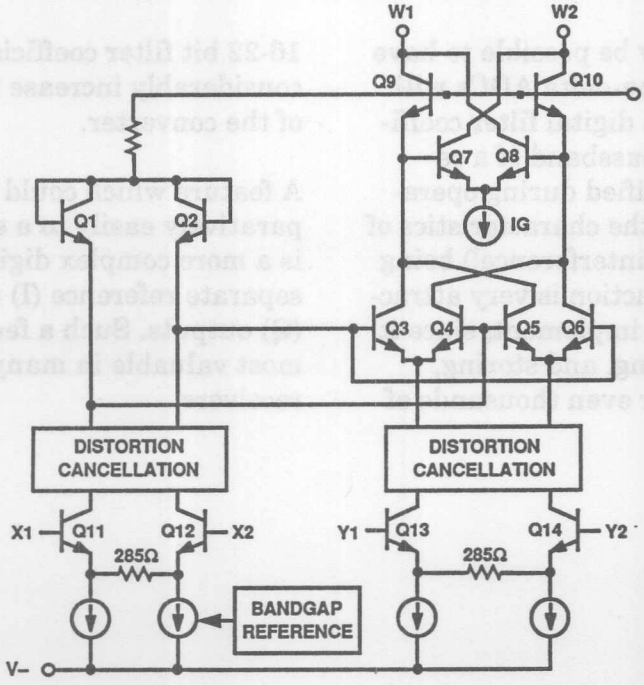


Figure 15.32

A 90MHz VCA USING THE AD834 AND THE AD811

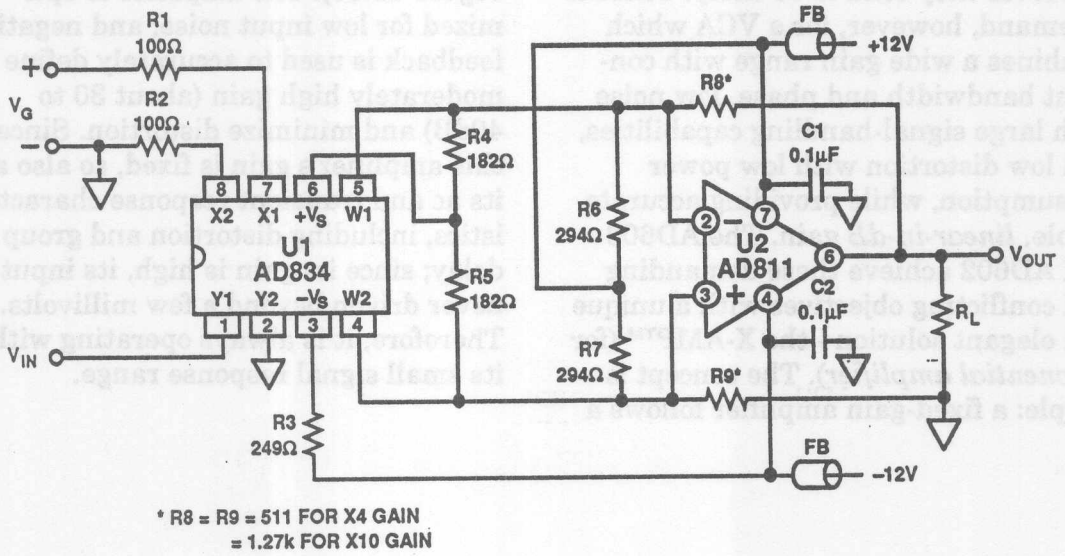


Figure 15.33

FREQUENCY RESPONSE OF THE 90MHz VCA

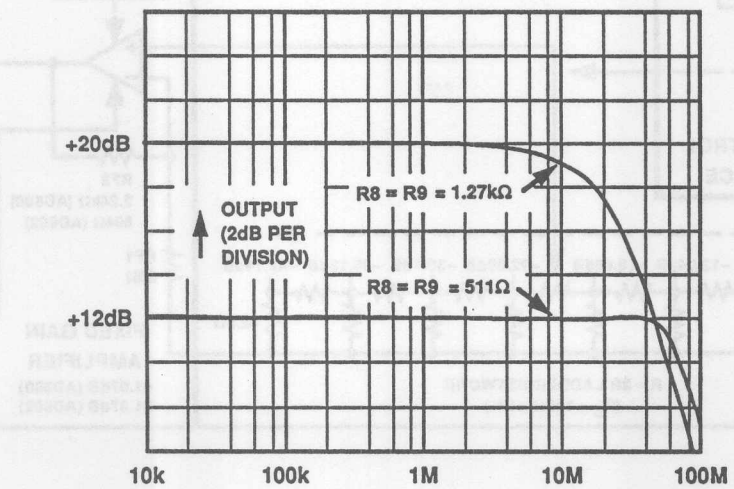


Figure 15.34

Most VCAs made with analog multipliers have gain which is *linear in volts* with respect to the control voltage, moreover they tend to be noisy. There is a demand, however, for a VCA which combines a wide gain range with constant bandwidth and phase, low noise with large signal-handling capabilities, and low distortion with low power consumption, while providing accurate, stable, *linear-in-dB* gain. The AD600 and AD602 achieve these demanding and conflicting objectives with a unique and elegant solution - the X-AMP™ (for *exponential amplifier*). The concept is simple: a fixed-gain amplifier follows a passive, broadband attenuator equipped with special means to alter its attenuation under the control of a voltage (see Figure 15.35). The amplifier is optimized for low input noise, and negative feedback is used to accurately define its moderately high gain (about 30 to 40dB) and minimize distortion. Since this amplifier's gain is fixed, so also are its ac and transient response characteristics, including distortion and group delay; since its gain is high, its input is never driven beyond a few millivolts. Therefore, it is always operating within its small signal response range.

SINGLE CHANNEL OF THE DUAL 30MHz AD600/AD602 X-AMP

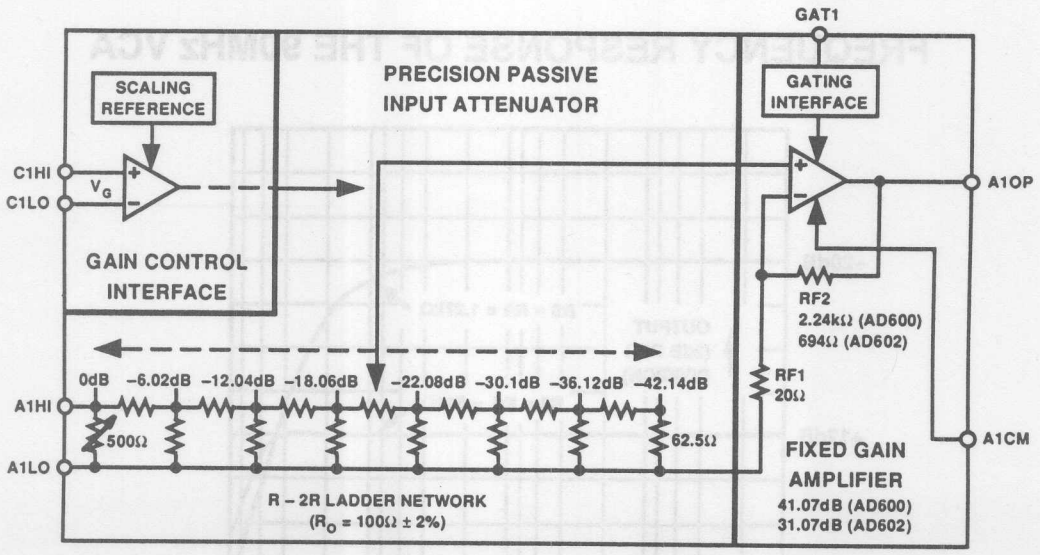


Figure 15.35

The attenuator is a 7-section (8-tap) R-2R ladder network. The voltage ratio between all adjacent taps is exactly 2, or 6.02dB. This provides the basis for the precise linear-in-dB behavior. The overall attenuation is 42.14dB. As will be shown, the amplifier's input can be connected to any one of these taps, or even *interpolated* between them, with only a small deviation error of about ±0.2dB. The overall gain can be varied all the way from the fixed (maximum) gain to a value 42.14dB less. For example, in the AD600, the fixed gain is 41.07dB (a voltage gain of 113); using this choice, the full gain range is −1.07dB to +41.07dB. The gain is related to the control voltage by the relationship $G_{dB} = 32V_G + 20$ where V_G is in volts. For the AD602, the fixed gain is 31.07dB (a voltage gain of 35.8), and the gain is given by $G_{dB} = 32V_G + 10$.

The gain at $V_G = 0$ is laser trimmed to an absolute accuracy of ±0.2dB. The gain scaling is determined by an on-chip bandgap reference (shared by both channels), laser trimmed for high accuracy and low temperature coefficient. Figure 15.36 shows the gain versus the differential control voltage for both the AD600 and the AD602.

GAIN OF THE AD600/AD602 AS A FUNCTION OF CONTROL VOLTAGE

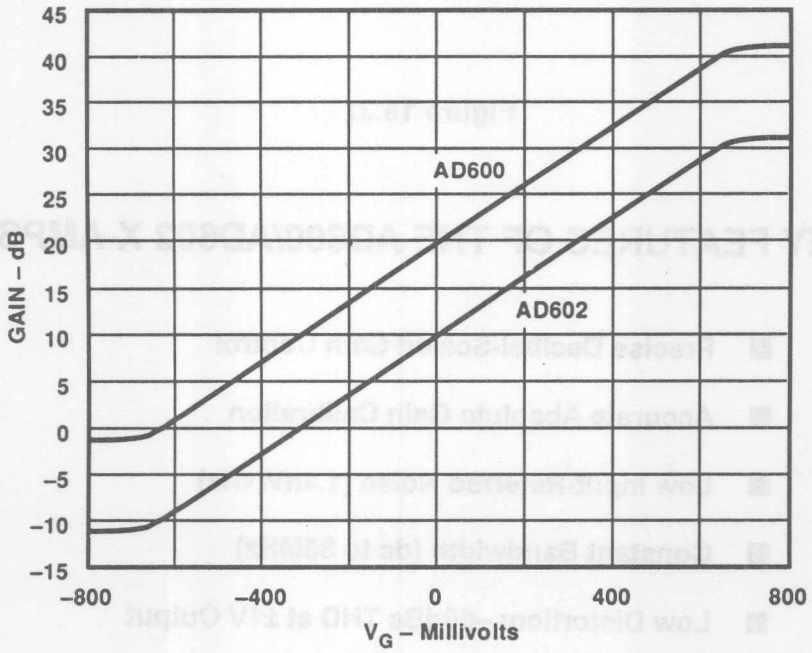


Figure 15.36

In order to understand the operation of the AD600/AD602, consider the simplified diagram shown in Figure 15.37. Notice that each of the eight taps is connected to an input of one of eight bipolar differential pairs, used as current-controlled transconductance (g_m) stages; the other input of all these gm stages is connected to the amplifier's gain-determining feedback network, R_{F1}/R_{F2}. When the emitter bias current, I_E, is directed to one of the 8 transistor pairs (by means not shown here), it becomes the input stage for the complete amplifier.

15

CONTINUOUS INTERPOLATION BETWEEN TAPS IN THE X-AMP IS PERFORMED WITH CURRENT-CONTROLLED gm STAGES

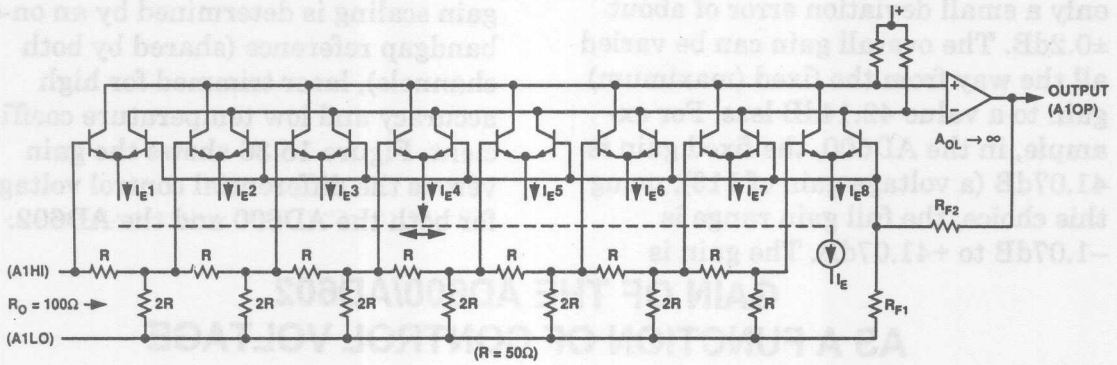


Figure 15.37

KEY FEATURES OF THE AD600/AD602 X-AMPS

- Precise Decibel-Scaled Gain Control
- Accurate Absolute Gain Calibration
- Low Input-Referred Noise (1.4nV/√Hz)
- Constant Bandwidth (dc to 35MHz)
- Low Distortion: –60dBc THD at ±1V Output
- Stable Group Delay (±2ns Over Gain Range)
- Response Time: Less than 1µs for 40dB Gain Change
- Low Power (125mW per channel maximum)
- Differential Control Inputs

Figure 15.38

When I_E is connected to the pair on the left-hand side, the signal input is connected directly to the amplifier, giving the maximum gain. The distortion is very low, even at high frequencies, due to the careful open-loop design, aided by the negative feedback. If I_E were now to be abruptly switched to the second pair, the overall gain would drop by exactly 6.02dB, and the distortion would remain low, because only one g_m stage remains active.

In reality, the bias current is *gradually* transferred from the first pair to the second. When I_E is equally divided between two gm stages, both are active, and the situation arises where we have an op amp with two input stages fighting for control of the loop, one getting the full signal, and the other getting a signal exactly half as large.

Analysis shows that the effective gain is reduced, not by 3dB, as one might first expect, but rather by 20log1.5, or 3.52dB. This error, when divided equally over the whole range, would amount to a gain ripple of ±0.25dB; however, the interpolation circuit actually generates a Gaussian distribution of bias currents, and a significant fraction of I_E always flows in adjacent stages. This smoothes the gain function and actually lowers the ripple (see Reference 19). As I_E moves further to the right, the overall gain progressively drops.

The total input-referred noise of the X-AMP™ is 1.4nV/√Hz; only slightly more than the thermal noise of a 100Ω resistor which is 1.29nV/√Hz at 25°C. The input-referred noise is constant regardless of the attenuator setting, therefore the output noise is always constant and independent of gain. For the AD600, the amplifier gain is 113 and the output noise spectral density is therefore 1.4nV/√Hz×113 or 158nV/√Hz. Referred to its maximum output of 2V rms, the signal-to-noise ratio would be 82dB in a 1MHz bandwidth. The corresponding signal-to-noise ratio of the AD602 is 10dB greater, or 92dB.

WIDE DYNAMIC RANGE ULTRASOUND SYSTEMS

Walt Kester

A block diagram of a typical ultrasound system is shown in Figure 15.39. A burst of ultrasound energy (1 to 13MHz) is generated in a piezoelectric transducer which physically contacts the outer body surface. The velocity of propagation of the ultrasound waves in most soft-body tissues (air and bones are the exception) is about 1500m/sec. Echoes are produced at interfaces between various types of soft-body structures. The round-trip time of each echo is used to determine its distance from the transducer.

B-SCAN ULTRASOUND SYSTEM BLOCK DIAGRAM

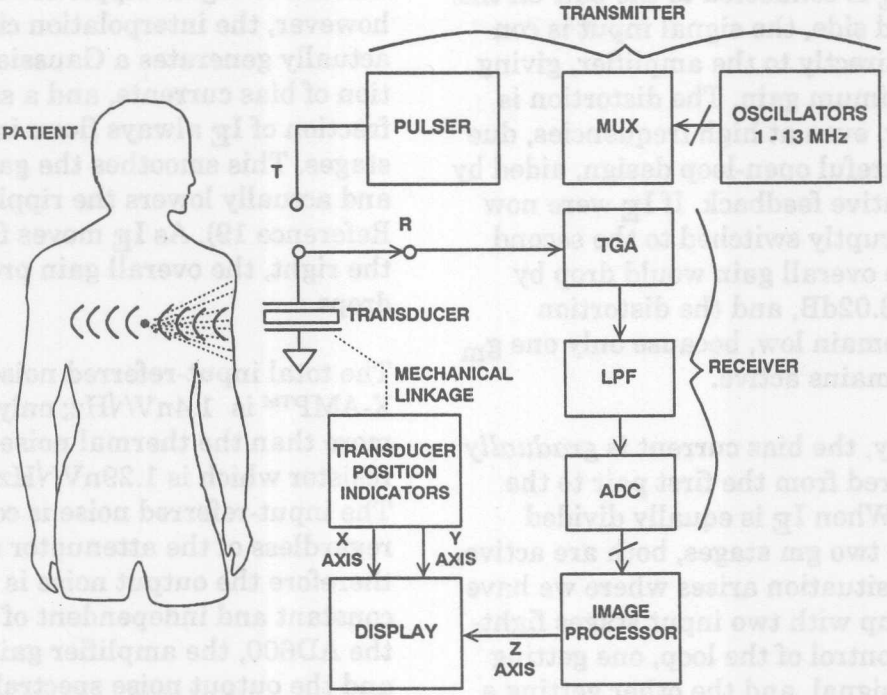


Figure 15.39

Soft-body tissues attenuate the burst of ultrasound energy by approximately 1dB/cm/MHz. For the thicker parts of the body, as in abdominal imaging, frequencies of 1 to 2MHz are common. For imaging of shorter path lengths, as in studies of the eye or other superficial structures, frequencies as high as 20MHz can be used. Because of soft-body tissue attenuation, the receiving transducer will see a dynamic range of 100dB when scanning from 1 to 10cm at 10MHz, independent of the tissue variations that need to be observed. Add the 50dB dynamic range typical for variations in tissue, and the transducer must have close to 150dB dynamic range. For this reason, the transducer output is usually applied to a Time Gain Amplifier (TGA) whose gain in dB is directly proportional to the amount of time elapsed from the transmission of the burst (see Figure 15.40). The AD600 X-AMP™ previously discussed is exactly such a device.

TIME GAIN AMPLIFIER

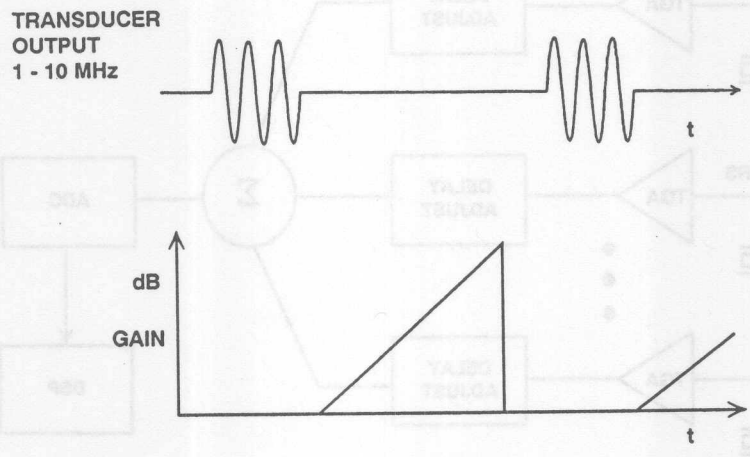


Figure 15.40

For reflections that are near the surface, there will be little attenuation. For deep signal returns, gain is applied to compensate for the path attenuation. The TGA thus compensates for normal signal attenuation associated with delay/distance. The receiver (ADC) therefore only sees the intensity variations associated with the different tissue types. In scans where the propagation path is primarily soft tissue structures of comparable attenuation, such as the abdomen, a fixed gain versus time function is usually adequate. In other cases involving blood pools or fixed regions, it is often desirable to vary the gain versus time function. Many commercial systems make this option available. In some cases it is even desirable for the operator to calibrate the TGA on a per-patient basis in order to achieve the best diagnostic image.

In phased array ultrasound systems, the angular information is precisely determined by phasing the delays from a number of transducers (transmitted and received) to electronically select the angle to be processed. The first generation of phased array elements used analog beam forming techniques as shown in Figure 15.41. Delays at the transmitter and receiver are adjusted using variable delay filters. The next generation of phased arrays will be digital. Low cost, low power, high performance ADCs and DSPs make it practical to digitize the rf directly and digitally control the delay requirements as shown in Figure 15.42. This technique is often referred to as digital beamforming and is also used in some modern radar and sonar systems.

ANALOG BEAMFORMING

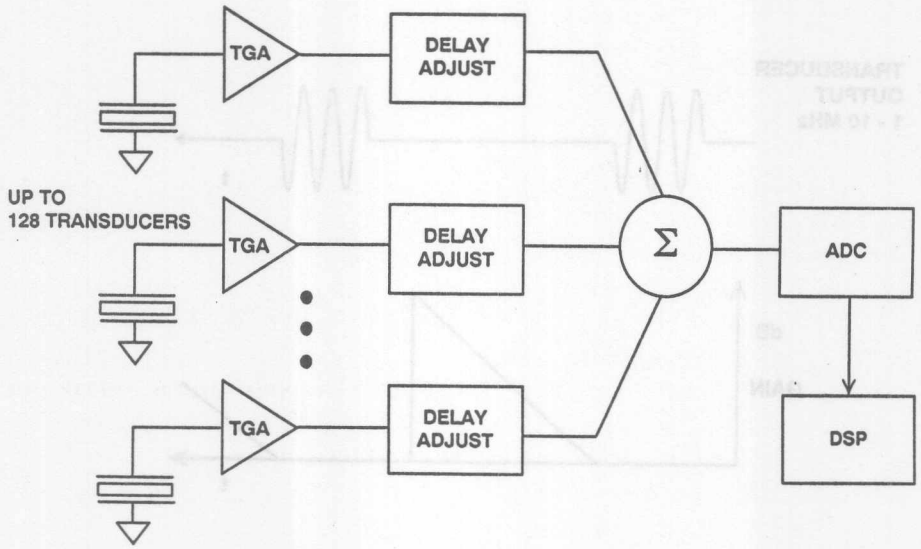


Figure 15.41

DIGITAL BEAMFORMING

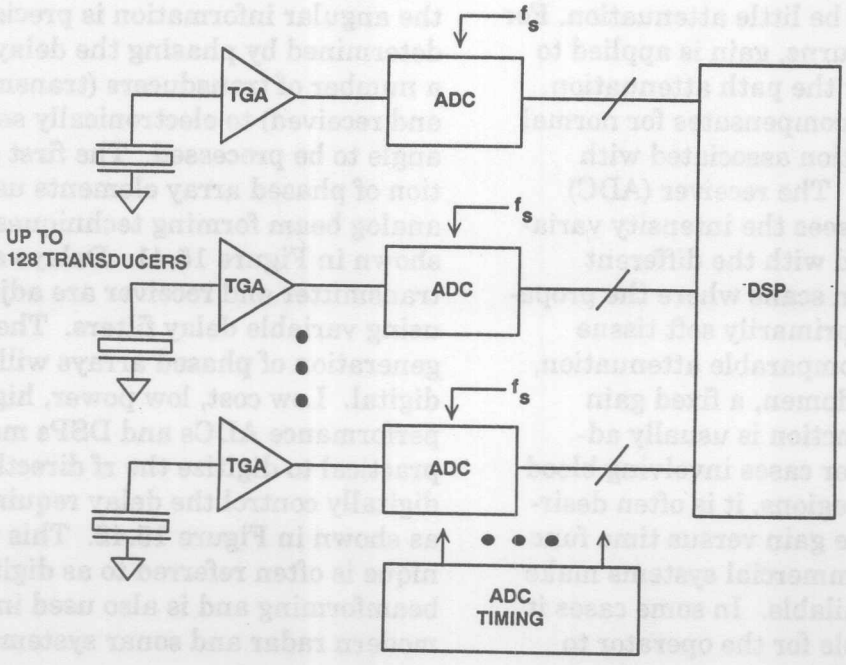


Figure 15.42

Figure 15.43 shows the complete signal path for a single channel of a phased array ultrasound system. The peak signal from the transducer is about 1V p-p into a 100Ω load. The signal then passes through a gain-of-two low noise pre-amplifier which drives the 100Ω input of the AD600. The appropriate gain function is generated by cascading each half of the AD600 and controlling the gain with the calibrated ramp voltage. The gain of the two stages can be changed from 0dB to 80dB. The interstage bandpass filter blocks the dc offset from the first gain stage and limits the out-of-band noise. The output of the second gain stage drives another bandpass filter and the AD9040 ADC input. The AD9040 output goes to the memory and the DSP circuits for further processing. This system is capable of maintaining a SFDR of greater than 55dB at ultrasound frequencies up to 15MHz.

Extreme care in layout, decoupling, grounding, and signal routing is essential in order to prevent oscillation in these circuits. A gain of 80dB (10,000) at a bandwidth of 1MHz corresponds to an effective *gain-bandwidth* product of 10GHZ!

Figure 15.44 shows the calculations to determine the proper gain function for the TGA assuming a 5MHz burst into soft body tissue. The corresponding control voltage ramp for the AD600 is shown in Figure 15.45.

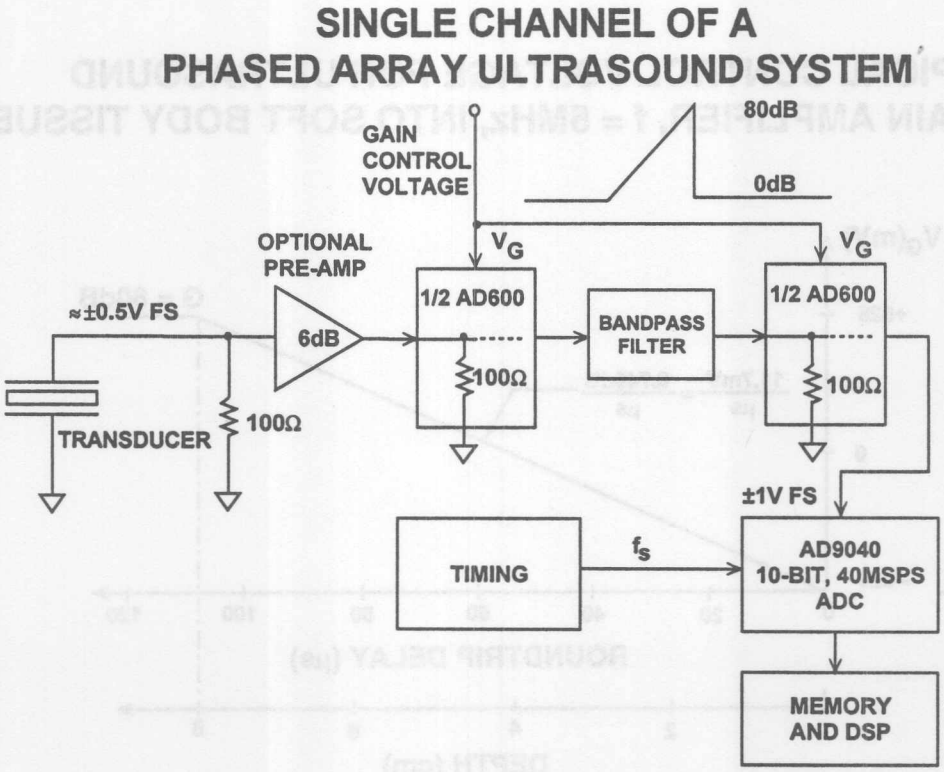


Figure 15.43

CALCULATION OF TGA COMPENSATION RAMP SLOPE FOR 5MHz ULTRASOUND BURST INTO SOFT BODY TISSUE

- Acoustic Velocity = 1500m/s (Soft Body Tissue)
- Propagation Delay = 6.7µs/cm (One Way)
  = 13.4µs/cm (Round Trip)
- Attenuation = 1dB/cm/MHz (One Way)
  = 5dB/cm @ 5MHz (One Way)
  = 10dB/cm @ 5MHz (Round Trip)
- TGA Ramp Slope = (10dB/cm)÷(13.4µs/cm) = 0.746dB/µs

Figure 15.44

TYPICAL CONTROL VOLTAGE FOR ULTRASOUND TIME GAIN AMPLIFIER, f = 5MHz, INTO SOFT BODY TISSUE

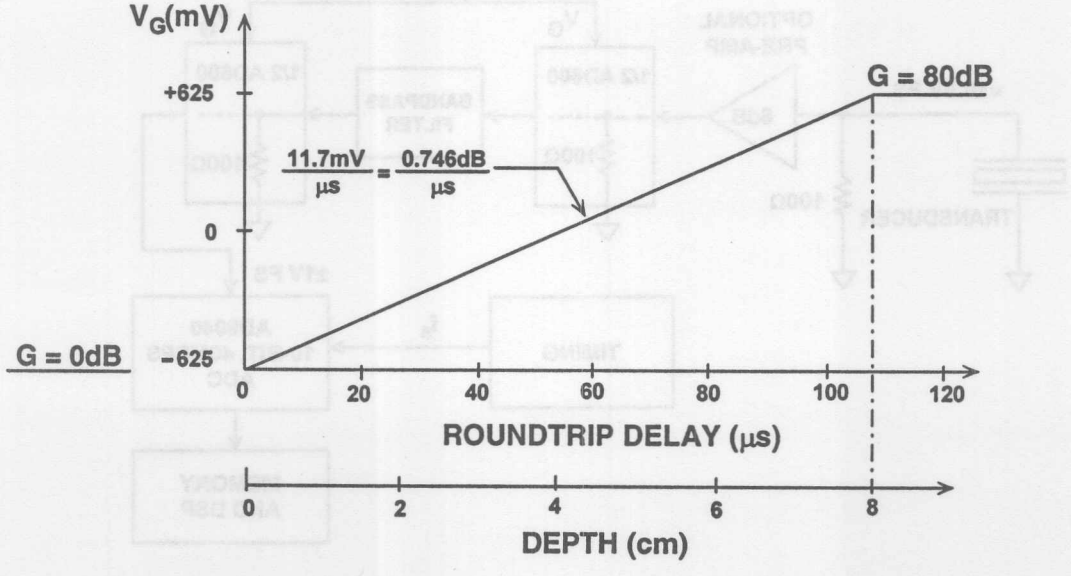


Figure 15.45

In some ultrasound applications, the user may wish to use a high input impedance preamplifier to avoid the signal attenuation that would result from loading the transducer by the 100Ω input resistance of the X-AMP. High gain cannot be tolerated, because the peak transducer signal is typically ±0.5V, while the peak input capability of the AD600/AD602 is only slightly more than ±1V. A gain of two is a suitable choice. In order to maintain the 1.4nV/√Hz noise performance of the AD600/AD602, the preamplifier's input noise should be less than 1.2nV/√Hz.

An inexpensive circuit, using complementary transistor types chosen for the low $r_{bb'}$, is shown in Figure 15.46. The gain is determined by the ratio of the net collector load resistance to the net emitter resistance, that is, it is an open-loop amplifier. The gain will be ×2 (6dB) only into a 100Ω load, assumed to be provided by the input to the X-AMP.; R2 and R7 are in shunt with this load, and their value is important in defining the gain. For small-signal inputs, both transistors contribute an equal transconductance, which is rendered less sensitive to signal level by the emitter resistors R4 and R5, which also play a dominant role in setting the gain.

This is a Class AB amplifier. As V_{IN} increases in a positive direction, Q1 conducts more heavily and its r_e becomes lower while that of Q2 increases. Conversely, more negative values of V_{IN} result in the r_e of Q2 decreasing, while that of Q1 increases. The design is chosen such that the net emitter resistance is essentially independent of the instantaneous value of V_{IN}, resulting in moderately low distortion. Low values of resistance and moderately high bias currents are important in achieving the low noise, wide bandwidth, and low distortion of this preamplifier. Heavy decoupling prevents noise on the power supply lines from being conveyed to the input of the X-AMP.

A LOW-NOISE ULTRASOUND PREAMPLIFIER FOR THE AD600 AND AD602

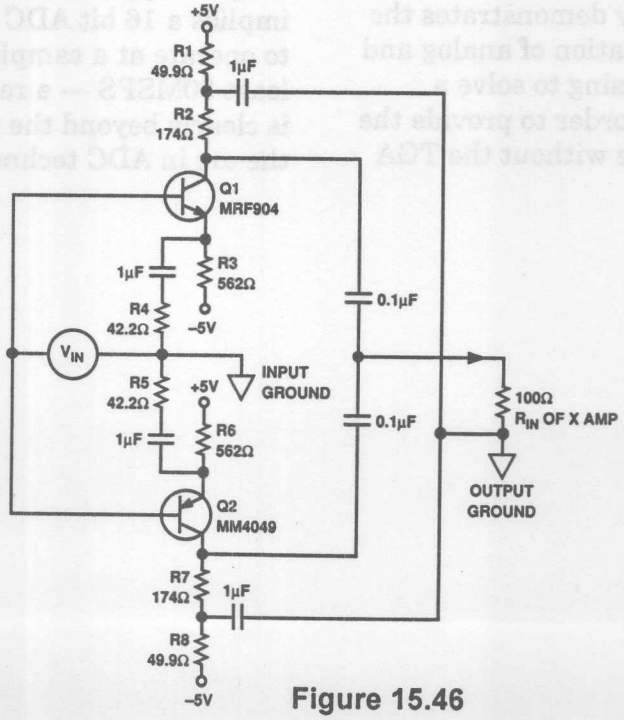


Figure 15.46

ULTRASOUND PREAMPLIFIER PERFORMANCE

Measurement	Value
Gain (f = 30MHz)	6dB
Bandwidth (–3dB)	250MHz
Input Signal for 1dB Compression	1V p-p
Second Harmonic Distortion, V_{IN} = 200mV p-p	–51dBc
Third Harmonic Distortion, V_{IN} = 200mV p-p	–57dBc
Second Harmonic Distortion, V_{IN} = 500mV p-p	–47dBc
Third Harmonic Distortion, V_{IN} = 500mV p-p	–45dBc
System Input NSD (Including X-AMP)	1.03nV/√Hz
Input Resistance	1.4kΩ
Input Capacitance	15pF
Input Bias Current	±150µA
Power Supply Voltage	±5V
Quiescent Current	15mA

Figure 15.47

For ultrasound frequencies below 1MHz, the AD797 op amp makes a good choice for the ultrasound pre-amplifier.

This example clearly demonstrates the power of the combination of analog and digital signal processing to solve a system problem. In order to provide the same dynamic range without the TGA (i.e. the ADC interfaces directly to the transducer via a fixed-gain preamp), the ADC would have to have a dynamic range of approximately 100dB. This implies a 16 bit ADC which would have to operate at a sampling frequency of at least 30MSPS — a requirement which is clearly beyond the present state of the art in ADC technology!

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SECTION 16

TECHNIQUES FOR VERIFYING HIGH SPEED ADC PERFORMANCE

- ANALOG TECHNIQUES FOR EVALUATION OF ADC STATIC TRANSFER FUNCTIONS
- ANALOG TECHNIQUES FOR EVALUATING ADC DYNAMIC TRANSFER FUNCTION
- BENCH TESTING HIGH SPEED ADCS USING DSP TECHNIQUES
- FFT TESTING
- TROUBLESHOOTING THE FFT OUTPUT

SECTION 16

TECHNIQUES FOR VERIFYING HIGH SPEED ADC PERFORMANCE

Walt Kester, Allen Hill

Successful users of high speed ADCs generally have performed at least a few fundamental bench tests before committing to a final system designs. While dc and ac ADC testing (especially on a production basis) is a complete subject in itself, a basic understanding of the principles will allow users to perform powerful bench testing without large investments in time or capital.

High performance converter manufacturers such as Analog Devices have anticipated this need and have designed evaluation boards for most recently released high performance ADCs, op amps, DACs, etc. A generic evaluation board for an ADC is shown in Figure 16.1. This board has all the peripheral support circuitry required to operate the ADC including input buffer amplifier, voltage reference (if required), timing circuits, output registers, etc. In order to make simple analog tests on the ADC, an on-board reconstruction DAC is often supplied. The output data from the external latch is brought out on a connector which allows interfacing to an external DSP test system. A photograph of the evaluation board for the AD9022 12bit, 20MSPS ADC is shown in Figure 16.2.

The board has been properly laid out using good grounding, decoupling, and signal routing techniques. Analog Devices will supply interested customers with actual artwork for the PC board layout. The user need only supply power, an input signal, and a sampling clock to make the ADC operational.

A TYPICAL ADC EVALUATION BOARD

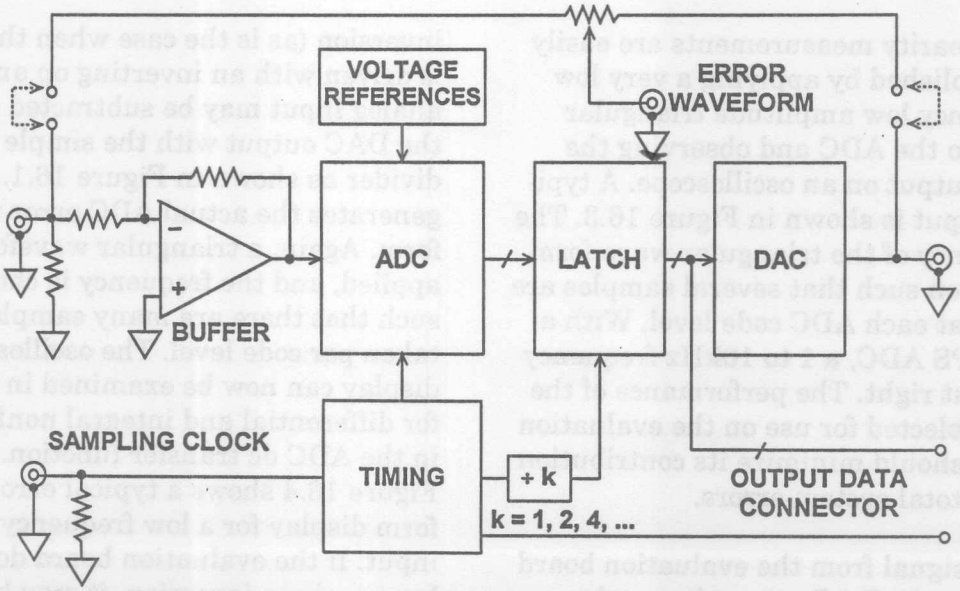


Figure 16.1

PHOTOGRAPH OF EVALUATION BOARD FOR THE AD9022 12-BIT, 20MSPS ADC

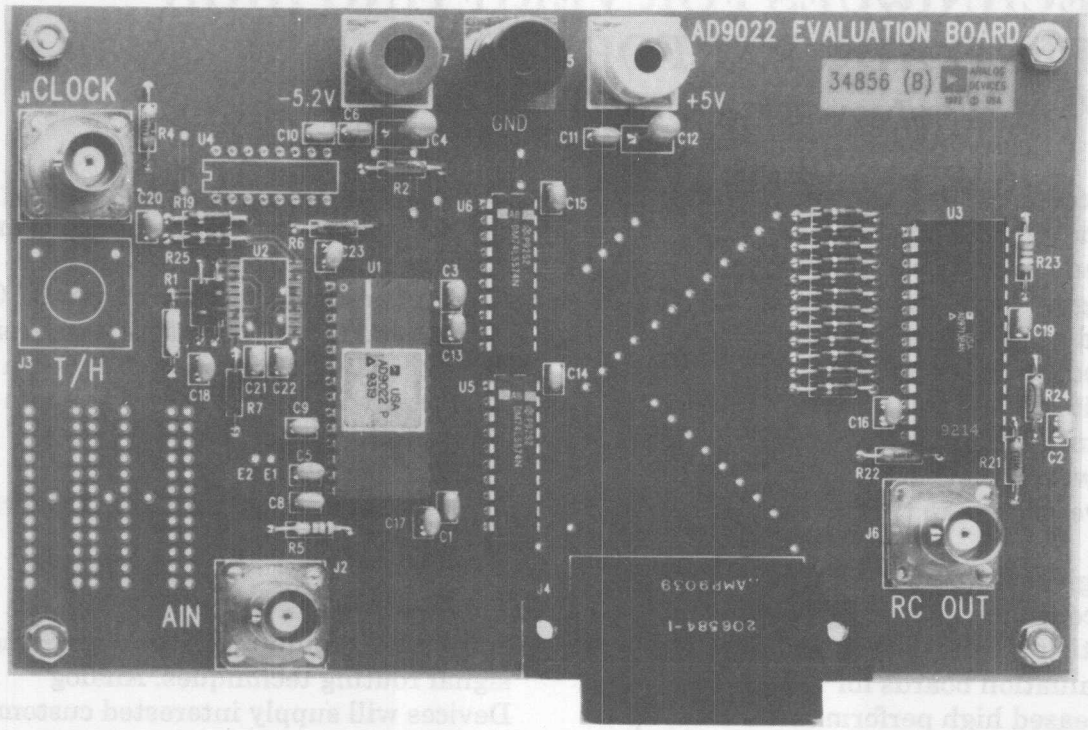


Figure 16.2

ANALOG TECHNIQUES FOR EVALUATION OF ADC STATIC TRANSFER FUNCTIONS

DC linearity measurements are easily accomplished by applying a very low frequency low amplitude triangular wave to the ADC and observing the DAC output on an oscilloscope. A typical output is shown in Figure 16.3. The frequency of the triangular wave form is chosen such that several samples are taken at each ADC code level. With a 10MSPS ADC, a 1 to 10kHz frequency is about right. The performance of the DAC selected for use on the evaluation board should minimize its contribution to the total system errors.

If the signal from the evaluation board input to the DAC output has a phase inversion (as is the case when the ADC is driven with an inverting op amp), the analog input may be subtracted from the DAC output with the simple resistor divider as shown in Figure 16.1. This generates the actual ADC error waveform. Again, a triangular waveform is applied, and the frequency is chosen such that there are many samples taken per code level. The oscilloscope display can now be examined in detail for differential and integral nonlinearity in the ADC dc transfer function. Figure 16.4 shows a typical error waveform display for a low frequency ramp input. If the evaluation board does not have a phase inversion, it may be

performed externally. In fact, the actual subtraction function can be accomplished using the channel-invert and the channel-addition features on a dual-trace oscilloscope. When performing the subtraction with a scope, however, the amplitude of the signal must be kept very low in order to prevent potential waveform distortion due to scope overdrive.

DAC RECONSTRUCTION OF ADC OUTPUT FOR LOW-AMPLITUDE, LOW FREQUENCY TRIANGULAR WAVE INPUT

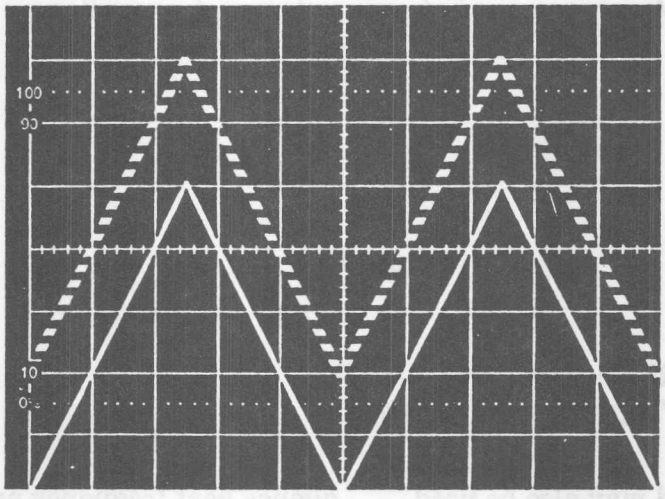


Figure 16.3

The methods described above will allow visual observation of the static transfer characteristic of high speed ADCs having resolutions up to 12 bits. Beyond 12 bits, however, noise, DAC errors, etc., require the use of other methods such as histograms in order to make the measurement accurately.

SUBTRACTING THE DAC OUTPUT FROM THE ADC INPUT ALLOWS DIRECT OBSERVATION OF THE ERROR IN THE ADC TRANSFER FUNCTION

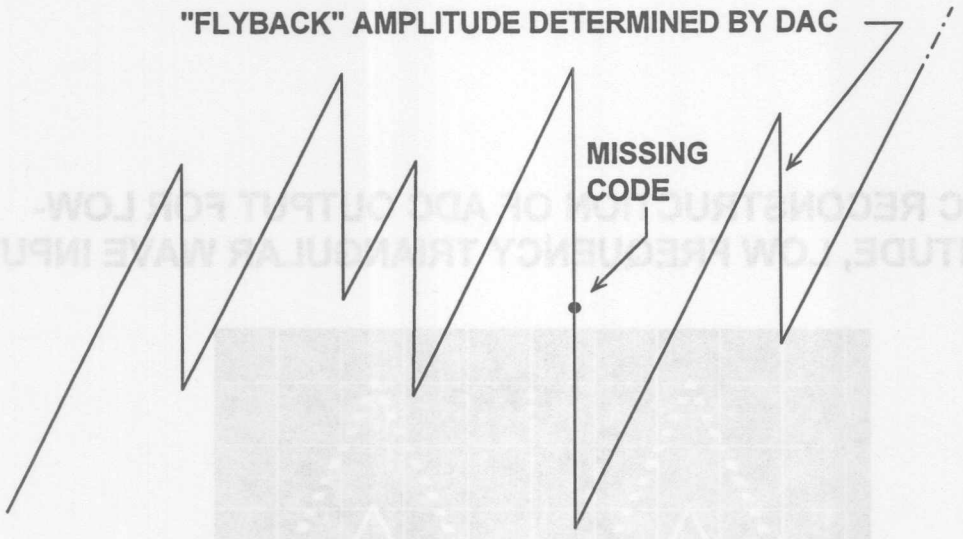


Figure 16.4

ANALOG TECHNIQUES FOR EVALUATING ADC DYNAMIC TRANSFER FUNCTION

The evaluation board may also be used to roughly evaluate the dynamic performance of the ADC by performing a beat frequency test. A block diagram for this test is shown in Figure 16.5.

This test is extremely powerful in evaluating ADCs on the bench because is does not require the use of DSP techniques. A pair of frequency synthesizers is all that is required. The beat frequency test is performed by applying a sinewave input to the ADC which is very slightly offset from the sample clock by a frequency, Δf. This low frequency beat frequency appears at the DAC output due to aliasing as shown in Figure 16.6. The beat frequency is chosen to be small enough so that each ADC code is sampled many times. In order for this frequency to be stable, however, the ADC input frequency must be very stable with respect to the sampling clock frequency. This requires the use of locked frequency synthesizers, or crystal oscillators for the ADC input and the sampling clock. The low frequency beat may be visually analyzed for nonlinearities and missing codes.

BEAT FREQUENCY TEST BLOCK DIAGRAM

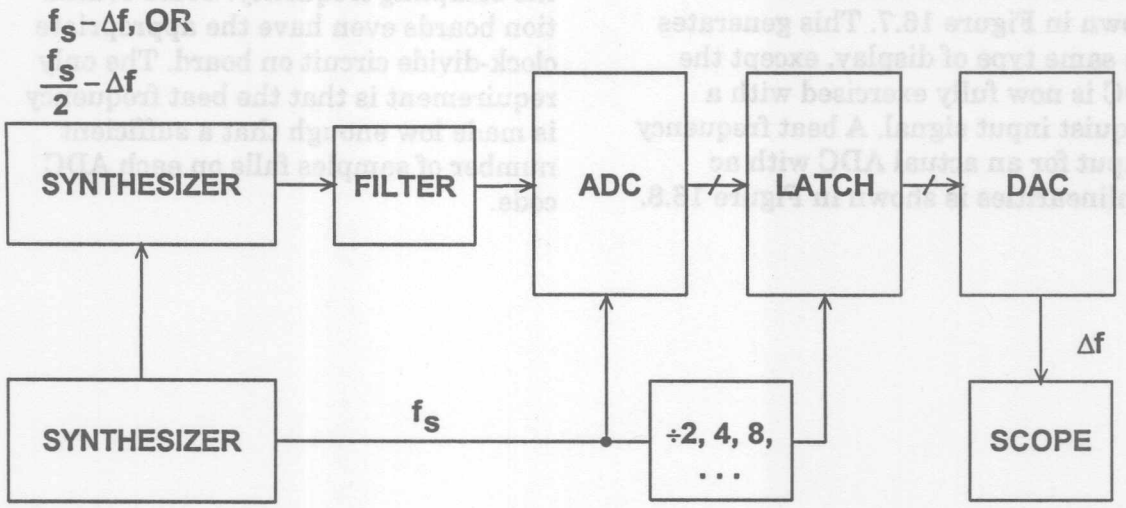


Figure 16.5

BEAT FREQUENCY TESTING

SAMPLING RATE: f_S

SINEWAVE FREQ: $f_S - \Delta f$

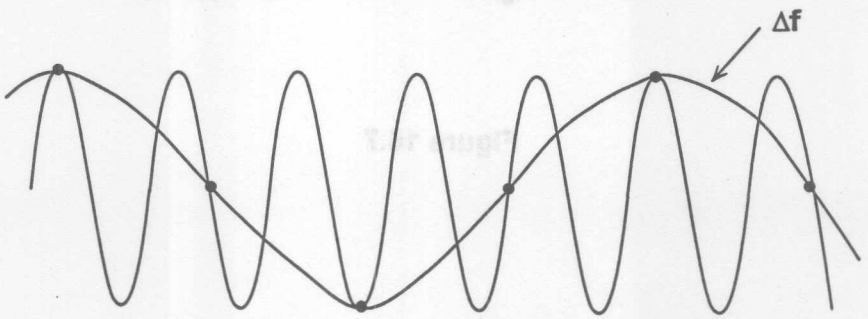


Figure 16.6

The beat frequency test can also be run for an input signal which is slightly offset from the Nyquist frequency, $f_S/2$. In this test, every other sample from the ADC is loaded into the DAC as shown in Figure 16.7. This generates the same type of display, except the ADC is now fully exercised with a Nyquist input signal. A beat frequency output for an actual ADC with ac nonlinearities is shown in Figure 16.8.

In both types of beat frequency test, the effects of DAC glitches and settling time can be minimized by clocking the DAC register with an even sub-multiple of the sampling frequency. Some evaluation boards even have the appropriate clock-divide circuit on board. The only requirement is that the beat frequency is made low enough that a sufficient number of samples falls on each ADC code.

BEAT FREQUENCY TESTING

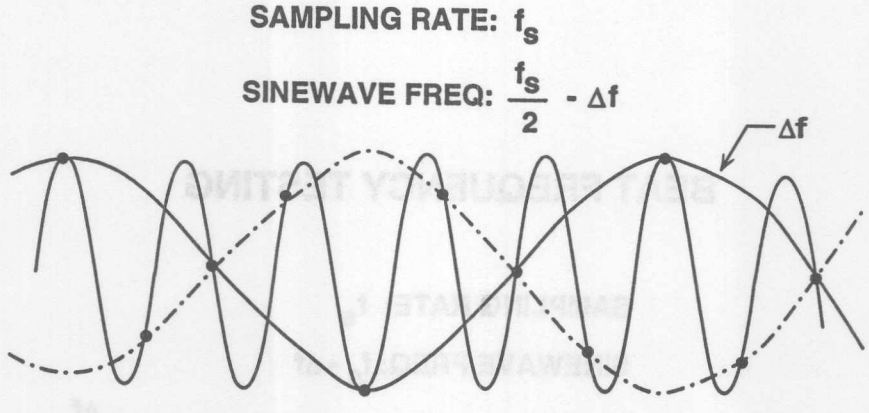


Figure 16.7

BEAT FREQUENCY TEST SHOWS FLASH CONVERTER AC NON-LINEARITIES

FULLSCALE VIEW

EXPANDED VIEW

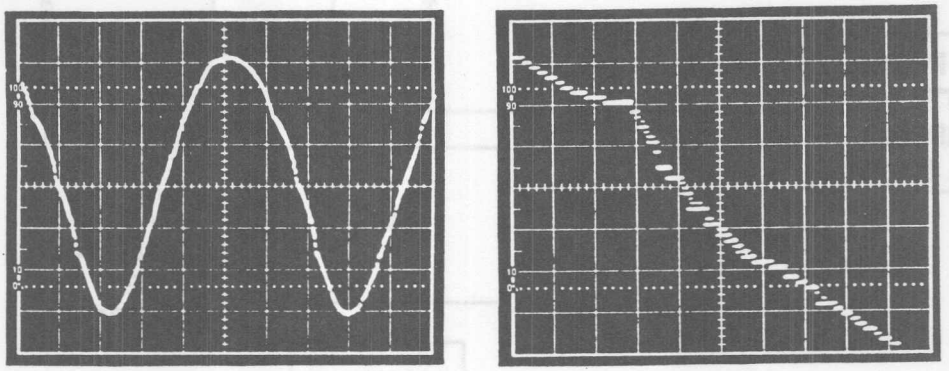


Figure 16.8

BENCH TESTING HIGH SPEED ADCS USING DSP TECHNIQUES

The speed of personal computers and the availability of suitable software now makes DSP bench testing of high speed ADCs relatively easy. A block diagram of a typical DSP PC-based test system is shown in Figure 16.9. In order to perform any DSP testing, the first requirement is a high speed buffer memory of sufficient width and depth. High speed logic analyzers make a convenient memory and eliminate the need for designing special hardware. The HP1663A is a 100MHz logic analyzer which has a simple IEEE-488 output port for easy interfacing to a personal computer. The analyzer can be configured as either a 16-bit wide by 8k deep, or a 32-bit wide by 4k deep memory. This is more than sufficient to test a high speed ADC at sample rates up to 100MHz. For higher sample rates, faster logic analyzers are available, but are fairly costly. An alternative to using a high speed logic analyzer is to operate the ADC at the desired sample rate, but only clock the final output register at an even sub-multiple of the sample clock frequency. This is sometimes called *decimation* and is useful for relaxing memory requirements. If an FFT is performed on the decimated output data, the fundamental input signal and its associated harmonics will be present, but translated in frequency. Simple algorithms can be used to find the locations of the signal and its harmonics provided the original signal frequency is known.

A SIMPLE PC-BASED TEST SYSTEM

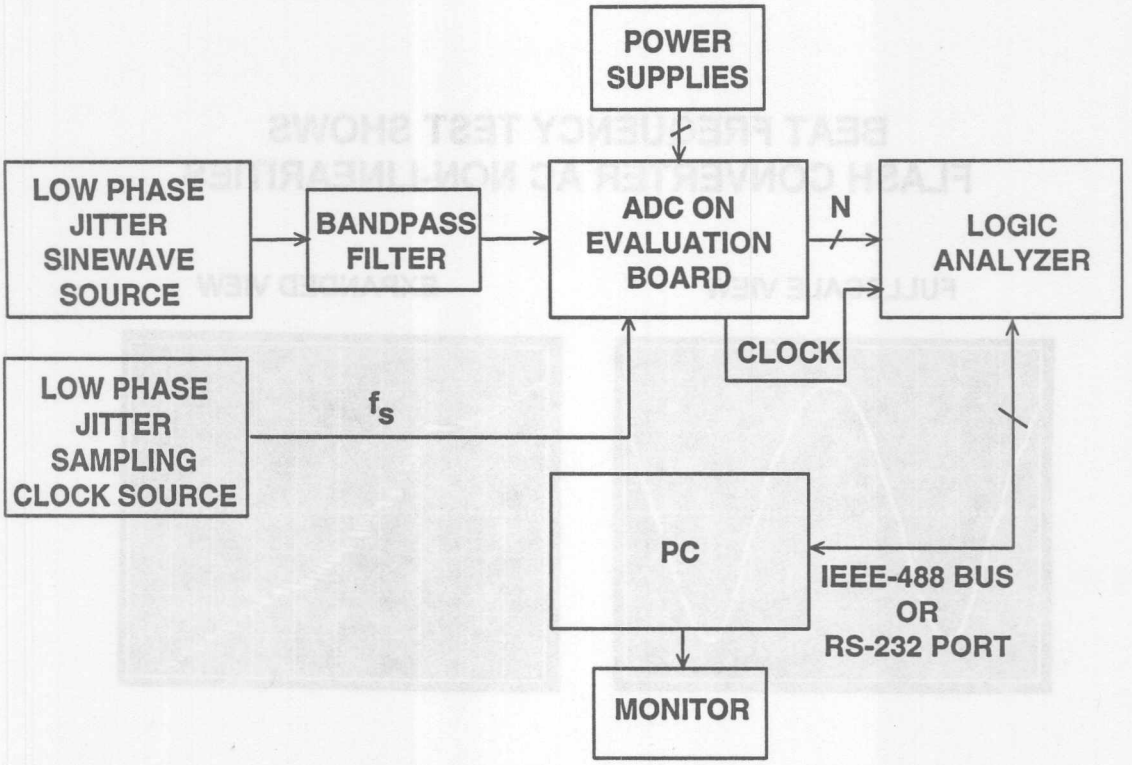


Figure 16.9

AC LINEARITY USING HISTOGRAMS

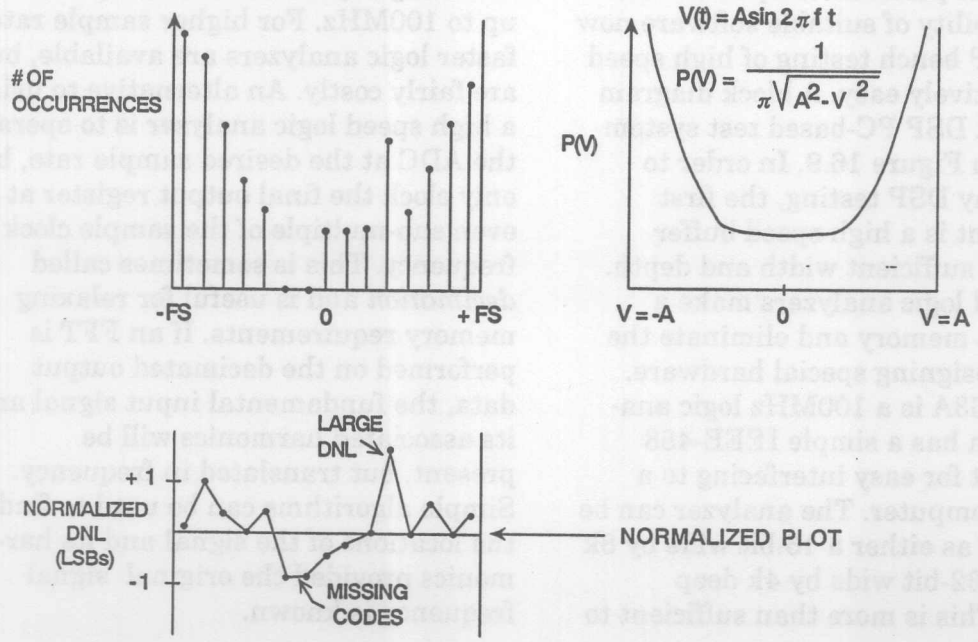


Figure 16.10

Both dc and ac nonlinearity can be measured using the histogram method and this test setup. For this measurement, a fullscale sinewave is applied to the ADC, and a large number of samples are taken. The number of occurrences of each code is recorded on a histogram plot as shown in the top left-hand curve in Figure 16.10. In the case of a 12-bit ADC, several million samples are required in order to achieve statistically significant results. The histogram should follow the ideal probability density distribution of a sinewave, which is shown in the top righthand curve in Figure 16.10. The histogram data is then normalized using the sinewave probability density function to obtain the DNL plot shown in the bottom curve of the figure. The normalized histogram data can be analyzed for DNL, wide codes, and missing codes. This test can be performed for low- and high-frequency inputs to check both static and dynamic ADC nonlinearity.

FFT TESTING

Easy to use mathematical software packages, such as Mathcad™ (available from MathSoft, Inc., 201 Broadway, Cambridge MA, 02139) are available to perform fast FFTs on most 386-based PCs. The use of a co-processor allows a 4096-point FFT to run in a few seconds on a 33MHz,386 PC. The entire system will run under the Windows environment and provide graphical displays of the FFT output spectrum. It can be programmed to perform SNR, THD, and SFDR computations. A simple QuickBasic program transfers the data stored in the logic analyzer into a file in the PC via the IEEE-488 port.

Properly understanding of FFT fundamentals is necessary in order to achieve meaningful results. The first step is to determine the number of samples, M, in the FFT record length. In order for the FFT to run properly, M must be a power of 2. The value of M determines the frequency *bin width*, $\Delta f = f_S/M$. The larger M, the more frequency resolution. Figure 16.11 shows the relationship between the average noise floor of the FFT with respect to the broadband quantization noise level. Each time M is doubled, the average noise in the Δf bandwidth decreases by 3dB. Larger values of M also tend to give more repeatable results from run to run (see Figure 16.11).

RELATIONSHIP BETWEEN AVERAGE NOISE IN FFT BINS AND BROADBAND RMS QUANTIZATION NOISE LEVEL

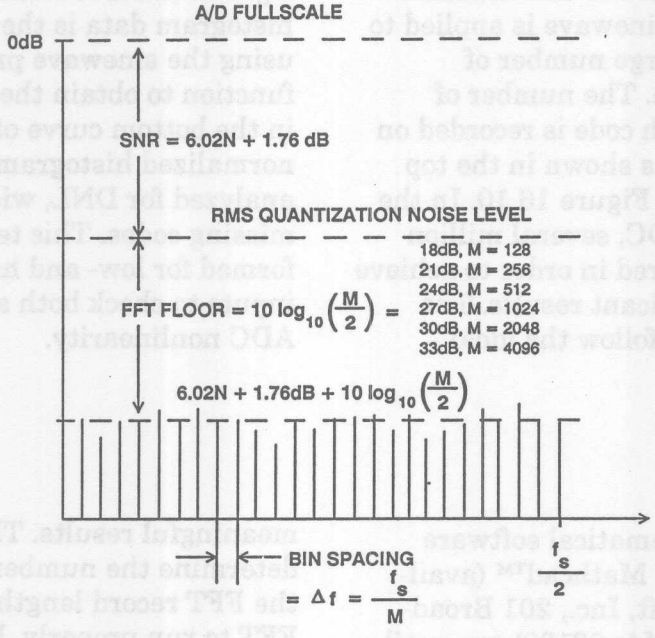


Figure 16.11

M values of 512 (for 8-bit ADCs), 2048 (for 10-bit ADCs), and 4096 (for 12-bit ADCs) have proven to give good accuracy and repeatability. For extremely wide dynamic range applications (such as spectral analysis using the AD9014 14-bit, 10MSPS ADC) M=8192 may be desirable. Rather than use extremely deep FFTs, the data for several shorter FFTs may be averaged before performing the final FFT.

In order to obtain spectrally pure results, the FFT data window must contain an exact integral number of sinewave cycles as shown in Figure 16.12. These frequency ratios must be precisely observed to prevent end-point discontinuity. In addition, it is desirable that the number of sinewave cycles contained within the data window be a prime number. This method of FFT testing is referred to as *coherent* testing because two locked frequency synthesizers are used to insure the proper ratio (coherence) between the sampling clock and the sinewave frequency. The requirements for coherent sampling are summarized in Figure 16.13.

FFT OF SINEWAVE HAVING INTEGRAL NUMBER OF CYCLES IN WINDOW

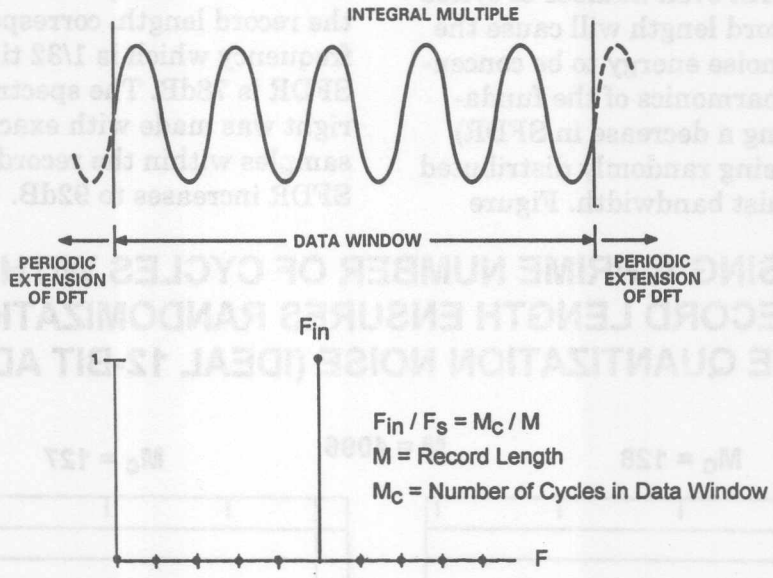


Figure 16.12

REQUIREMENTS FOR COHERENT SAMPLING

- f_s = Sampling Rate
- f_{in} = Input Sinewave Frequency
- M = Number of Samples in Record (Integer Power of 2)
- M_C = Prime Integer Number of Cycles of Sinewave During Record (Makes All Samples Unique)
- Make $\frac{f_{in}}{f_s} = \frac{M_C}{M}$

Figure 16.13

16

Making the number of cycles within the record a prime number ensures a unique set of sample points within the data window. An even number of cycles within the record length will cause the quantization noise energy to be concentrated in the harmonics of the fundamental (causing a decrease in SFDR) rather than being randomly distributed over the Nyquist bandwidth. Figure 16.14 shows a 4096-point FFT output for a theoretically perfect 12-bit sinewave. The spectrum on the left was made with exactly 128 samples within the record length, corresponding to a frequency which is 1/32 times f_S. The SFDR is 78dB. The spectrum on the right was made with exactly 127 samples within the record, and the SFDR increases to 92dB.

CHOOSING A PRIME NUMBER OF CYCLES WITHIN THE FFT RECORD LENGTH ENSURES RANDOMIZATION OF THE QUANTIZATION NOISE (IDEAL 12-BIT ADC)

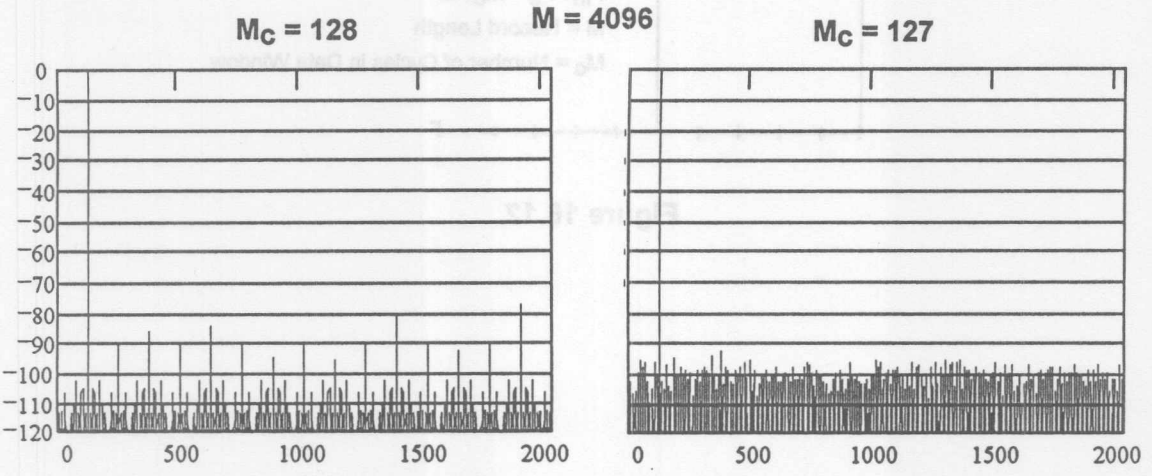


Figure 16.14

Coherent FFT testing ensures that the fundamental signal occupies one discrete line in the output spectrum. Any leakage or smearing into adjacent bins is the result of aperture jitter, phase jitter on the sampling clock, or other unwanted noise due to improper layout, grounding, or decoupling.

If the ratio between the sampling clock and the sinewave frequency is such that there is and endpoint discontinuity in the data (shown in Figure 16.15), then spectral leakage will occur. The discontinuities are equivalent to multiplying the sinewave by a rectangular windowing pulse which has a sin(x)/x frequency response. The discontinuities in the time domain result in leakage or smearing in the frequency domain, because many spectral terms are needed to fit the discontinuity. Because of the endpoint discontinuity, the FFT spectral response shows the main lobe of the sinewave being smeared, and a large number of associated sidelobes which have the basic characteristics of the rectangular time pulse. This leakage must be minimized using a technique called *windowing* (or *weighting*) in order to obtain usable results in non-coherent tests.

FFT OF SINEWAVE HAVING NON-INTEGRAL NUMBER OF CYCLES IN WINDOW

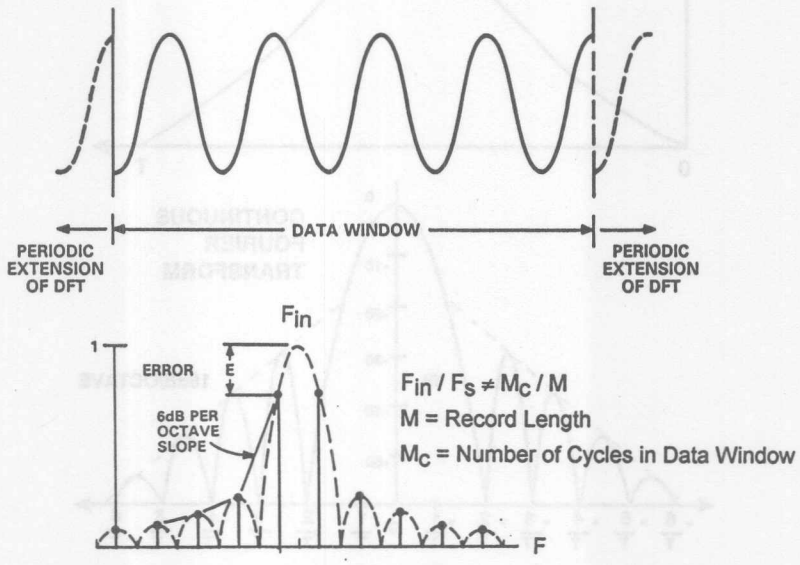


Figure 16.15

This situation is exactly what occurs in real-world spectral analysis applications where the exact frequencies being sampled are unknown and uncontrollable. Sidelobe leakage is reduced by choosing a *windowing* (or *weighting*) function other than the rectangular window. The input time samples are multiplied by an appropriate windowing function which brings the signal to zero at the edges of the window. The selection of an appropriate windowing function is primarily a tradeoff between main-lobe spreading and sidelobe rolloff.

The time-domain and frequency-domain characteristics of a simple windowing function (the Hanning Window) are shown in Figure 16.16. A comparison of the frequency response of the Hanning window and the more sophisticated Minimum 4-Term Blackman-Harris window is given in Figures 16.17 and 16.18. For general ADC testing with non-coherent input frequencies, the Hanning window will give satisfactory results. For critical spectral analysis or two-tone IMD testing, the Minimum 4-Term Blackman-Harris window is the better choice because of the increase in spectral resolution.

TIME AND FREQUENCY REPRESENTATION OF THE HANNING WINDOW

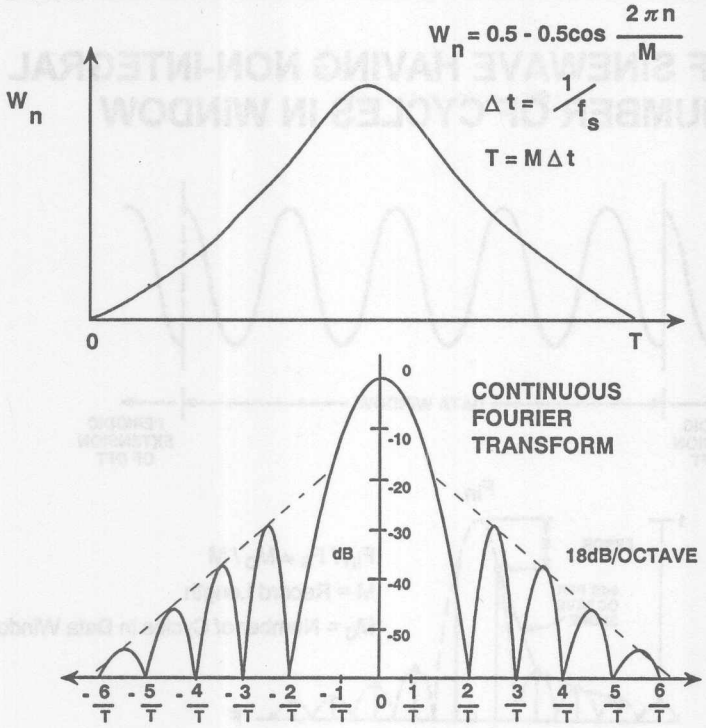


Figure 16.16

FREQUENCY RESPONSE OF THE HANNING WINDOW

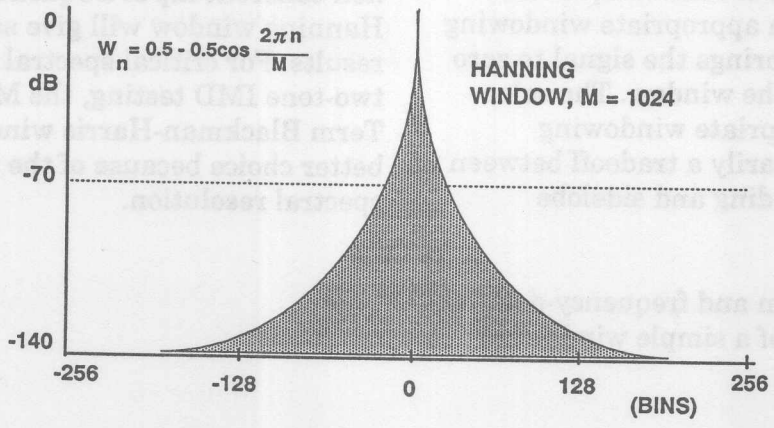


Figure 16.17

FREQUENCY RESPONSE OF THE MINIMUM 4-TERM BLACKMAN-HARRIS WINDOW

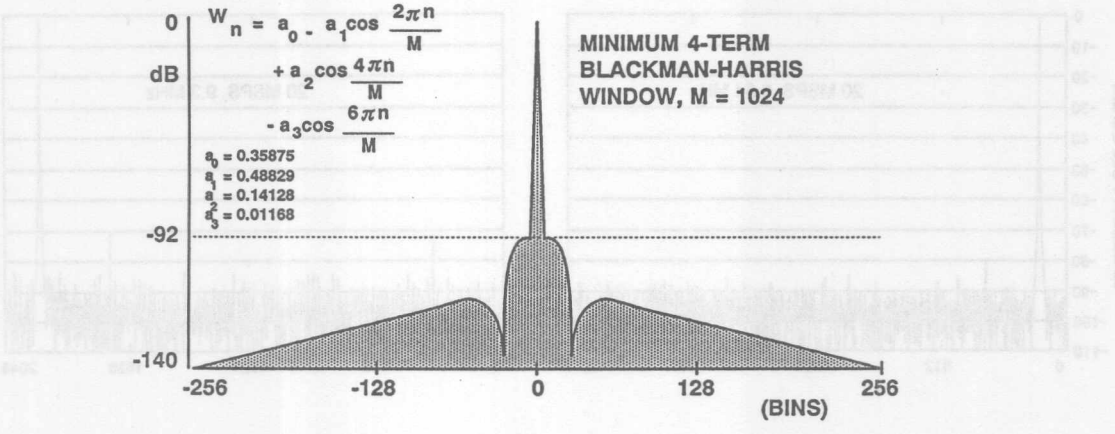


Figure 16.18

The addition of a windowing function to the FFT software involves first calculating the proper coefficient for each time sample within the record. These values are then stored in a memory file. Each time sample is multiplied by its appropriate weighting coefficient before performing the actual FFT. The software routine is easy to implement in QuickBasic.

When analyzing the FFT output resulting from windowing the input data samples, care must be exercised in determining the energy in the fundamental signal and the energy in the various spurious components. For example, sidelobe energy from the fundamental signal should not be included in the rms noise measurement. Consider the case of the Hanning Window function being used to test a 12-bit ADC with a theoretical SNR of 74dB. The sidelobe attenuation of the Hanning Window is as follows:

Bins From Fundamental	Sidelobe Attenuation
2.5	32dB
5.0	50dB
10.0	68dB
20.0	86dB

Therefore, in calculating the rms value of the fundamental signal, you should include at least 20 samples on either side of the fundamental as well as the fundamental itself.

If other weighting functions are used, their particular sidelobe characteristics must be known in order to accurately calculate signal and noise levels.

A typical Mathcad™ FFT output plot is shown in Figure 16.19 for the AD9022 12-bit, 20MSPS ADC using the Hanning Window and a record length of 4096.

MATHCAD™ 4096 POINT FFT OUTPUTS FOR AD9022 12-BIT, 20MSPS ADC (HANNING WEIGHTING)

F_S = 20 MSPS

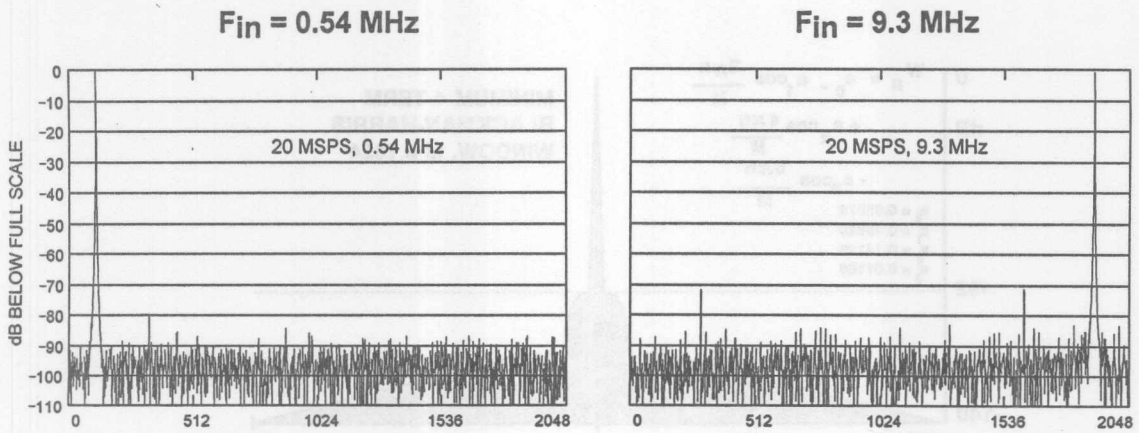


Figure 16.19

The actual QuickBasic routine for transferring the HP analyzer's data to a DOS file in the PC as well as the Mathcad™ routine are given at the end of this section.

TROUBLESHOOTING THE FFT OUTPUT

Erroneous results are often obtained the first time an FFT test setup is put together. The most common error is improper timing of the latch strobe to the buffer memory. The HP1663A logic analyzer accepts parallel data and a clock signal. It has an internal DAC which may be used to examine a record of time samples. Large glitches on the stored waveform probably indicate that the timing of the latch strobe with respect to the data should be changed.

After ensuring correct timing, the FFT routine should produce a reasonable spectral output. If there are large values of harmonics, the input signal may be overdriving the ADC at one or both ends of the range. After bringing the signal within the ADC range (usually about 1dB below fullscale), excess harmonic content becomes more difficult to isolate.

Make sure that the sinewave input to the ADC is spectrally pure. Bandpass filters are usually required to clean up the output of most high frequency oscillators, especially if wide dynamic range is expected.

After ensuring the spectral purity of the ADC input, make sure the data output lines are not coupling to either the

sampling clock or to the ADC analog input. Remember that the glitches produced on the digital lines are signal-dependent and will therefore contribute to harmonic distortion if they couple into either one of these two lines. The use of an evaluation board with separate sampling clock and analog input connectors will usually prevent this. The special ribbon cable used with the logic analyzer to capture the ADC output data has a controlled impedance and should not cause performance degradation.

In addition to the above hardware checks, the FFT software should be verified by applying a theoretically perfect quantized sinewave to the FFT and comparing the results to theoretical SNR, etc. This is easy to do using the "roundoff" function available in most math packages. The effects of windowing non-coherent inputs should also be examined before running actual ADC tests.

QuickBasic Routine for Transferring Data from Logic Analyzer to DOS File over IEEE-488 Bus

```
'IEEE 488 interface routine for IOTECH Interface and HP1663A Logic Analyzer
'HP1663A 488 Address = 07
'ADC data is stored in filename FFTDATA.DAT
'This program works with a 12 Bit ADC

DEF FNPEEKW (addr) = PEEK(addr) + 256 * PEEK(addr + 1)


CLS


OPEN "\DEV\IEEEOUT" FOR OUTPUT AS #1
OPEN "\DEV\IEEEIN" FOR INPUT AS #2

IOCTL #1, "BREAK"
PRINT #1, "RESET"
PRINT #1, "ABORT"
PRINT #1, "LOCAL 07"
PRINT #1, "OUTPUT 07;BEEP"
INPUT ZZ$

DIM i AS INTEGER, ii AS INTEGER, count AS INTEGER, pts AS INTEGER
pts = 8192
DIM adcdata(pts) AS INTEGER




PRINT #1, "OUTPUT 07;:SYSTEM:HEADER ON"
PRINT #1, "OUTPUT 07;:SYSTEM:LONGFORM ON"
PRINT #1, "OUTPUT 07;:SELECT 1"
PRINT #1, "OUTPUT 07;:SYSTEM:DATA?"

Q$ = SPACE$(203)
QSEG = VARSEG(Q$)
RDESC = 0
RDESC = VARPTR(Q$)


PRINT #1, "ENTER 07 #203 BUFFER"; QSEG; ":"; FNPEEKW(RDESC + 2)
PRINT #1, "WAIT"

D$ = SPACE$(6144)
DSEG = VARSEG(D$)
RDESC = 0
RDESC = VARPTR(D$)
count = 1
FOR ii = 1 TO pts / 1024

PRINT #1, "ENTER 07 #6144 BUFFER"; DSEG; ":"; FNPEEKW(RDESC + 2)
PRINT #1, "WAIT"

FOR i = 1 TO LEN(D$) STEP 6
adcdata(count) = ASC(MID$(D$, i, 1)) * 16
adcdata(count) = adcdata(count) + ASC(MID$(D$, i + 1, 1))
count = count + 1
```

```
NEXT i
NEXT ii

OPEN "c:\fftdata.dat" FOR OUTPUT AS #3
SCREEN 9
VIEW (30, 10)-(600, 300), 1, 1
WINDOW (0, 0)-(pts, 4096)
FOR i = 1 TO pts
PSET (i, adcdata(i))
WRITE #3, adcdata(i)
NEXT i
CLOSE #3
PRINT #1, "LOCAL 07"
```

Mathcad™ FFT Program

$pts := 4096$

$numbts := 12$

$lsbs := 2^{numbts}$

$i := 0 .. pts - 1$

$t_i := READ(FFTDATA)$

$t_i := t_i - 2048$ **! Makes Data Bipolar !**

$hi := max(t)$

$lo := min(t)$

$fund := 20 \cdot \log\left(\frac{hi - lo}{lsbs}\right)$ $fund = -0.97$

$w_i := .5 - \left(.5 \cdot \cos\left(\frac{2 \cdot \pi \cdot i}{pts}\right)\right)$ **! Hanning Window !**

$t_i := w_i \cdot t_i$

$c := FFT(t)$

$j := 0 .. \frac{pts}{2}$

$d_j := |c_j|$

$f_j := d_j \cdot d_j$

$d_j := d_j + 1 \cdot 10^{-10}$

$d_j := \left(20 \cdot \log\left(d_j\right)\right)$

$a_j := -200$

$fund1 := max(d)$

$d_j := (fund - fund1) + d_j$

$e_j := until\left[\left(fund - d_j\right) - 1, 0\right]$

$fundat := last(e)$ $fundat = 1905$

$secondat := 2 \cdot fundat$

$thirdat := 3 \cdot fundat$

$$secondat := if\left[\left(secondat > \frac{pts}{2}\right), |pts - secondat|, secondat\right]$$

secondat = 286

$$thirdat := if\left[\left(thirdat > \frac{pts}{2}\right), |pts - thirdat|, thirdat\right]$$

thirdat = 1619

$j := secondat - 3 .. secondat + 3$

$a_j := d_j$

$second := max(a)$ second = -81

$a_j := -200$

$j := thirdat - 3 .. thirdat + 3$

$a_j := d_j$

$third := max(a)$ third = -77.2

$noise := 0$

$noise1 := 0$

$j := (fundat - 20) .. (fundat + 20)$

$$fundeng := \sum_j f_j$$

$j := (secondat - 2) .. (secondat + 2)$

$$secondeng := \sum_j f_j$$

$j := (thirdat - 2) .. (thirdat + 2)$

$$thirdeng := \sum_j f_j$$

$j := 3 .. fundat - 20$

$$noise1 := \sum_j f_j$$

$$j := fundat + 20 .. \frac{pts}{2}$$

$$noise := \sum_j f_j$$

$$noise := noise1 + noise$$

$$avgnoise := \frac{noise}{\left(\frac{pts}{2} - 41\right)}$$

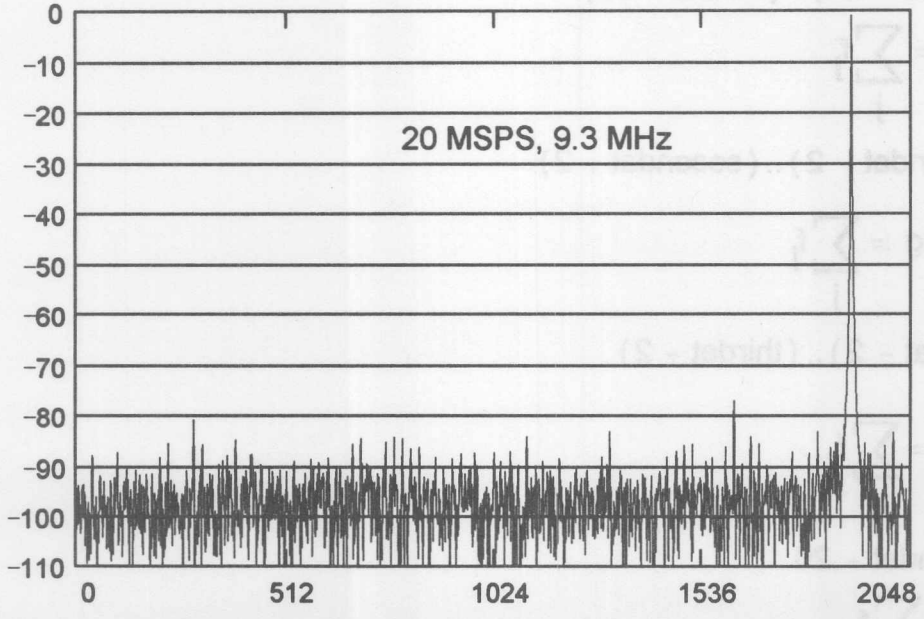
$$noise := noise + 41 \cdot avgnoise$$

$$SNR := 10 \cdot \log\left(\frac{fundeng}{noise}\right) \qquad SNR = 63.1$$

$$j := 0 .. \frac{pts}{2}$$

$$noise := noise - secondeng - thirdeng + 10 \cdot avgnoise$$

$$SNRwo := 10 \cdot \log\left(\frac{fundeng}{noise}\right) \qquad SNRwo = 63.4$$



SNR = 63.1 SNRwo = 63.4 second = -81 third = -77.2 fund = -1

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SECTION 17

HIGH SPEED DACs AND DIRECT DIGITAL SYNTHESIS

- SETTLING TIME
- GLITCH IMPULSE AREA
- HARMONIC DISTORTION AND SPURIOUS FREE DYNAMIC RANGE
- DACs DESIGNED FOR MAXIMUM DYNAMIC RANGE
- WIDE DYNAMIC RANGE DDS SYSTEMS
- INJECTING DIGITAL DITHER IN DDS SYSTEMS TO INCREASE SFDR
- DEGLITCHING DACs USING SHAs
- SIN(x)/x FREQUENCY ROLLOFF EFFECT

SECTION 17

HIGH SPEED DACs AND DIRECT DIGITAL SYNTHESIS

Walt Kester

High speed DACs have many applications in waveform reconstruction and direct digital synthesis (DDS). A new class of function generators called Arbitrary Waveform Generators (ARBs) allow a wide variety of complex waveforms to be programmed into a memory and then read out through a DAC.

Graphics display systems also utilize high speed DACs to direct and/or modulate the scanning electron beam across the CRT screen. A special type of DAC, sometimes referred to as a VIDEODAC, contains functions which allow ease of use in raster scan display systems. Some videodacs, called RAMDACs, contain on-chip color palette memories and provide even more functionality in graphics display systems.

HIGH SPEED DAC APPLICATIONS

- **Instrumentation:**
  - **Waveform Reconstruction,**
  - **Arbitrary Waveform Generators**
- **Direct Digital Synthesis:**
  - **Receiver Local Oscillators**
  - **Frequency Hopping Radios**
  - **Communications Systems**
  - **QAM Systems**
  - **Radar Systems**
- **Graphics Display Systems:**
  - **Vector Scan**
  - **Raster Scan - Videodacs, Ramdacs**

Figure 17.1

SETTLING TIME

Modern fast DACs generally have input registers which drive the internal switches as shown in Figure 17.2. The input latches minimize time-skew between the signals driving the switches and minimize signal-dependent glitches.

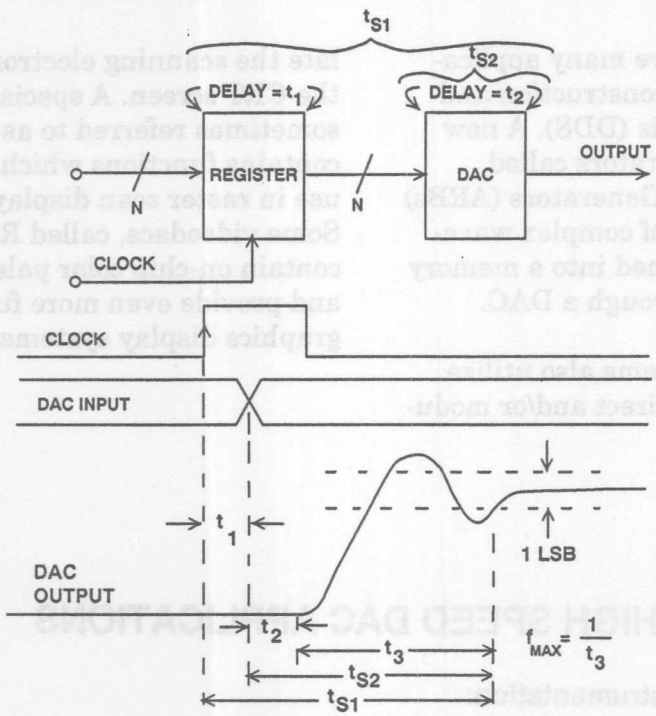


Figure 17.2

The settling time of a DAC is traditionally defined as the time from the digital input transition (usually measured from the 50% point) until the DAC output settles to within a certain error band (usually ±1/2 LSB) which is centered around the final value. As shown in Figure 17.2, a portion of the settling time may be due to a fixed propagation delay through the switches. If the DAC has a set of input latches or registers, the settling time should be measured from the 50% point of the latch strobe or register clock. Fullscale DAC settling time is measured for a digital input transition from 000...0 to 111...1. Midscale settling time is measured for a digital transition from 011...1 to 100...0 or 100...0 to 011...1.

It is often more useful to define DAC settling time with respect to the output alone as shown in Figure 17.3. Settling time is measured from the time the output leaves a ±1/2 LSB error band centered around the initial value until the time the output remains within a ± 1/2 LSB error band centered around the final value. The maximum DAC update rate allowable for ±1/2 LSB fullscale settling time then becomes $f_{max} = 1/t_s$. Faster update rates can be used if sample-to-sample changes in the DAC input are limited to values less than fullscale.

SETTLING TIME DEFINED WITH RESPECT TO DAC OUTPUT

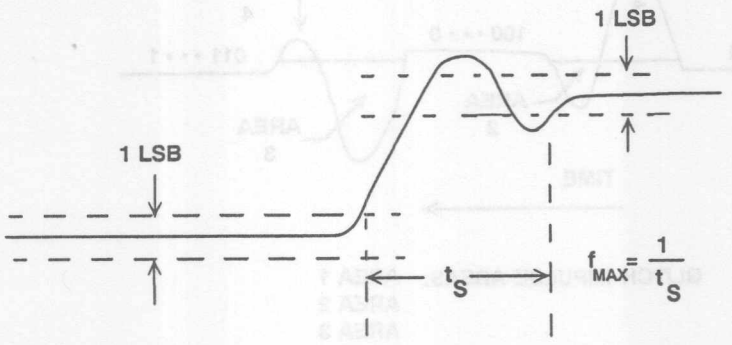


Figure 17.3

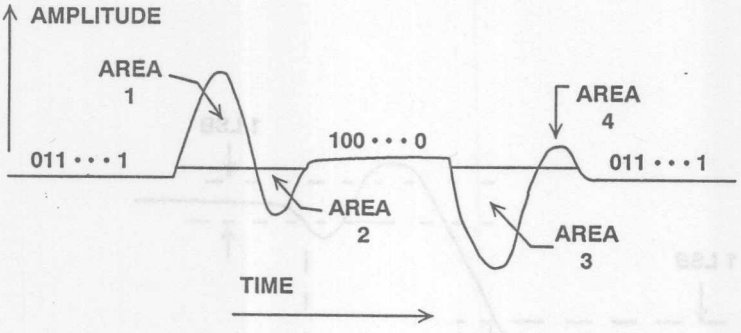
GLITCH IMPULSE AREA

Glitch impulse area is best understood by examining the waveform shown in Figure 17.4. The worst DAC glitches occur because of digital input logic skew and unequal propagation delays through the DAC switches (but there are other types, a noteworthy exception to this being the sigma-delta DAC architecture). These glitches are usually largest at the midscale transition because all bits in the DAC are changing at this point. The glitch produced by the 011...1 to 100...0 transition is usually different from that produced by the 100...0 to 011...1 transition, so each must be analyzed. Glitch impulse area is simply the area of a particular glitch, and is usually measured in the units of pV-sec, therefore the fullscale output voltage of the DAC must be known in order to make meaningful comparisons between DACs. The term *glitch energy* is incorrect since the unit pV-sec is *not* a measure of energy.

From Figure 17.4 it is clear that there are six possible glitch impulse areas to deal with. There are two glitch impulses associated with each transition. Their respective areas are designated 1,2,3, and 4. In addition, it is also useful to consider the *net glitch impulse* area associated with each of the two transitions. There are, respectively, AREA 1 – AREA 2, and AREA 3 – AREA 4. Examining the glitch impulse area specification on a DAC data sheet can lead to confusion unless a considerable amount of clarification is provided by the manufacturer.

Glitch impulse area remains constant regardless of filtering. Fast settling time does not always imply low glitch impulse. The desirable situation is for the DAC to have a net glitch impulse area of zero for each of the two transitions, i.e., AREA 1 – AREA 2 = AREA 3 – AREA 4 = 0. In the ideal case, of

GLITCH IMPULSE WAVEFORMS



GLITCH IMPULSE AREAS: AREA 1
AREA 2
AREA 3
AREA 4

NET GLITCH IMPULSE AREAS: | AREA 1 - AREA 2 |
| AREA 3 - AREA 4 |

Figure 17.4

AD9720 10-BIT, 400MSPS DAC MIDSCALE GLITCH IMPULSE WAVEFORM

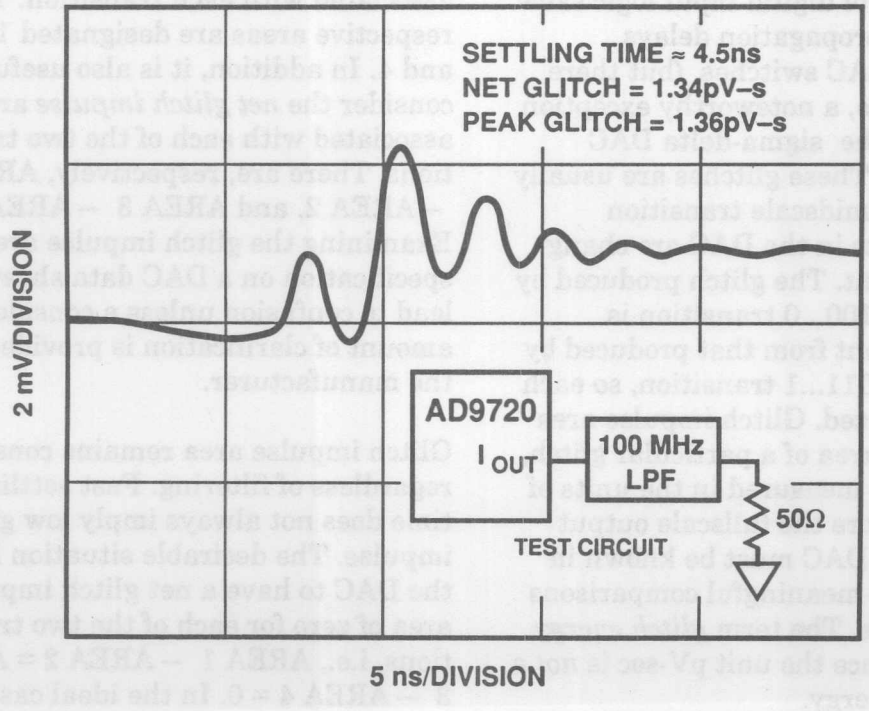


Figure 17.5

course, each of the four areas would be zero. A typical glitch impulse waveform for the AD9720 10-bit, 400MSPS DAC is shown in Figure 17.5. The waveform is for the midscale transition, and shows a net glitch area of 1.34pV-s, and a settling time of about 4.5ns.

HARMONIC DISTORTION AND SPURIOUS FREE DYNAMIC RANGE

Because the net glitch impulse area is code-dependent, it will produce both out-of-band and in-band harmonics when the DAC is reconstructing a sinewave. A net midscale glitch occurs twice during a single cycle of the reconstructed sinewave (at each zero crossing) and, therefore, will produce a second harmonic of the sinewave as shown in Figure 17.6. Note that higher order harmonics of the sinewave which alias back into the Nyquist bandwidth are not filterable. It is difficult to predict the harmonic distortion caused by a specified net glitch impulse area, therefore, both specifications are required to adequately evaluate the dynamic performance of a reconstruction DAC.

EFFECTS OF DAC GLITCHES ON SPECTRAL OUTPUT

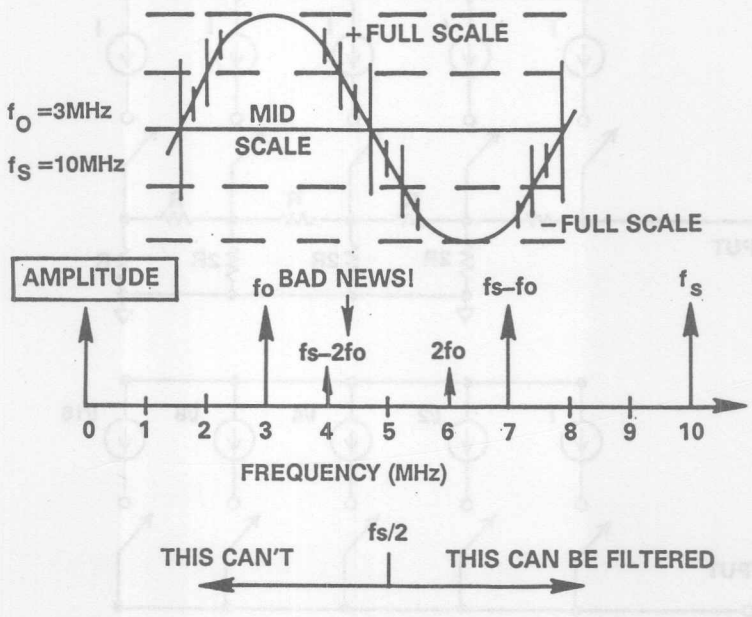


Figure 17.6

DACs Designed For Maximum Dynamic Range

Two fundamental high speed DAC architectures are shown in Figure 17.7. The first method switches equally-weighted currents into an R-2R resistor ladder network which performs the binary weighting. In the second method, the currents are binarily weighted and are switched into a load resistor. Many high speed DACs often use a combination of the above methods.

The large signal-dependent glitches produced by straight binary DACs generate unwanted harmonics of digital input signal. Many high speed DACs use a combination of several techniques to achieve small glitch and wide dynamic range.

If real estate, cost, power, and capacitance were of no consideration, the ideal "glitchless" DAC would consist of $2^N - 1$ equally weighted current switches preceded by latches and decoding logic as shown in Figure 17.8. The glitch produced by switching between levels is code-independent and, therefore, does not generate harmonics of the sinewave being reconstructed. It produces energy at the update rate (and also at multiples of the update rate) which can be filtered from the DAC output. The residual energy causes only a constant dc offset in the output signal. A set of latches is required after the binary decoding logic in order to equalize the delays to the actual switches themselves. The switches are designed using low-level logic levels to minimize coupling to the output.

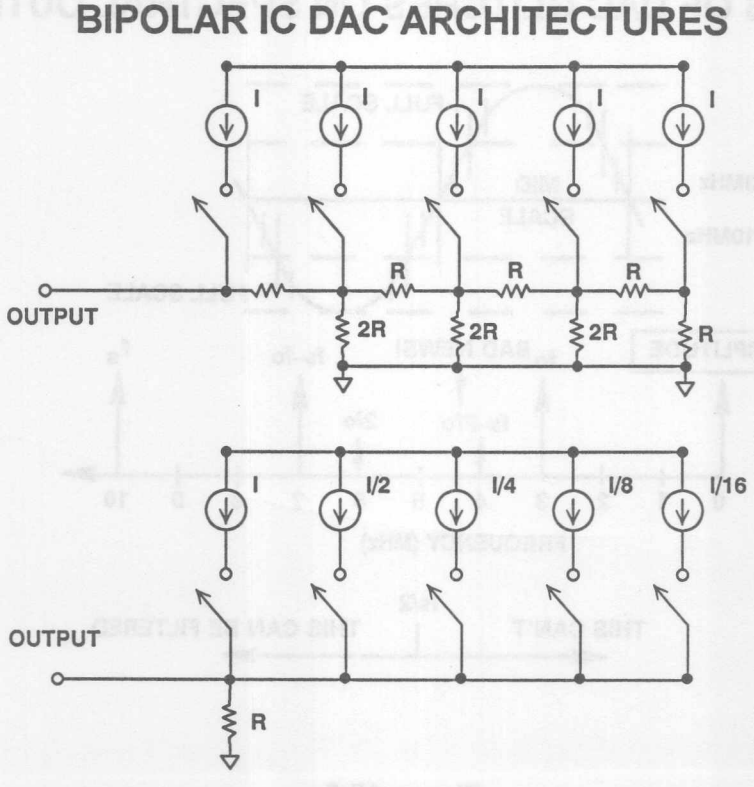


Figure 17.7

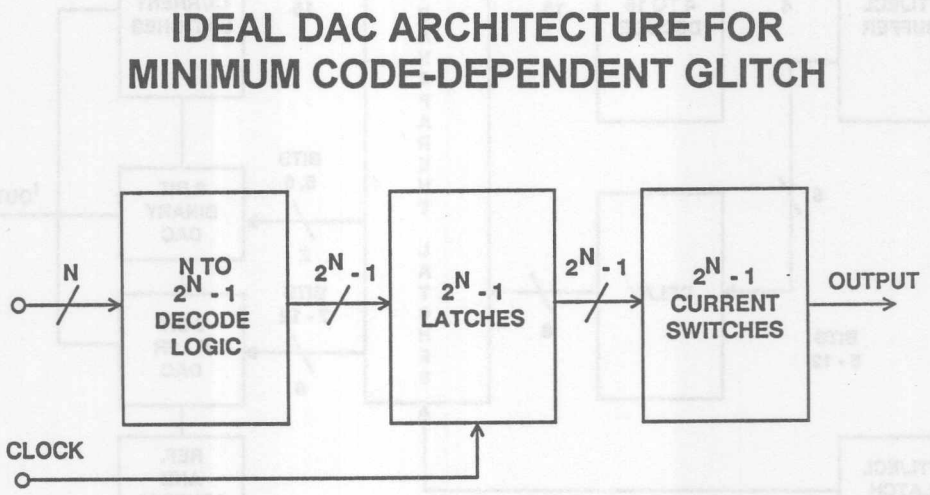


Figure 17.8

Obviously, this scheme is not practical for high resolution DACs, but is often used for the 4 to 6-bit DACs which are used as building blocks in subranging ADCs.

A significant amount of glitch reduction can be achieved by applying the above concept to the first few MSBs of a high resolution DAC in a technique called *segmentation*. This technique is often used in audio DACs.

A block diagram of the AD9712B 12-bit 100MSPS DAC is shown in Figure 17.9 to illustrate the segmented architecture. The four MSBs are decoded into a thermometer code which drives 15 equally weighted current switches after latching. The remaining bits are obtained using binary current weighting (bits 5 and 6) and R-2R current division (bits 7-12). Segmentation of the four MSBs reduces the effects of the midscale glitch impulse by a factor of 16 compared to the glitch which would result if straight binary decoding were employed. This technique used in the AD9712B achieves a glitch area of less than 28pV-s as shown in Figure 17.10.

SEGMENTED ARCHITECTURE USED IN THE AD9712B (ECL) AND AD9713B (TTL) DACs

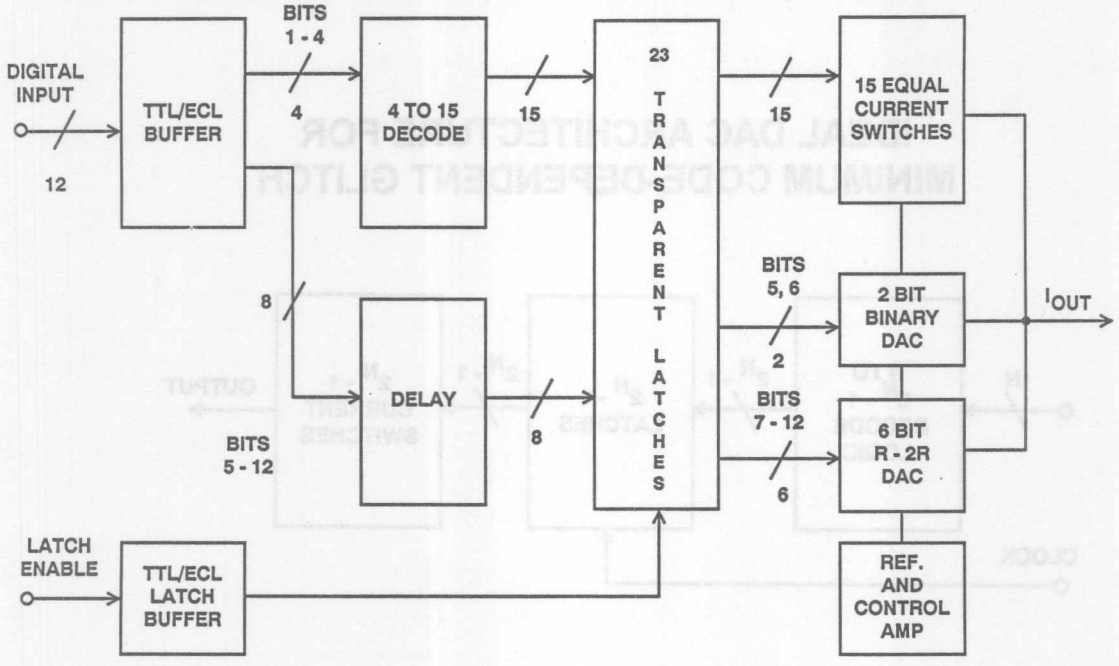


Figure 17.9

AD9712B/AD9713B MIDSCALE GLITCH IMPULSE AND FULLSCALE OUTPUT SIGNAL

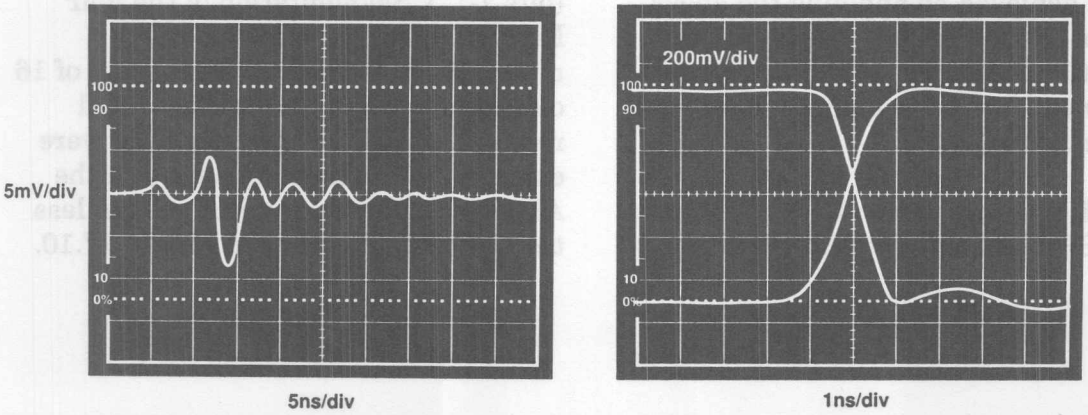


Figure 17.10

WIDE DYNAMIC RANGE DDS SYSTEMS

A simple circuit for generating a digital sinewave using a PROM and a DAC is shown in Figure 17.11. Each location in the PROM corresponds to a discrete sample of the sinewave. The PROM must contain an integral number of cycles in order to prevent a discontinuity when the PROM rolls over. This approach is limited, however, because the sinewave frequency can only be changed by varying the clock rate or by reprogramming the PROM.

A much more flexible scheme is shown in Figure 17.12 and is the basis of modern DDS techniques. The circuit driving the DAC is often referred to as a Numerically Controlled Oscillator (NCO) and serves the same function as the PROM in the simple DDS system described above.

SIMPLE DDS SYSTEM

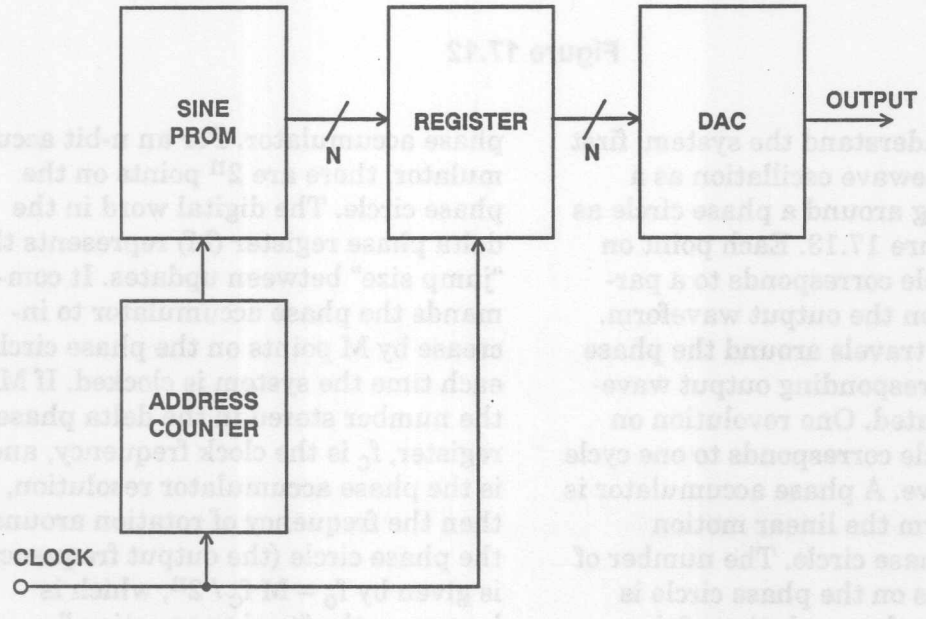


Figure 17.11

A MORE FLEXIBLE DDS SYSTEM

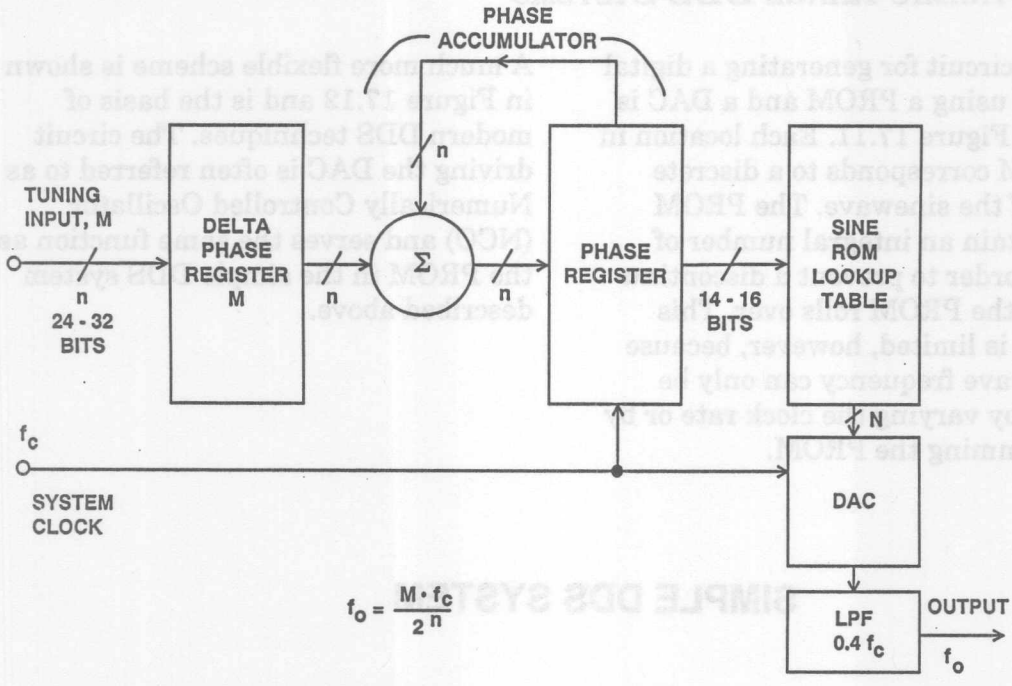
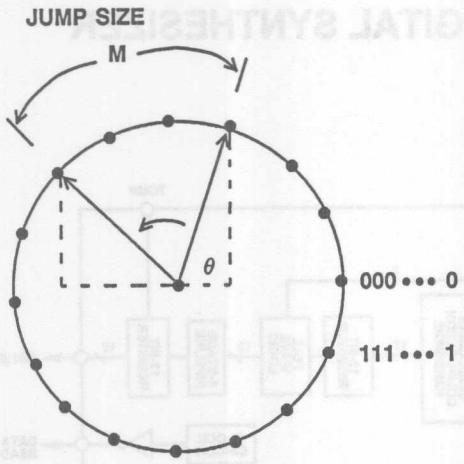


Figure 17.12

In order to understand the system, first consider a sinewave oscillation as a vector rotating around a phase circle as shown in Figure 17.13. Each point on the phase circle corresponds to a particular point on the output waveform. As the vector travels around the phase circle, the corresponding output waveform is generated. One revolution on the phase circle corresponds to one cycle of the sinewave. A phase accumulator is used to perform the linear motion around the phase circle. The number of discrete points on the phase circle is determined by the resolution of the phase accumulator. For an n-bit accumulator, there are 2^n points on the phase circle. The digital word in the delta phase register (M) represents the "jump size" between updates. It commands the phase accumulator to increase by M points on the phase circle each time the system is clocked. If M is the number stored in the delta phase register, f_c is the clock frequency, and n is the phase accumulator resolution, then the frequency of rotation around the phase circle (the output frequency) is given by $f_o = M \cdot f_c / 2^n$, which is known as the "tuning equation."

PHASE ACCUMULATOR OSCILLATOR



DIGITAL PHASE CIRCLE

$$f_O = \frac{M \cdot f_C}{2^n}$$

n	NUMBER OF POINTS
8	256
12	4096
16	65536
20	1048576
24	16777216
28	268435456
32	4294967296

Figure 17.13

The frequency resolution of the system is $f_C / 2^n$ which represents the smallest incremental frequency capable of being produced. The delta-phase register and the accumulator are typically 24 to 32 bits wide.

The output of the phase accumulator drives the address input of a sinewave ROM lookup table in which is stored amplitude information for exactly one cycle of a sinewave. The ROM drives a DAC which reconstructs the analog sinewave. The phase data is usually truncated in order to minimize the size of the ROM and the resolution of the DAC. The phase resolution (corresponding to the number of locations in the ROM) directly affects the spectral purity of the output. For example, if the phase information is truncated to 15 bits, the theoretically largest phase spur is about 90dB below fullscale (neglecting DAC spurs).

A functional block diagram of the AD9955 85MHz Direct Digital Synthesizer is shown in Figure 17.14. It comprises a 32-bit phase accumulator and a 15-bit phase-to-12-bit sine amplitude converter. The phase to sine amplitude converter calculates the sine amplitude using a proprietary algorithm for the first 90° of the sine cycle, and takes advantage of the symmetry of the waveform to calculate the remaining quadrants. Truncation of the phase information to 15-bits and the output data to 12-bits results in a 90dB SFDR as shown in the calculated response of Figure 17.15. The control logic is CMOS compatible, and the clock input is TTL. CMOS outputs are latched on board, and a data ready signal is provided.

AD9955 85MHz DIRECT DIGITAL SYNTHESIZER

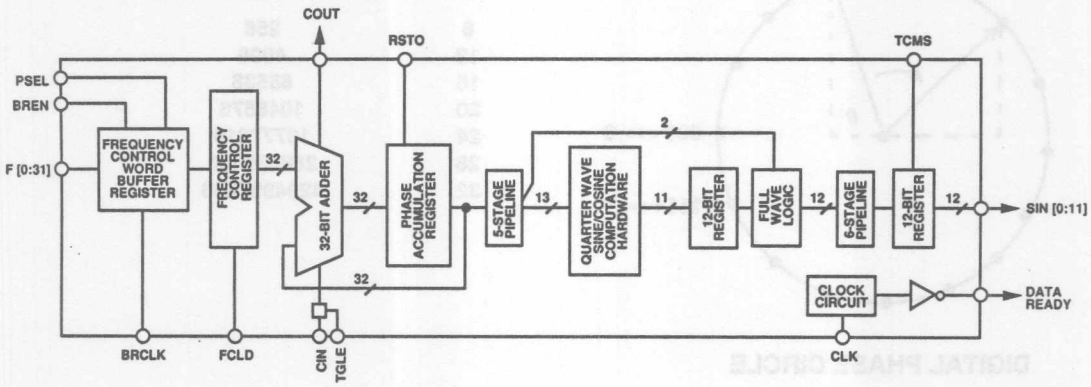


Figure 17.14

AD9955 OUTPUT SPECTRUM (CALCULATED) SHOWS 90dB SFDR FOR 15-BIT PHASE TRUNCATION AND 12-BIT OUTPUT DATA TRUNCATION

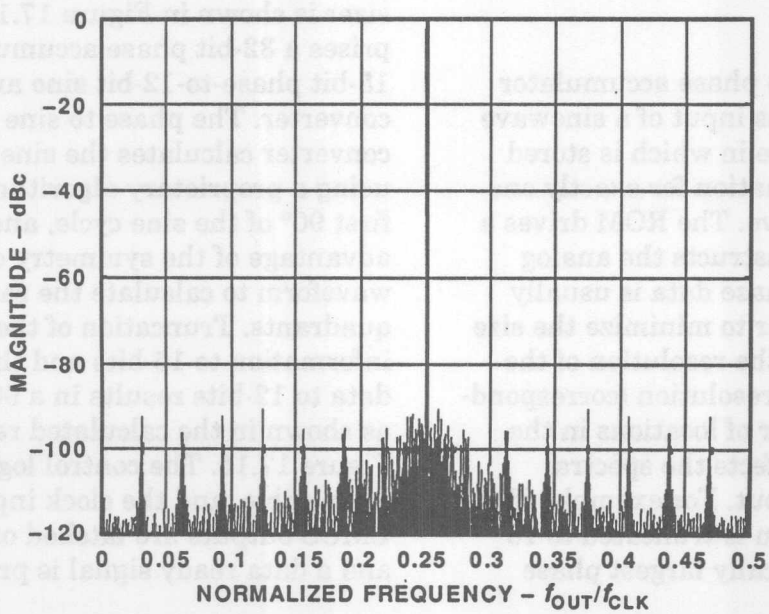


Figure 17.15

Exceptional SFDR performance can be obtained using the AD9955 DDS with the AD9721 10-bit, 100MSPS low glitch DAC as shown in Figure 17.16. As in all high speed applications, proper layout is critical. Analog signal paths should be kept as short as possible and properly terminated to avoid reflections. Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. The digital runs must be kept away from the analog runs and the clock run. The 130Ω series resistors are inserted between the AD9955 outputs and the AD9721 inputs to reduce data feedthrough effects which could impair spectral purity. Layout of the ground circuit is critical. A single, low impedance ground plane is essential. Power supplies should be decoupled to the ground with low inductance ceramic chip capacitors.

An evaluation board (see Figure 17.17) is available which combines the AD9955 and either the AD9713B, an 80MSPS 12-bit DAC, or the AD9721, a 10-bit 100MSPS DAC, both of which are supplied with the board.

AD9955 DIRECT DIGITAL SYNTHESIZER DRIVING AD9721 10-BIT, 100MSPS DAC

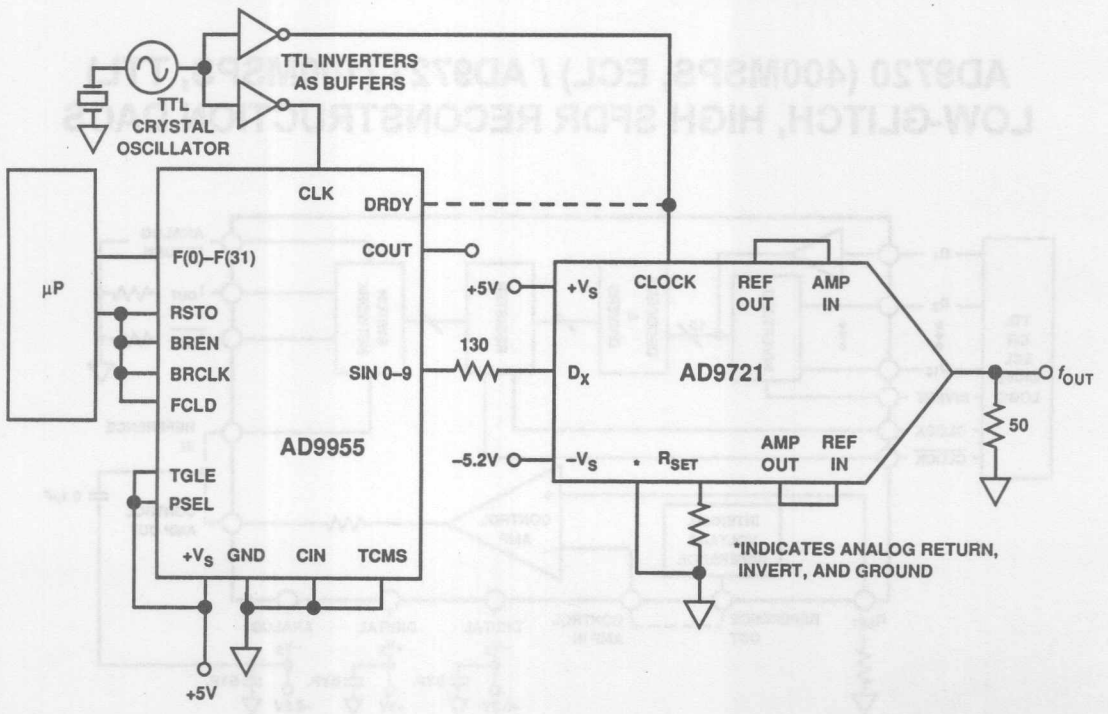


Figure 17.16

17

AD9955 DDS EVALUATION BOARD SETUP

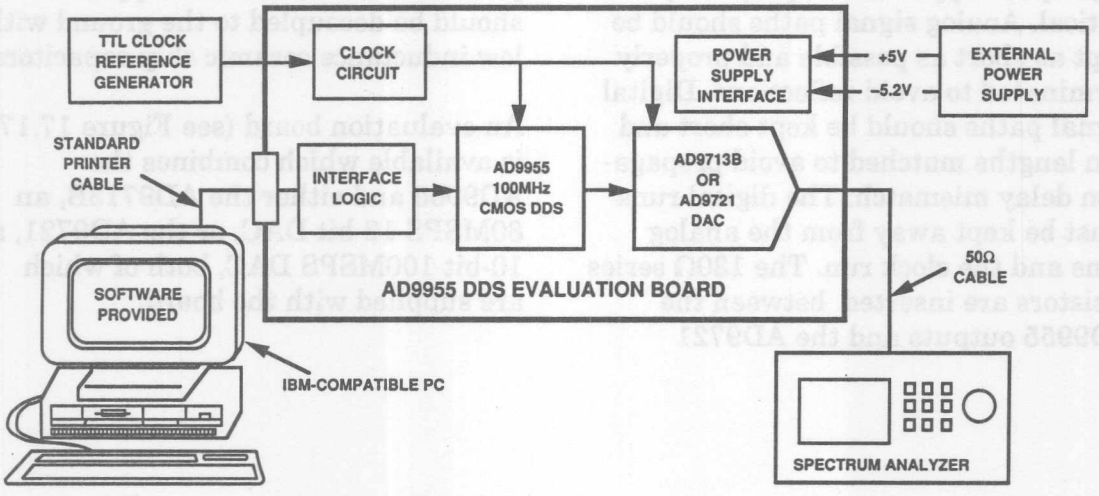


Figure 17.17

AD9720 (400MSPS, ECL) / AD9721 (100MSPS, TTL) LOW-GLITCH, HIGH SFDR RECONSTRUCTION DACS

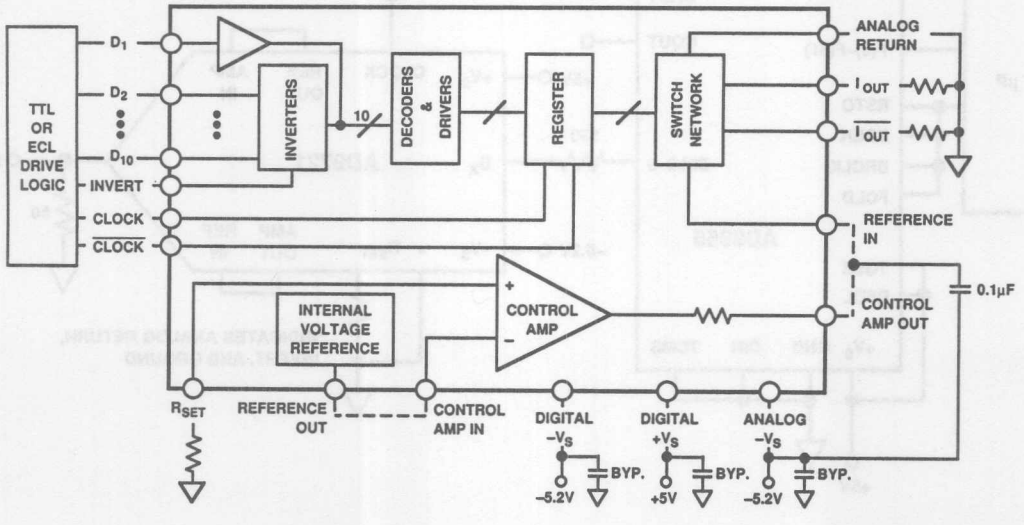


Figure 17.18

AD9720/AD9721 DAC MIDSCALE GLITCH SHOWS 1.34pV-s NET IMPULSE AREA AND SETTLING TIME OF 4.5ns

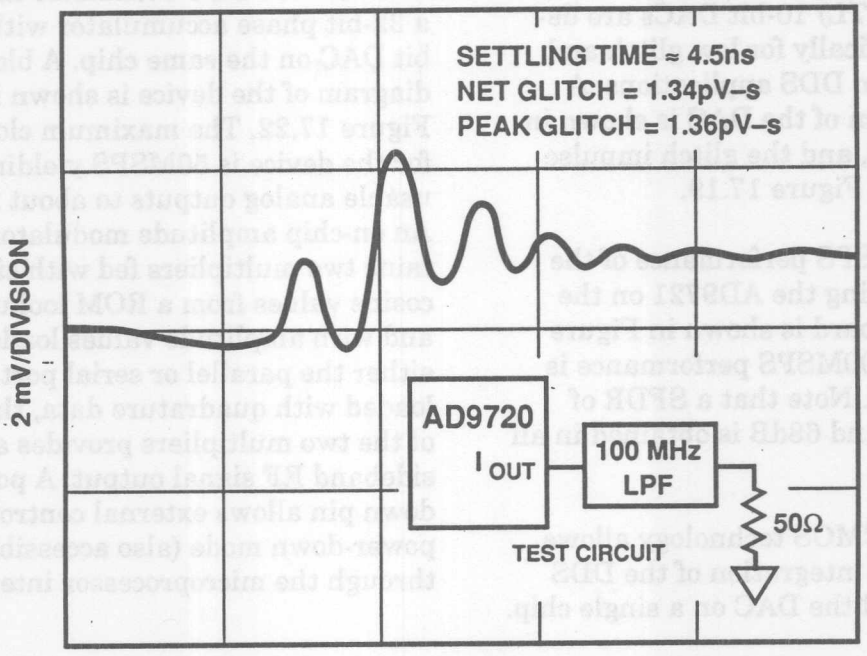


Figure 17.19

AD9955 DDS AND AD9721 DAC PERFORMANCE AT 50MSPS

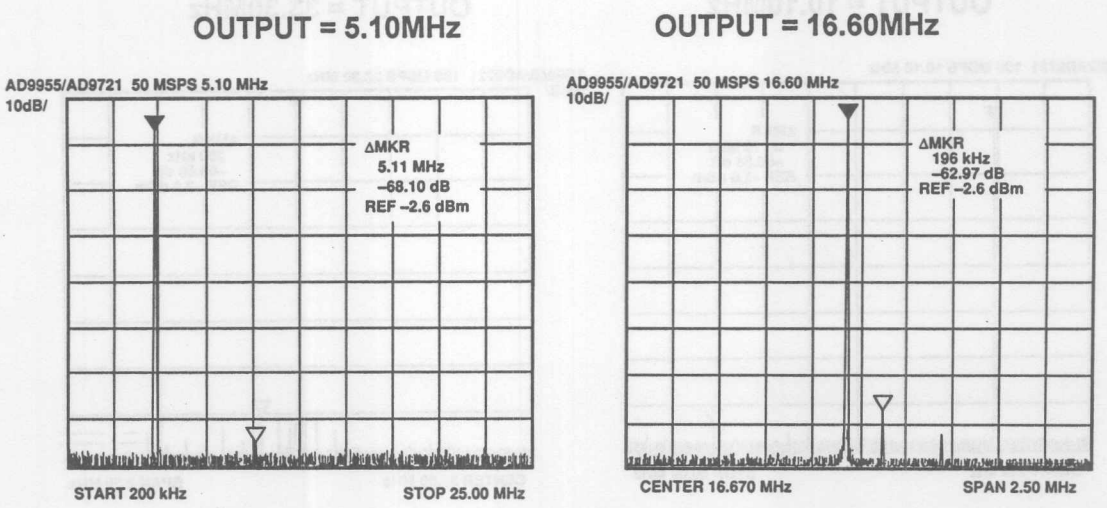


Figure 17.20

The AD9720 (400MSPS ECL) / AD9721 (100MSPS TTL) 10-bit DACs are designed specifically for low glitch and high SFDR in DDS applications. A block diagram of the DAC is shown in Figure 17.18, and the glitch impulse waveform in Figure 17.19.

Typical 50MSPS performance of the AD9955 driving the AD9721 on the evaluation board is shown in Figure 17.20, and 100MSPS performance is Figure 17.21. Note that a SFDR of between 63 and 68dB is obtained in all cases.

High speed CMOS technology allows the complete integration of the DDS oscillator and the DAC on a single chip.

The AD7008 DDS Modulator integrates a 32-bit phase accumulator with a 10-bit DAC on the same chip. A block diagram of the device is shown in Figure 17.22. The maximum clock rate for the device is 50MSPS yielding usable analog outputs to about 20MHz. An on-chip amplitude modulator contains two multipliers fed with sine and cosine values from a ROM lookup table, and with amplitude values loaded from either the parallel or serial port. When loaded with quadrature data, the sum of the two multipliers provides a single-sideband RF signal output. A power-down pin allows external control of a power-down mode (also accessible through the microprocessor interface.

AD9955 DDS AND AD9721 DAC PERFORMANCE AT 100MSPS

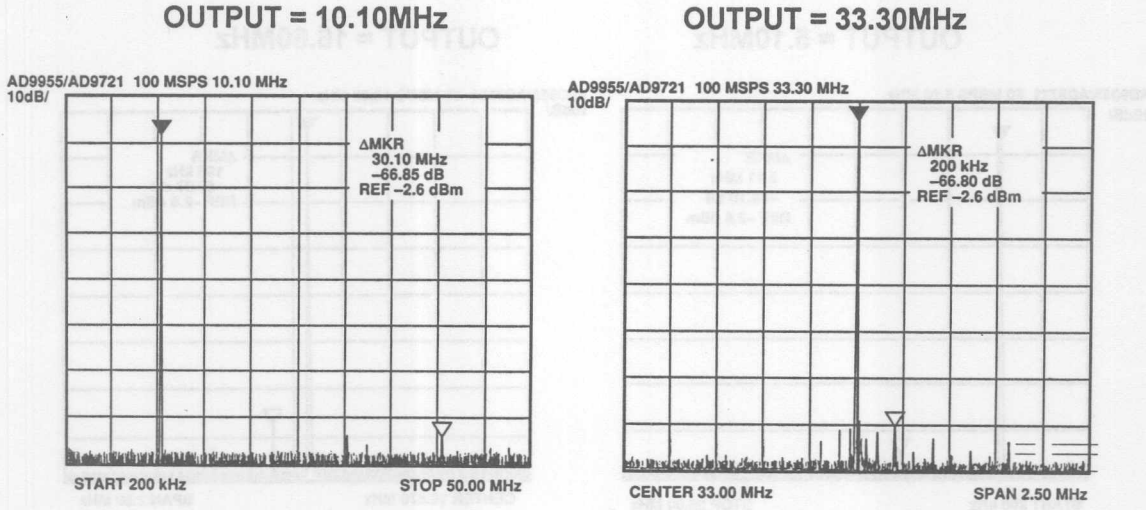


Figure 17.21

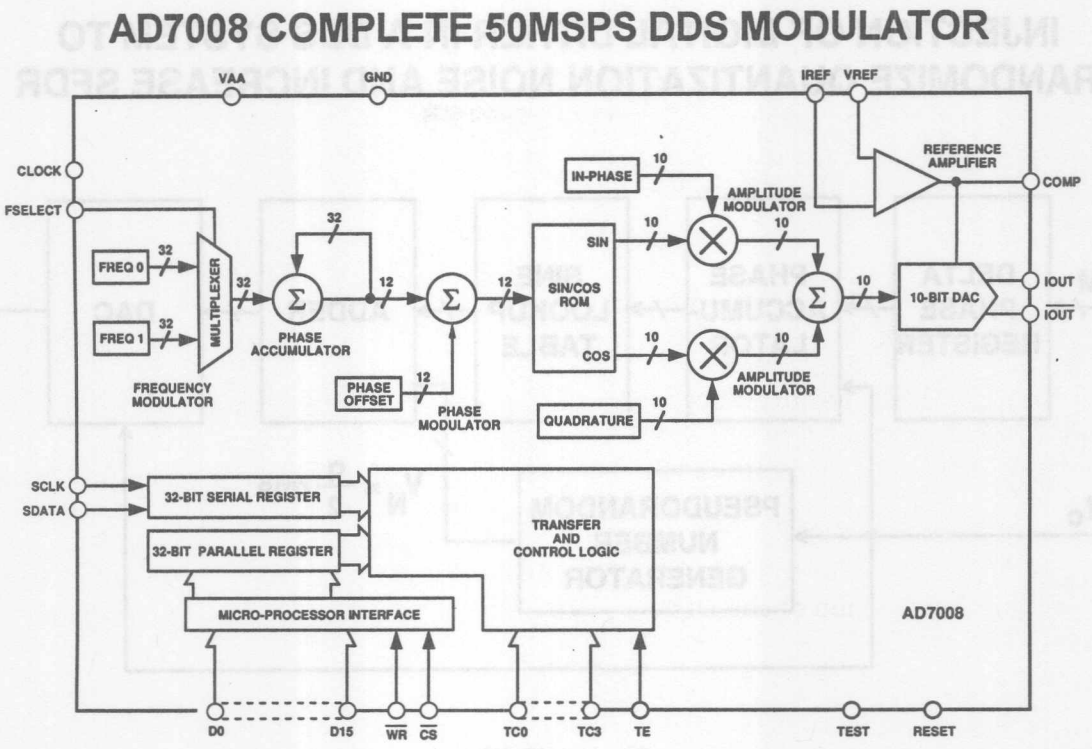


Figure 17.22

INJECTING DIGITAL DITHER IN DDS SYSTEMS TO INCREASE SFDR

Since a DDS system is a sampled data system, the DAC output sinewave has quantization noise superimposed on the fundamental sinewave output. Although the rms value of this noise in the bandwidth dc to $f_S/2$ is $q/\sqrt{12}$, certain ratios between the clock frequency and the output frequency may cause this noise to concentrate in harmonics of the fundamental sinewave, thereby degrading the SFDR. In the case of ADCs, a small amount of broadband noise (rms value of 1/2 LSB) is added to the ADC input to randomize the quantization noise spectrum. The same thing can be done in a DDS system as shown in Figure 17.23 (see Reference 1). The pseudo-random digital noise generator output is added to the DDS sine amplitude word before being loaded into the DAC. The amplitude of the digital noise is set to about 1/2 LSB. This accomplishes the randomization process at the expense of a slight increase in the overall output noise floor.

INJECTION OF DIGITAL DITHER IN A DDS SYSTEM TO RANDOMIZE QUANTIZATION NOISE AND INCREASE SFDR

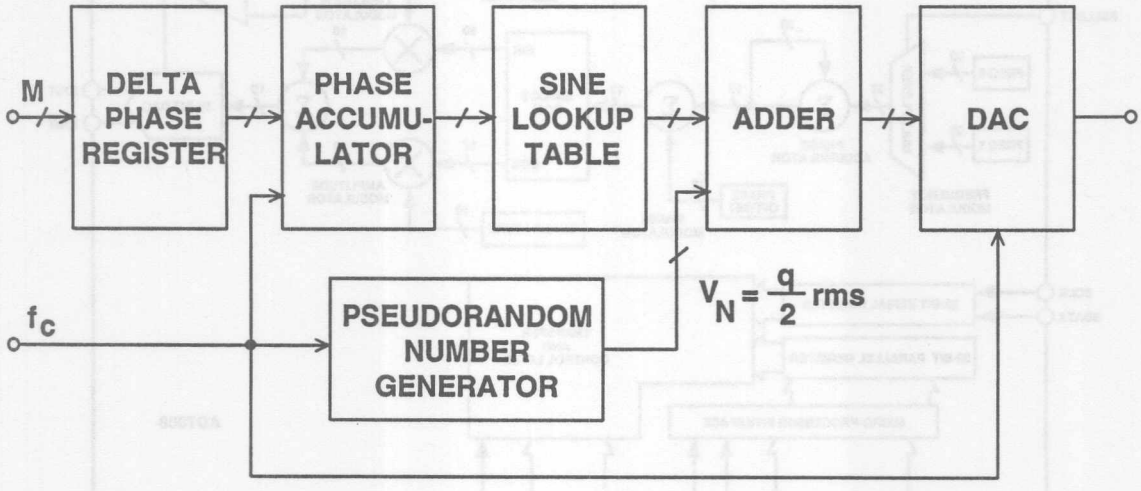


Figure 17.23

DEGLITCHING DACS USING SHAS

SHAs such as the AD9100 and AD9101 can be used to deglitch DACs as shown in Figure 17.24. Just prior to latching new data into the DAC, the SHA is put into the hold mode so that the DAC switching glitches are isolated from the output. The switching transients produced by the SHA are code-independent and occur at the update frequency and hence are easily filterable. However, when using a high performance low glitch DAC such as the AD9712B/ AD9713B or the AD9720/AD9721 there may only be marginal improvement.

SIN(X)/X FREQUENCY ROLLOFF EFFECT

The output of a reconstruction DAC can be visualized as a series of rectangular pulses whose width is equal to the reciprocal of the update rate as shown in Figure 17.25. Note that the reconstructed signal is down 3.92dB at the Nyquist limit with respect to the low frequency value. An inverse sin(x)/x filter is sometimes placed after the DAC to correct for this effect.

DEGLITCHING A DAC OUTPUT USING A SAMPLE-AND-HOLD

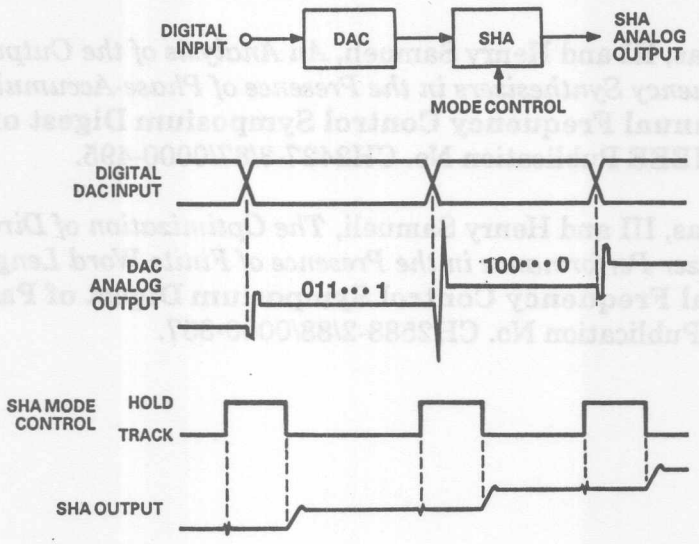


Figure 17.24

(SIN X) / X ROLLOFF

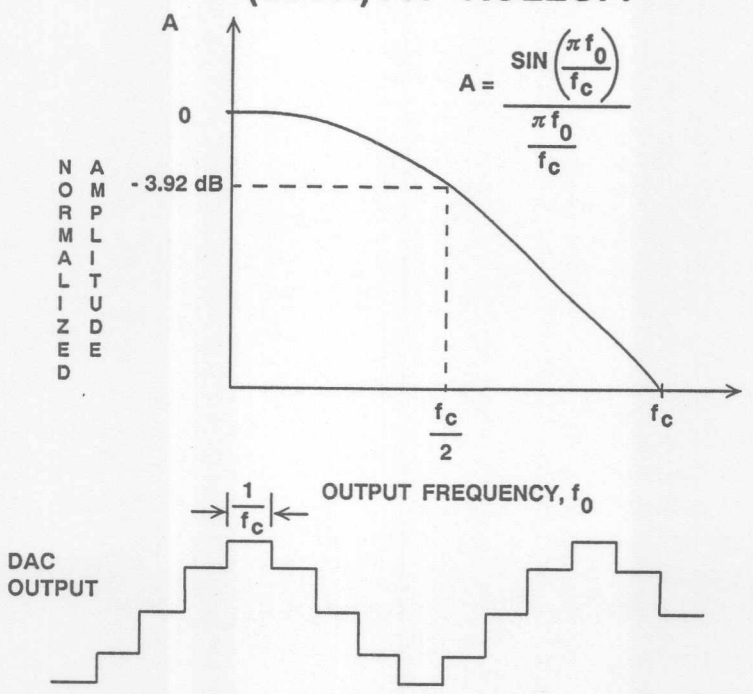


Figure 17.25

REFERENCES

1. Richard J. Kerr and Lindsay A. Weaver, *Pseudorandom Dither for Frequency Synthesis Noise*, United States Patent Number 4,901,265, February 13, 1990.

2. Henry T. Nicholas, III and Henry Samueli, *An Analysis of the Output Spectrum of Direct Digital Frequency Synthesizers in the Presence of Phase-Accumulator Truncation*, **IEEE 41st Annual Frequency Control Symposium Digest of Papers**, 1987, pp. 495-502, IEEE Publication No. CH2427-3/87/0000-495.

3. Henry T. Nicholas, III and Henry Samueli, *The Optimization of Direct Digital Frequency Synthesizer Performance in the Presence of Finite Word Length Effects*, **IEEE 42nd Annual Frequency Control Symposium Digest of Papers**, 1988, pp. 357-363, IEEE Publication No. CH2588-2/88/0000-357.

SECTION 18

SIGNAL COMPUTING APPLICATIONS IN COMMUNICATIONS

- Introduction to Signal Computing: Applications Of Signal Computing, Signal Computing Hardware, Software: Open Architecture the Key, What It All Means
- High Performance Modems For Data Transmission
- The AD28msp01 PSTN Signal Port for V.32 Modems
- The AD20msp500-Series Of Software Programmable PSTN Communications Chipsets And The ADAT-DSI01 DataPump Algorithm Toolkit
- Digital Telephone Answering Machine Solution Using Signal Computing From Analog Devices
- Digital Mobile Radio Overview
- The GSM System

SECTION 18

SIGNAL COMPUTING APPLICATIONS IN COMMUNICATIONS

Walt Kester, Bill Schweber

INTRODUCTION TO SIGNAL COMPUTING

Bill Schweber

Signal Computing is a technology framework and business model which recognizes that DSP-based signal-processing applications can benefit substantially by combining sets of high-performance processor- and interface chips with powerful, sophisticated algorithms from independent third parties. Employing open designs and architectures, signal computing is characterized by well-defined levels of standardization that carefully define the hardware and software roles and the layers that make them up.

SIGNAL COMPUTING: A TECHNOLOGY AND BUSINESS MODEL FOR REALTIME SIGNAL PROCESSING SOLUTIONS

- Hardware Chipsets:
  Analog I/O (Codecs), DSP Processors, ASIC Interface Chips
- Software Algorithms: Independent Algorithm Vendors (IAVs)
- Manufacturing Design Kits
- Typical Applications:
  Modems, Speech Processing, Music Processing, Digital Mobile Radio, Image Processing, Multimedia

Figure 18.1

This allows companies—both chip- and software vendors and OEM and system designers—to participate at the level where each brings maximum "value-added" expertise to the application. The chip supplier furnishes standard high-performance, low-cost ICs; the market-oriented algorithm developer provides the standard configurable software that produces the desired electronic performance from the chips; and the OEM designer integrates them into a system specialized to meet the performance needed within his market niche. This environment avoids saddling the designer with the job of recreating all aspects of the overall design. An example of a signal computing product, a telecommunications modem chipset and algorithm toolkit, is discussed later in this section.

Low-cost digital signal processing is an "enabling" function, allowing broad expansion of *real-time* signal processing, through the combination of software and hardware defined as "signal computing." Signal computing is characterized by the synchronized execution of algorithms on *real-time* data streams. It is quite distinct from the use of DSP, or any processor, in conventional numerical acceleration, where computations and graphics are simply speeded up—but still occur off-line: images are redrawn "more quickly" on the graphics workstation screen, but even though waiting time is reduced, it is still palpable.

In contrast to numerical acceleration, signal computing involves real-time signal processing with a straightforward criterion: if it isn't fast enough for the real-time requirements and synchronization of the application, it simply isn't fast enough. Speeded-up processing alone doesn't help if the real-time constraint can't be satisfied.

End users see signal computing functionality in two distinct forms. First, personal computers (whatever actual form they take) can have signal computing circuitry built in to add those real-time functions (involving intensive computation) that the user needs to access, such as audio, video, and telecommunications capabilities. The software to exercise the hardware for the application must be as available as—or more available than—the hardware, and is generally downloaded into RAM as needed from disk. In this way, new functions can execute on the same hardware, or existing functions can be enhanced with new, more efficient algorithms or incorporate newly defined standards.

Second, in a large number of applications, the signal-computing capabilities are *embedded*, in an essentially non-reprogrammable design, for dedicated use. For example, voice recognition in home "appliances" will be implemented by a carefully defined, fixed-function, minimum-cost subsystem that is optimized for the application, with code in ROM.

APPLICATIONS OF SIGNAL COMPUTING

As low-cost DSP ICs and interface chips, and the software to drive them, are becoming more widely available, signal computing is spurring a mind-boggling expansion of real-time applications that work with real-world information and signals: voice recognition (including voice-programmed operation of mundane products such as VCRs); spoken-word-to-text and spoken-word-to-spoken-word language translation; personal communications systems; fax-to-OCR-to-voice (so that incoming faxes received at your office can be passed to you over the phone); and voice synthesis that is tailored to the application and the listener. CD quality (44-kbps) will be the standard used for audio and music, except in standard voiceband applications, where the higher sampling rates make less sense.

Video has a place among signal computing applications. Under the broad title of "multimedia"—perhaps better characterized as "mixed media"—it allows for integration of audio and video where appropriate. This means that a video signal, along with its audio channel, can be compressed, stored, transmitted, and recreated with perfect synchronization. Video telephones and conferencing are in the cards—especially for business applications, as a ready substitute for costly and time-consuming travel. Video segments can be stored as easily as typed text is now, and then incorporated into picture-and-sound documents and messages. Video processing allows users to perform editing on images, reducing blurring, improving sharpness, and performing other enhancements with the ease-of-use and power of today's word processors.

SIGNAL COMPUTING HARDWARE

The early days of the microprocessor were characterized by a highly fragmented industry without an architectural standard. Each microprocessor-based design was sufficiently different from others that economies of design standardization could not be realized. The wide acceptance and cloning of the PC-platform changed all that; the core hardware design of each PC is virtually the same. Although each PC design today may use different specific ICs or levels of IC integration, the overall functionality is identical, with the same signal interface functions at the block diagram level.

A similar thing is happening around the signal-computing model. "Reference" designs—complete working schematics and block diagrams—are being made available as chips or sets of chips to provide a standard set of circuit functions. Engineers who use DSP, whether embedded in systems or available with PC-like flexibility, can choose the reference design that has the capabilities they need—and seek out those vendors whose components can implement the design most cost-effectively. Scalable architectures allow more-powerful DSPs (faster clock, more

memory) to be used as needed with minimum system-design disruption.

For signal computing, the hardware system consists of three low-cost blocks integrated as a "datapump" :the *DSP*, as the controller and central processor, the *analog input/output interface* to the signal source or sink (Examples include the public switched telephone network (PSTN), an audio source and its corresponding output, or a video source and its output), and the *signal processing algorithm* (usually downloaded and *resident in RAM).*

GENERALIZED SIGNAL COMPUTING HARDWARE BLOCK DIAGRAM

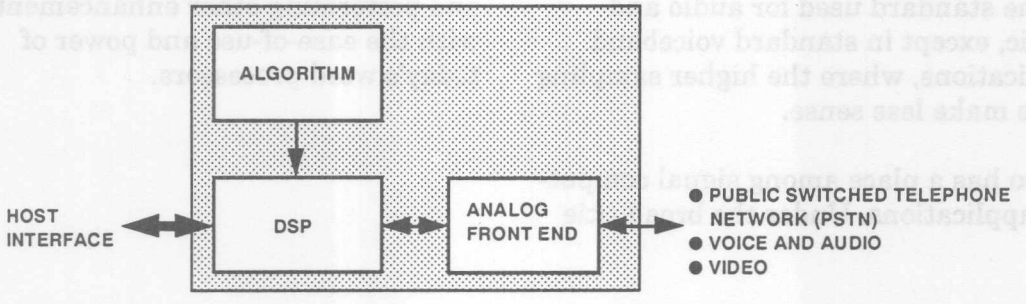


Figure 18.2

This datapump supports a host interface for PC-based applications. The DSP and analog front end are available as chipsets, specifically designed to work with each other and compatible with available algorithms. For embedded, dedicated applications the host interface is not needed, and the algorithm is in ROM.

SOFTWARE: OPEN ARCHITECTURE THE KEY

At present, much DSP-related software is custom-fit to the application. This includes the application code itself, as well as the operating system (if any), and the "hooks" to the rest of the system. Libraries and library calls to these libraries are available, but they lack the high degree of standardization found in the PC world with well-defined BIOS and operating system, and related interfaces.

Fortunately, many of the software elements needed to encourage the growth of creative algorithms and software are now taking shape. The final structure is roughly analogous to the 7-layer OSI telecommunications model (Figure 18.3), which has worked very well at providing flexibility to users by assigning implementation responsibility in well defined blocks, while at the same time assuring transparency between layers. As a result, vendors can offer unique, innovative solutions within each layer—solutions that enhance performance or reduce cost of the total system, yet do not adversely affect the total system structure. While this process, when we discuss its details, may sound complicated, it does indeed model a working technology.

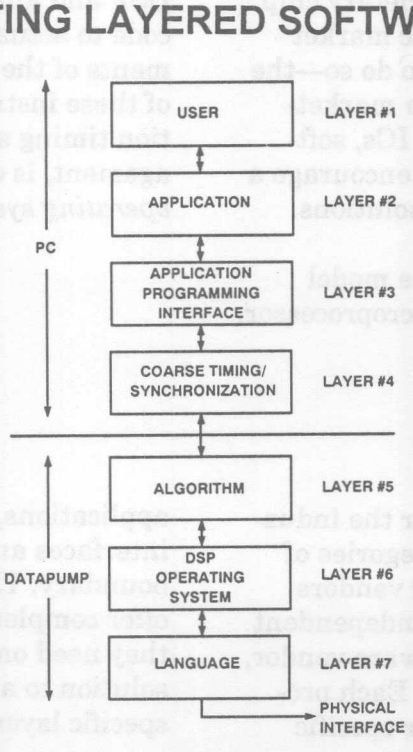


Figure 18.3

The key to this layer structure is its *open architecture*. Each interface between layers is well-defined and distinct. Individual algorithm vendors and complementary software vendors are free to offer their solutions in competition, to meet the challenges of the market and the application. Algorithm vendors provide algorithms to solve specific application needs, such as image compression, audio compression, or telecommunication interface. Software vendors convert these algorithms to code which actually implements these algorithms on specific DSP and chipset platforms.

The "best" hardware and software solution for a particular application is thus determined by the competitive market, since all vendors are free to offer their product on whatever sale or licensing terms they choose. Although DSP IC vendors offer proprietary chip solutions focused on specific market needs—and will continue to do so—the ferment in the open-system marketplace, involving vendors of ICs, software, and algorithms, will encourage a wider range of innovative solutions.

The upper four layers of the model reside in the PC and its microprocessor. At the top layer is the user interface, for example screen and keyboard. Immediately below is the application, which defines the broad needs of the user. The application program interface (API), layer #3, is where the broadly defined needs are translated into more-specific instructions and service requests. Layer #4 is the PC's operating system, which provides coarse timing, prioritization, synchronization, and scheduling among the various applications requesting service.

The lower three layers, #5 through 7, are implemented by the signal-computing DSP chipset and algorithm. For embedded, dedicated applications, are the only layers needed. The *algorithm* layer defines how the specific application needs will be implemented in real time. The lowest layer, *language*, provides the set of instructions for the DSP and analog front end as executable code to actually implement the requirements of the application. The execution of these instructions, with fine resolution timing and detailed resource management, is controlled by the *real-time operating system*.

WHAT IT ALL MEANS

What does all this mean for the industry? It means that new categories of DSP and signal-computing vendors emerge (Figure 18.4): the independent algorithm vendor, the software vendor, and the DSP O/S supplier. Each provides solutions designed for specific applications, using well-specified open interfaces and architectures at each boundary. The vendors do not have to offer complete solutions at all layers: they need only compete to provide a solution to a part of the problem—for a specific layer.

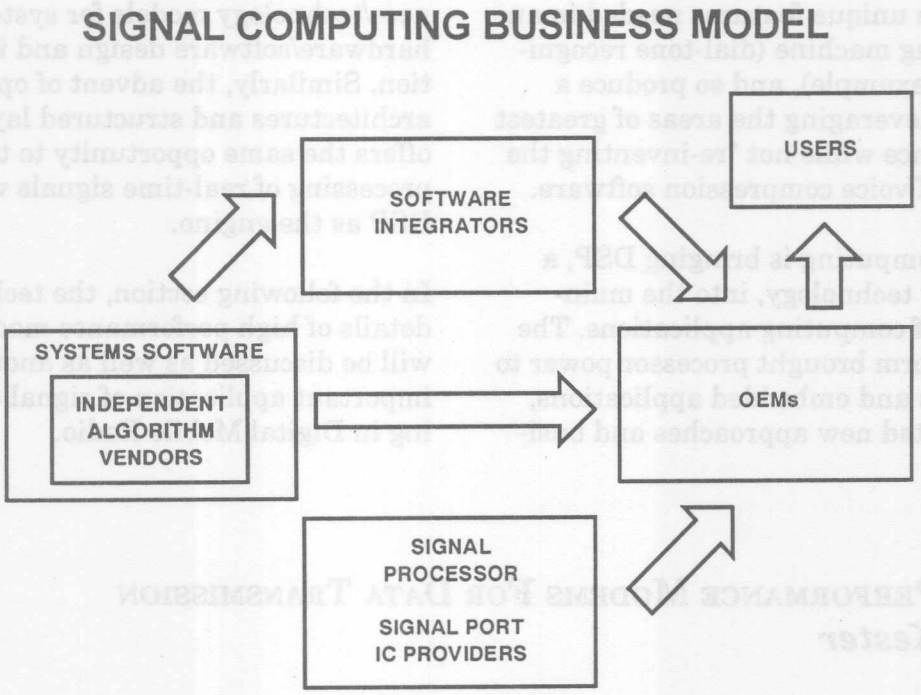


Figure 18.4

Since these independent vendors provide support for all the major DSP families used in signal computing, design engineers are not tied exclusively to one IC vendor. Small, innovative companies also have clear opportunities in the market, since they can leverage their efforts via the path provided by the well-defined layers and open architecture.

What does this mean for the design engineer who must assemble a complete system? In the future, he or she will choose among the various vendors to find a suitable chipset, along with appropriate operating system and algorithms. The project engineer's principal focus will be on system integration. For the many applications with industry-wide standards (for example, JPEG and MPEG image compression and telecommunications), algorithm vendors will offer a variety of solutions. For more-specialized, less-standard niche applications, where there may be only a handful of vendors (of not-totally suitable solutions for the specific problem), the design engineer may find it more cost-effective to develop the algorithm and code as part of the project.

Once the algorithm has been selected, the design engineer can choose between buying the code to implement it, or writing the code as part of the project. Again, the choice depends on the application and the number of vendors. For some applications—such as telecom or voice and image compression—"validated" (tested and verified) code will be available and preferable.

Here's an example: suppose a company that designs answering machines, with expertise in telephone-system line format and protocol, wants to develop a DSP-based, no-moving-part answering machine. The designer can buy suitable algorithms for voice compression, add to

these the unique features needed in an answering machine (dial-tone recognition, for example), and so produce a product leveraging the areas of greatest competence while not "re-inventing the wheel" of voice compression software.

Signal computing is bringing DSP, a specialty technology, into the mainstream of computing applications. The PC platform brought processor power to both PCs and embedded applications, and created new approaches and business/technology models for system hardware/software design and integration. Similarly, the advent of open architectures and structured layers offers the same opportunity to the processing of real-time signals with DSP as the engine.

In the following section, the technical details of high performance modems will be discussed as well as another important application of signal computing in Digital Mobile Radio.

HIGH PERFORMANCE MODEMS FOR DATA TRANSMISSION
Walt Kester

Modems (*Mo*dulator/*Demo*dulator) are widely used to transmit and receive digital data over analog channels, especially, but not exclusively over the Public Switched Telephone Network (PSTN). Although the data to be transmitted is digital, the telephone channel is designed to carry voice signals having a bandwidth of approximately 300 to 3300Hz. The telephone transmission channel suffers from delay distortion, noise, crosstalk, near-end and far-end echoes, and other imperfections listed in Figure 18.5. While certain levels of these signal degradations are perfectly acceptable for voice communication, they can cause high error rates in digital data transmission. The fundamental purpose of the transmitter portion of the modem is to prepare the digital data for transmission over the analog voice line. The purpose of the receiver portion of the modem is to receive the signal which contains the analog representation of the data , and reconstruct the original digital data with an acceptable error rate. High performance modems make use of digital computing techniques to perform such functions as modulation, demodulation, error detection and correction, equalization, and echo cancellation.

A block diagram of a telephone channel is shown in Figure 18.6. Most voiceband telephone connections involve several connections through the telephone network. The 2-wire subscriber line available at most sites is generally converted to a 4-wire signal at the telephone central office. The signal is converted back to a 2-wire signal at the far-end subscriber line. The 2- to 4-wire interface is implemented with a circuit called a *hybrid*. The hybrid intentionally inserts impedance mismatches to prevent oscillations on the 4-wire trunk line. The mismatch forces a portion of the transmitted signal to be reflected or echoed back to the transmitter. This echo can corrupt data the transmitter receives from the far-end modem.

IMPERFECTIONS IN THE TELEPHONE CHANNEL

- Attenuation
- Bandwidth Flatness
- Harmonic Distortion
- Echoes (Near-End and Far-End)
- Phase Jitter
- Phase Distortion, Group Delay Variation
- Noise
- Impedance Mismatches
- Frequency Offset
- Phase and Gain Hits

Figure 18.5

TELEPHONE CHANNEL BLOCK DIAGRAM

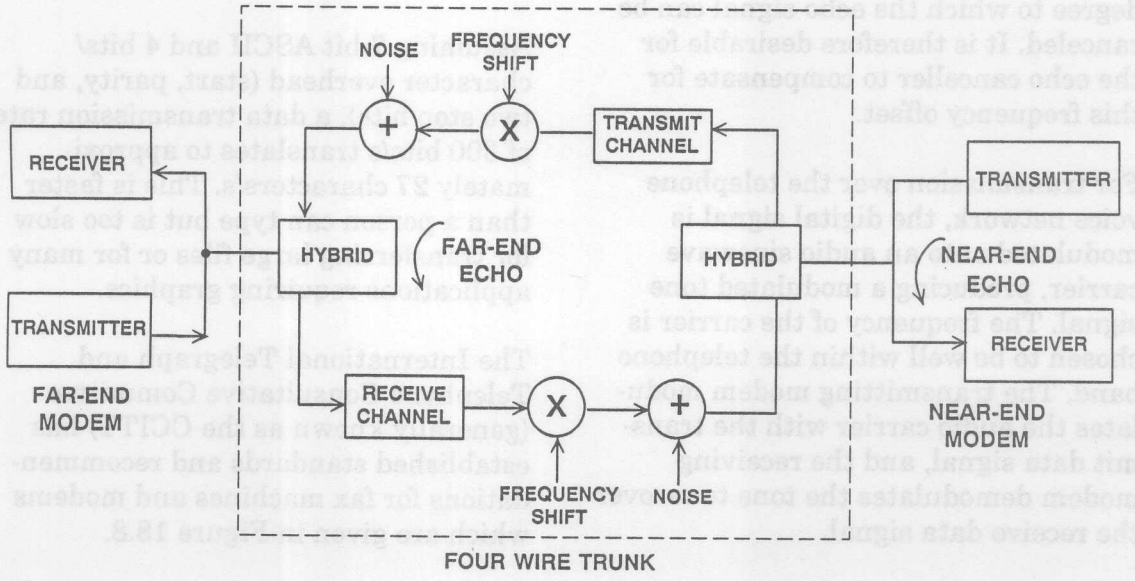


Figure 18.6

Half-duplex modems are capable of passing signals in either direction on a 2-wire line, but not simultaneously. *Full-duplex* modems operate on a 2-wire line and can transmit and receive data simultaneously. Full-duplex operation requires the ability to separate a receive signal from the reflection (echo) of the transmitted signal. This is accomplished by assigning the signals in the two directions different frequency bands separated by filtering, or by echo canceling in which a locally synthesized replica of the reflected transmitted signal is subtracted from the composite receive signal.

There are two types of echo in a typical voiceband telephone connection. The first echo is the reflection from the near-end hybrid, and the second echo is from the far-end hybrid. In long distance telephone transmissions, the transmitted signal is heterodyned to and from a carrier frequency. Since local oscillators in the network are not exactly matched, the carrier frequency of the far-end echo may be offset from the frequency of the transmitted carrier signal. In modern applications this shift can affect the degree to which the echo signal can be canceled. It is therefore desirable for the echo canceller to compensate for this frequency offset.

For transmission over the telephone voice network, the digital signal is modulated onto an audio sinewave carrier, producing a modulated tone signal. The frequency of the carrier is chosen to be well within the telephone band. The transmitting modem modulates the audio carrier with the transmit data signal, and the receiving modem demodulates the tone to recover the receive data signal.

The baseband data signal may be used to modulate the amplitude, the frequency, or the phase of the audio carrier, depending on the data rate required. These three types of modulation are known as amplitude shift keying (ASK), frequency shift keying (FSK), and phase shift keying (PSK). In its simplest form the modulated carrier takes on one of two states - that is, one of two amplitudes, one of two frequencies, or one of two phases. The two states represent a logic 0 or a logic 1.

Low- to medium-speed data links usually use FSK up to 1200 bits/s. Multiphase PSK are used for 2400 bits/s and 4800 bits/s links. PSK utilizes bandwidth more efficiently than FSK but is more costly to implement. ASK is least efficient and is used only for very low speed links (less than 100 bits/s) For 9600 bits/s, a combination of PSK and ASK is used, known as Quadrature Amplitude Modulation (QAM). Better performance at 9600 bits/s can be achieved using Trellis Code Modulation (TCM). For 14400 bits/s, Trellis Code Modulation (TCM) is essential.

Assuming 7-bit ASCII and 4 bits/character overhead (start, parity, and two stop bits), a data transmission rate of 300 bits/s translates to approximately 27 characters/s. This is faster than a person can type but is too slow for transferring large files or for many applications requiring graphics.

The International Telegraph and Telephone Consultative Committee (generally known as the CCITT) has established standards and recommendations for fax machines and modems which are given in Figure 18.8.

MODULATION METHODS FOR MODEMS

- Amplitude Shift Keying (ASK): Up to 100 bits/s
- Frequency Shift Keying (FSK): Up to 1200 bits/s
- Phase Shift Keying (PSK) and Differential Phase Shift Keying (DPSK): Up to 4800 bits/s
- Quadrature Amplitude Modulation (QAM): Up to 9600 bits/s
- Trellis Code Modulation (TCM): Up to 14400 bits/s

Figure 18.7

CCITT MODEM AND FAX STANDARDS

CCITT Standard	Speed (bits/s)	Half Duplex/ Full Duplex/ Echo Cancellation	Modulation Method
V.17 (FAX)	14400	Half Duplex	TCM
V.21	300	Full Duplex	FSK
V.22	1200	Full Duplex	DPSK
V.22bis	2400	Full Duplex	QAM
V.23	1200/75rev	Half Duplex	FSK
V.24	RS-232 Serial Connection		
V.27ter (FAX)	4800	Half Duplex	DPSK
V.29 (FAX)	9600	Half Duplex	QAM
V.32	9600	Full Duplex (EC)	QAM
V.32bis	14400	Full Duplex (EC)	TCM

Figure 18.8

V.32 Modem Overview

The goal in designing high performance modems is to achieve the highest data transfer rate possible over the channel used (normally the PSTN) and avoid the expense of using dedicated conditioned private telephone lines. The V.32 recommendation describes a full-duplex (simultaneous transmission and reception) synchronous modem that operates on the Public Switched Telephone Network (PSTN). The V.32 modem communicates at a rate of 9600 bits/s and may utilize either quadrature amplitude modulation (QAM) or Trellis Code Modulation (TCM). Higher performance (lower bit-error-rates) may be achieved using TCM. In TCM, four-bit symbols (bauds) modulate a carrier frequency of 1800Hz with a modulation rate of 2400 bauds/s. The modulation of 4-bit symbols at a rate of 2400 symbols/s yields the 9600 bits/s specification. These 4-bit symbols are transmitted using 32-state trellis-encoded QAM. The trellis encoding provides an extra bit per symbol for forward error correction. This additional bit dramatically increases the noise performance of the modem. Characteristics of V.32 and V.32bis modems are summarized in Figure 18.9.

V.32 / V.32bis MODEM CHARACTERISTICS

- 9600 bits/second Bit Rate on PSTN (V.32)
- 14400 bits/second Bit Rate on PSTN (V.32bis)
- 1800Hz Carrier Frequency (Transmit and Receive)
- 4 Bits/Symbol, 2400Hz Symbol Rate
- 32-QAM, Trellis Coded, 4 Bit Data + Redundancy Bit
- Transmit/Receive Isolation Using Echo Cancellation
- Extensive Use of DSP Techniques

Figure 18.9

A simplified block diagram for a V.32 modem is shown in Figure 18.10. The diagram shows that the bulk of the signal processing is done digitally. Both the transmit and receive portions of the modem subject the digital signals to a number of DSP algorithms which can be run efficiently on modern processors.

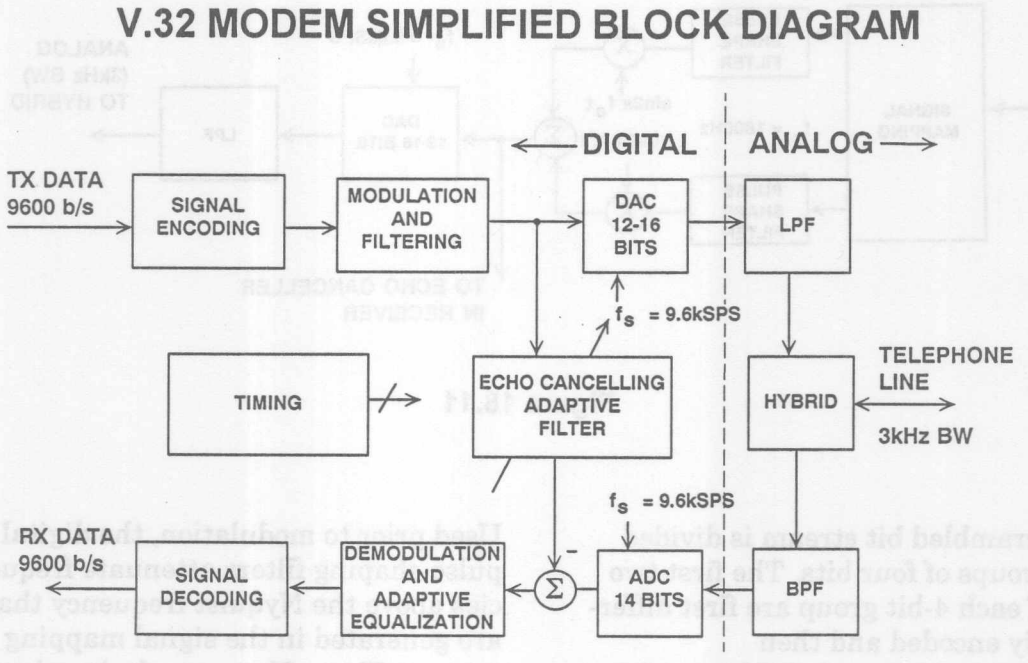


Figure 18.10

V.32 Modem Transmitter

A block diagram of the V.32 transmitter is shown in Figure 18.11. The input serial bit stream is first scrambled. Scrambling takes the input bit stream and produces a pseudo-random sequence. The purpose of the scrambler is to whiten the spectrum of the transmitted data. Without the scrambler, a long series of identical symbols could cause the receiver to lose carrier lock. Scrambling makes the transmitted spectrum resemble white noise, to utilize the bandwidth of the channel more efficiently, makes carrier recovery and timing synchronization easy, and makes adaptive equalization and echo cancellation possible.

V.32 MODEM TRANSMITTER

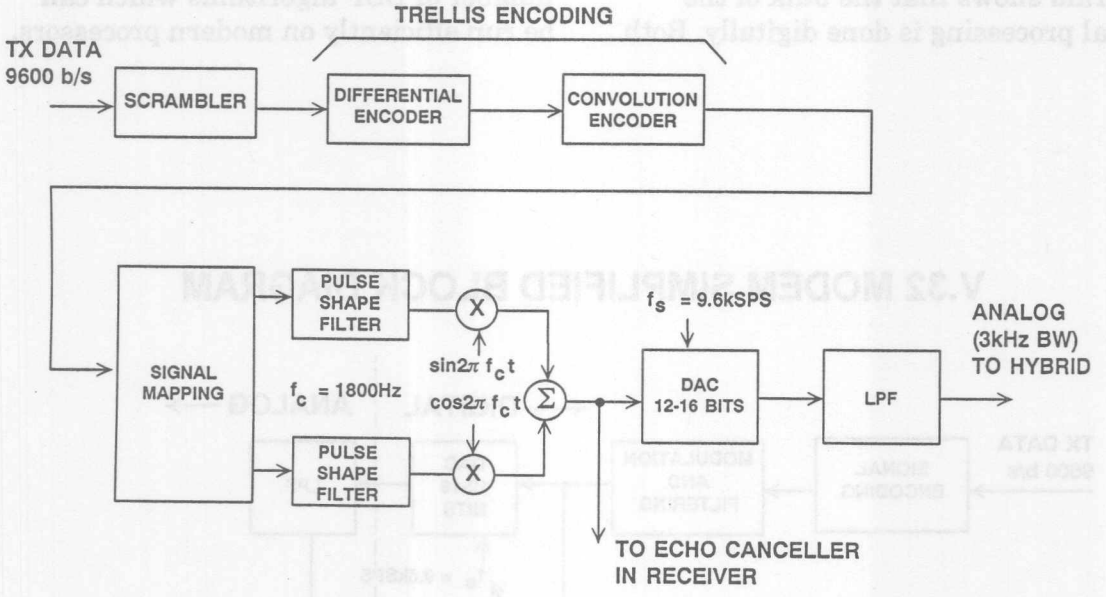


Figure 18.11

The scrambled bit stream is divided into groups of four bits. The first two bits of each 4-bit group are first differentially encoded and then convolutionally encoded. This produces a 5-bit trellis-coded symbol in which the extra bit is a redundantly coded bit.

The 5-bit symbols are then mapped into the signal space using trellis-coding as defined in the V.32 recommendation. The signal space mapping produces two coordinates, one for the real part of the QAM modulator and one for the imaginary part. A diagram of the resulting V.32 signal constellation is shown in Figure 18.12.

Used prior to modulation, the digital pulse shaping filters attenuate frequencies above the Nyquist frequency that are generated in the signal mapping process. These filters are designed to have zero crossings at the appropriate frequencies to cancel intersymbol interference. The pulse shape filter is based on the impulse response of a raised cosine function as shown in Figure 18.13. The value T is equal to the reciprocal of the symbol rate (2400 symbols/second). For a sampling rate of 9600Hz and a symbol rate of 2400Hz, a 17-tap FIR filter can be used.

V.32 MODEM SIGNAL CONSTELLATION

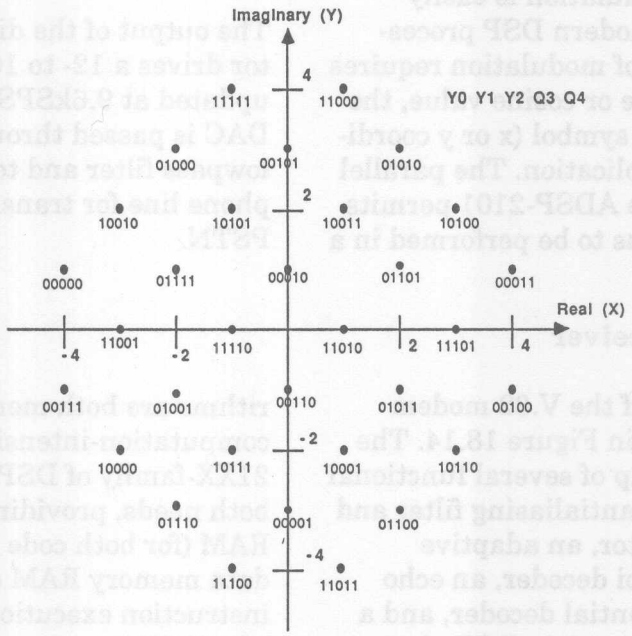


Figure 18.12

PULSE SHAPING FILTER IMPULSE RESPONSE

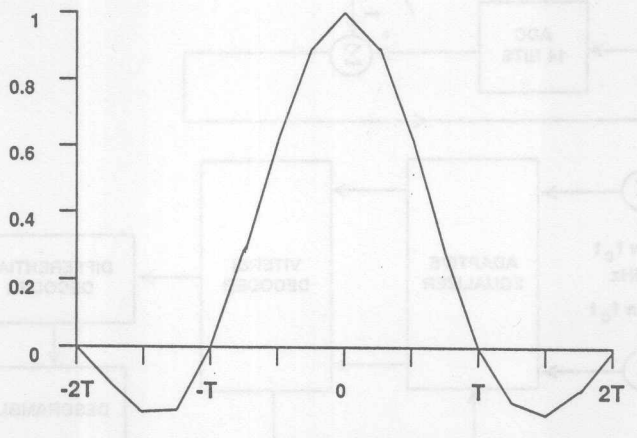


Figure 18.13

The modulation for the V.32 coding scheme is quadrature amplitude modulation (QAM). Modulation is easily implemented in modern DSP processors. The process of modulation requires the access of a sine or cosine value, the access of an input symbol (x or y coordinate) and a multiplication. The parallel architecture of the ADSP-2101 permits all three operations to be performed in a single 80ns cycle (60ns for the ADSP-2116).

The output of the digital QAM modulator drives a 12- to 16-bit DAC which is updated at 9.6kSPS . The output of the DAC is passed through a 3.5kHz analog lowpass filter and to the 2-wire telephone line for transmission over the PSTN.

V.32 Modem Receiver

A block diagram of the V.32 modem receiver is shown in Figure 18.14. The receiver is made up of several functional blocks: the input antialiasing filter and ADC, a demodulator, an adaptive equalizer, a Viterbi decoder, an echo canceller, a differential decoder, and a descrambler. The receiver DSP algorithms are both memory-intensive and computation-intensive. The ADSP-21XX-family of DSP processors address both needs, providing program memory RAM (for both code and data) on chip, data memory RAM on chip, and an instruction execution rate of up to 16.67MIPS.

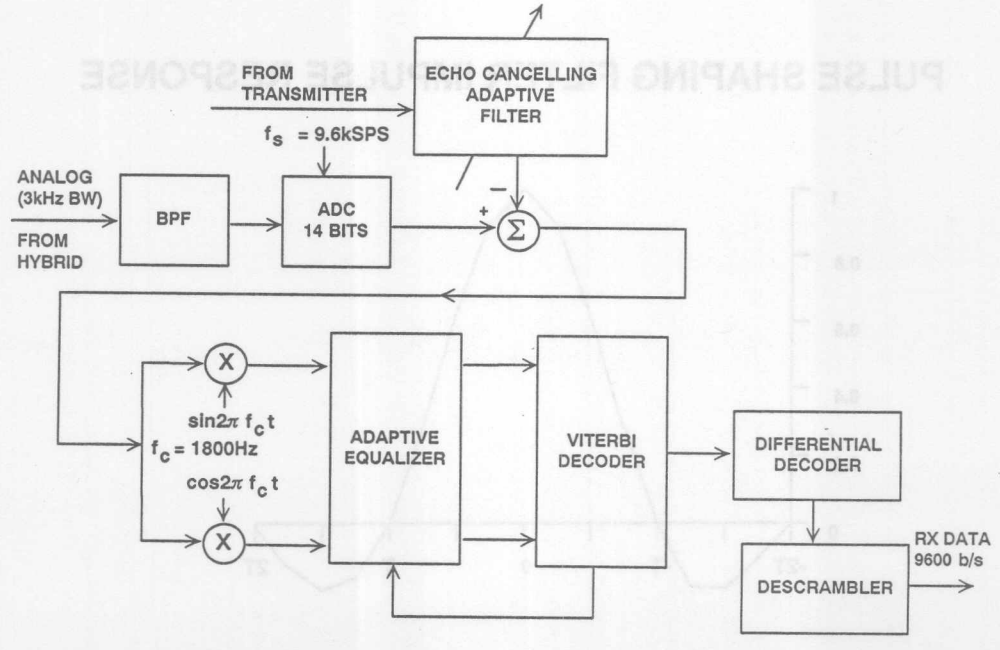


Figure 18.14

The antialiasing filter and ADC in the receiver need to have a dynamic range from the largest echo signal to the smallest received signal. The received signal can be as low as –40dBm, while the near-end echo can be as high as –6dBm. In order to insure that the analog front end of the receiver does not contribute any significant impairment to the channel under these conditions, an instantaneous dynamic range of 80dB (14 bits) and an SNR of 72dB is required.

In order to compensate for amplitude and phase distortion in the telephone channel, equalization is required to recover the transmitted data at an acceptably low bit error rate. In order to respond to rapidly changing conditions on the telephone line, adaptive equalization is required for the V.32 modem receiver. An adaptive equalizer can be implemented digitally in an FIR filter whose coefficients are continuously updated based on current line conditions. A 64-tap fractionally spaced equalizer provides the performance necessary for V.32 applications.

Separation between the transmit and receive signal in the V.32 modem is accomplished using echo cancellation. Echo cancellation is mandatory since both the calling and the answering modem use the same carrier frequency of 1800Hz. Both near-end and far-end echo must be canceled in order to yield reliable communication. Echo cancellation is achieved by subtracting an estimate of the echo return signal from the actual received signal. The predicted echo is determined by feeding the transmitted signal into an adaptive filter with a transfer function that approximates the telephone channel. The adaptive filter commonly used in echo cancellers is the FIR filter (chosen for its stability and linear phase response), where the taps are determined using the least-mean-square (LMS) algorithm during a training sequence executed prior to full-duplex communications. The echo canceller must be able to cancel 16ms of echo. At 9600 samples/second, a 154-tap FIR filter is required to cancel the echo. Assuming that the canceller and frequency shifter have converged during the training period, about 200 cycles are required to cancel an echo in a V.32 modem.

The most common technique for decoding the received data is Viterbi decoding. Named after its inventor, the Viterbi algorithm is a general-purpose technique for making an error-corrected decision. Viterbi decoding provides a certain degree of error correction by examining the received bit pattern over time to deduce the value that was the most likely to have been transmitted at a particular time. Viterbi decoding is computation-intensive. A history for each of the possible symbols sent at each symbol interval has to be maintained. For the V.32 modem, the symbol history spans 20 symbol intervals. At each symbol interval, the length of the path backward in time from each possible received symbol to a symbol sent some time ago is calculated. After 20 symbol intervals, the symbol that has the shortest path back to the original signal is chosen to be the current decoded symbol. A complete description of Viterbi decoding and its implementation on the ADSP-2100 family of DSP processors is given in Reference 2.

The AD28msp01 PSTN Signal Port for V.32 Modems

The AD28msp01 is a complete analog front end for high performance modems. The AD28msp01 contains a 16 bit sigma-delta ADC and DAC and is capable of sampling rates of 7.2, 8.0, and 9.6kSPS with SNR and THD performance of 84dB. The extensive support of bit, baud, and convert clocks allow the AD28msp01 to support many modem standards such as the V.32 and V.32bis. A block diagram is shown in Figure 18.15, and key specifications are summarized in Figure 18.16.

AD28msp01 PSTN SIGNAL PORT BLOCK DIAGRAM

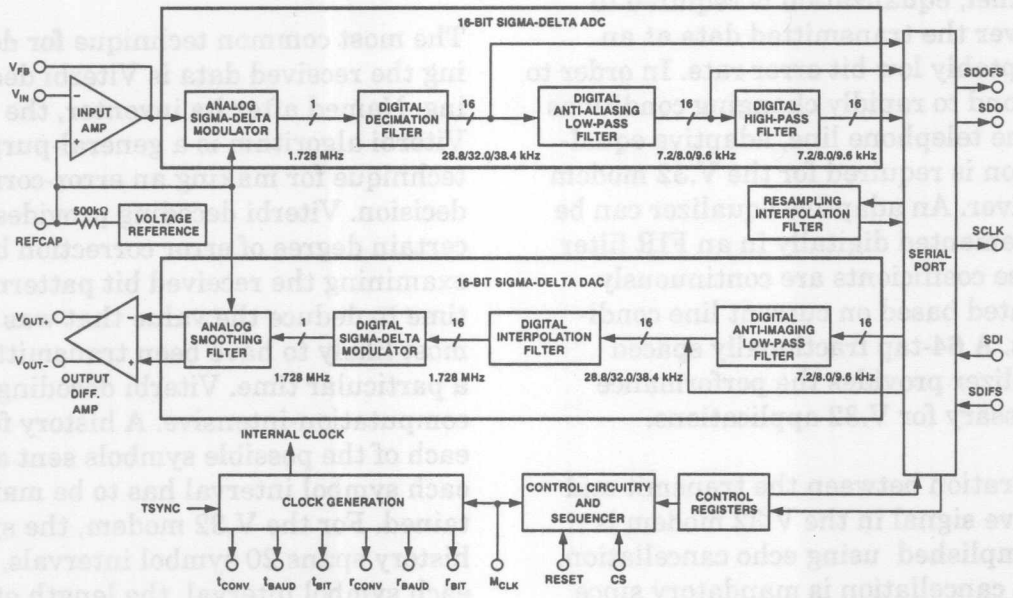


Figure 18.15

AD28msp01 INTEGRATED MODEM ANALOG FRONT END KEY SPECIFICATIONS

- 16 Bit Sigma-Delta ADC and DAC
- On-Chip Antialiasing and Anti-Imaging Filters
- On-Chip Clock Generation Circuitry
- 80 dB THD and SNR
- Programmable Sampling Frequency of 7.2, 8.0, and 9.6kSPS
- DSP Compatible Serial Port
- Single +5V Supply, 350mW Power Dissipation
- 28 Pin DIP/SOIC

Figure 18.16

The AD20msp500-Series Of Software Programmable PSTN Communications Chipsets And The ADAT-DSI01 DataPump Algorithm Toolkit

These two packages (Figure 18.17) form a good example of what Analog Devices' Signal Computing technology provides to solve a systems design problem. The chipsets are key building blocks for a variety of low-cost modems and "datapumps." They consist of the AD28msp01 analog signal port for PSTN (public switched telephone network), plus a member of Analog Devices' ADSP-2100 fixed-point DSP family.

SIGNAL COMPUTING SOLUTION FOR HIGH PERFORMANCE MODEMS

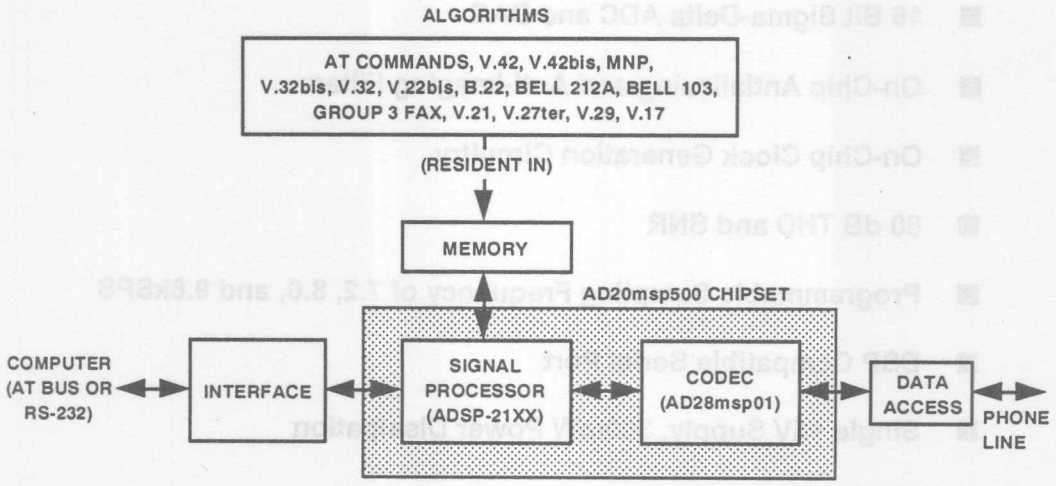


Figure 18.17

The AD28msp01 signal port (previously described) is designed specifically for echo-canceling V.32 and V.32bis modem designs, while the DSP processor provides processing power to implement algorithms for these standards—plus all fallback standards, and fax-, data-compression-, and error-correction functions. No microcontroller is used—all functionality is defined and implemented by software; thus the range of functions can be easily upgraded or stripped back (to meet the market needs of the system designer), and any repairs of software defects are easily made.

The toolkit, developed by Digicom Systems, Inc., provides all the software and documentation needed to implement the modem using the chipset. The algorithms can be used "as is" for a standard design—or augmented for applications where customized signal processing algorithms are needed. The toolkit provides the datapump algorithms (which represent telecom standards) as modules; and only the desired modules need be included in the final product.

The ADMK-100 Modem Chipset Development Kit is a design kit developed by Digicom Systems, Inc., and is available from Analog Devices. This kit contains all schematics, layout, parts list, DSP object code, and other software necessary to build a complete low-cost modem using the AD20msp500-series of chipsets. A sample modem is also included in the kit.

ADMK-100 MODEM MANUFACTURING KIT

- AD20msp500-Series Modem Chipset
- Parts List, Schematics, PC Board Layout
- DSP Object Code, License Agreement
- Sample Stand-Alone Modem

Figure 18.18

Digital Telephone Answering Machine Solution Using Signal Computing From Analog Devices

The ADDS-CSDK-100 is a Manufacturing Kit for the design of digital telephone answering machines. The kit provides an answering machine development tool program, a demonstration board, and complete production information (gerber files, schematics, and user's guide). The development tool software allows developers to prototype their digital answering machine. The tool outputs an EPROM file that contains the DSP object code to run the answering machine. The EPROM is coded to run on the AD20msp700 (ADSP-21XX compatible) DSP. Key features of the answering machine manufacturing kit are summarized in Figure 18.19.

ADDS-CSDK-100 DIGITAL TELEPHONE ANSWERING MACHINE DESIGN KIT

- Complete Set of Hardware and Software Tools for Development of Compressed-Speech Digital Answering Machine Including Demo Board
- High Quality Speech Coding Algorithms based on RPE-LTP-LPC Coding
- Supports DTMF, Busy Tone, and Ring Detection
- Synthetic Voice Announces Time Stamp and DTMF Phone Number
- Functions: Record, Play, Delete, Memo, Cue, Review, Skip, Save, Remote
- 5 to 50 Minutes of Voice Recording Using 4 to 16Mbit DRAM or ARAM
- Voice Activity Detection for Pause Compression to Optimize Memory Usage
- Minimal Glue Logic, No ASIC Required

Figure 18.19

DIGITAL MOBILE RADIO OVERVIEW

Walt Kester

The rapidly growing number of cellular mobile phones in the United States has created significant system performance problems, especially in crowded metropolitan areas such as New York and Los Angeles. Call blocking during rush hour, flaws in call processing (disconnects and misconnects), and undesirable interchannel crosstalk are only a few. In addition, the current system lacks privacy and security, and data transmission over a mobile link is almost impossible at rates above 1200 bits/s. These factors have led to the search for a more efficient and robust system based on digital techniques. Several digital approaches are being considered in the United States, while the Pan-European Digital Cellular Radio System (also known as *Groupe Speciale Mobile*, or GSM) is already in use throughout Europe and much of the rest of the world.

The current system in the United States is a cellular system based on Frequency Division Multiple Access (FDMA). A region is broken up into cells, with each cell having its own base station and its own group of assigned frequencies (see Figure 18.21). Because the radius of each cell is small (10 miles, for example) low power transmitters and receivers can be used. The cellular system lends itself to frequency reuse, since cells which are far enough apart can utilize the same band of frequencies without interference. The base stations must be linked together with an elaborate central control network so that a call may be handed-off to another cell when the signal strength from the mobile unit becomes too low for the current cell to handle.

PROBLEMS WITH CURRENT ANALOG CELLULAR RADIO

- Call Blocking During Busy Hours
- Misconnects and Disconnects due to Rapidly Fading Signals
- Lack of Privacy and Security
- Data Transmission Limited to 1200 bits/s

Figure 18.20

CELLULAR RADIO FREQUENCY REUSE

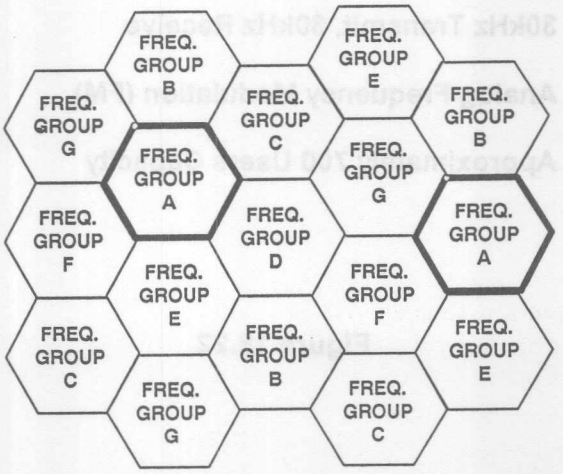


Figure 18.21

The frequency spectrum allocation for cellular radio in the United States is approximately 825 to 850MHz and 870 to 895MHz. Conventional architectures (both analog and digital) are channelized. The total spectrum is divided up into a large number of relatively narrow channels, defined by a carrier frequency. The carrier frequency is frequency-modulated with the voice signal using analog techniques. Each full-duplex channel requires a pair of frequencies, each with a bandwidth of approximately 30kHz. A user is assigned both frequencies for the duration of the call. The forward and reverse channel are widely separated, to help the radio keep the transmit and receive functions separated. The 40MHz allocated to cellular service can therefore be divided up into 666 frequency pairs, each serving one full-duplex circuit.

U.S. FREQUENCY DIVISION MULTIPLE ACCESS (FDMA) ANALOG MOBILE RADIO SYSTEM

- Uses 825-850MHz and 870-895MHz Spectrum
- 30kHz Transmit, 30kHz Receive
- Analog Frequency Modulation (FM)
- Approximately 700 Users Capacity

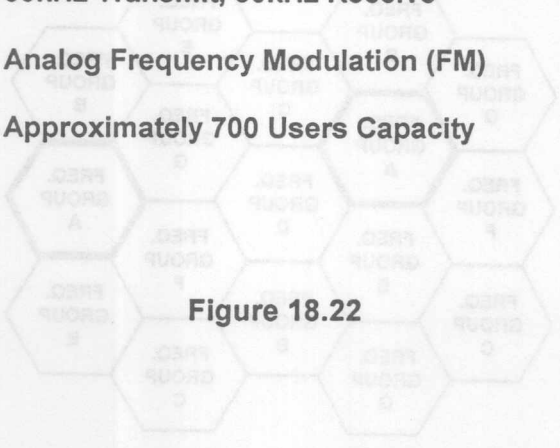


Figure 18.22

Time Division Multiple Access (TDMA) allocates bandwidth on a time-slot basis. In the proposed United States TDMA system, the entire 30kHz channel is assigned to a particular transmission, but only for a short period of time. A 3:1 multiplexing scheme means that three conversations can take place with TDMA using the same amount of bandwidth as one analog cellular conversation does. Each transmit/receive sequence occurs on time slots lasting 6.7ms. The TDMA system relies on an extensive amount of DSP technology to reduce the coded speech bit-rate as well as to prepare the digital data for transmission over the analog medium. The TDMA approach has been chosen for the Pan-European GSM system and will be discussed later in more detail.

The second digital approach being considered in the United States is called Code Division Multiple Access (CDMA). This technique has been used in secure military communications for a number of years under the name of *spread spectrum*. In spread spectrum, the transmitter transmits in a pseudo-random sequence of frequency hops over a relatively wide frequency range. The receiver has access to the same random sequence and can decode the transmission. The effect of adding additional users on the system is to decrease the overall signal to noise ratio for all the users. With this technique, the effect of allowing more calls than the normal capacity is to increase the bit-error rate for all users. New callers can keep coming in, interference levels will rise gradually, until at some point the process will become self-regulating: the quality of the voice link will become so bad that users will cut short or refrain from making additional calls. No one is ever blocked in the conventional sense, as they are in FDMA or TDMA systems when all channels or slots are full.

DIGITAL MOBILE RADIO APPROACHES

- **Time Division Multiple Access (TDMA) - User Allocation Based on Time Slots: At Least 3X More Capacity than FDMA**
- **Code Division Multiple Access (CDMA) - Base on Spread Spectrum Technology: More Users Cause Graceful Degradation in Bit-Error Rate**
- **Both TDMA and CDMA Make Extensive Use of DSP in Speech Encoding and Channel Coding for Transmission**

Figure 18.23

Both TDMA and CDMA systems make extensive use of DSP algorithms in both speech encoding and in preparing the signal for transmission. In the receiver, DSP techniques are used for demodulation and decoding the speech signal. The remainder of this section will concentrate on speech processing and channel coding as they relate to the Pan-European GSM system. This will serve to illustrate the fundamental principles which are applicable to all digital mobile radio systems.

The GSM System

Figure 18.24 shows a simplified block diagram of the GSM Pan-European Digital Cellular Telephone System. The *speech encoder and decoder* and *discontinuous transmission* function will be described in detail. Up conversion and downconversion portions of the system contain a digital modem similar to the V.32 device previously discussed. Similar modem functions are performed digitally in the GSM system such as equalization, convolutional coding, Viterbi decoding, modulation and demodulation.

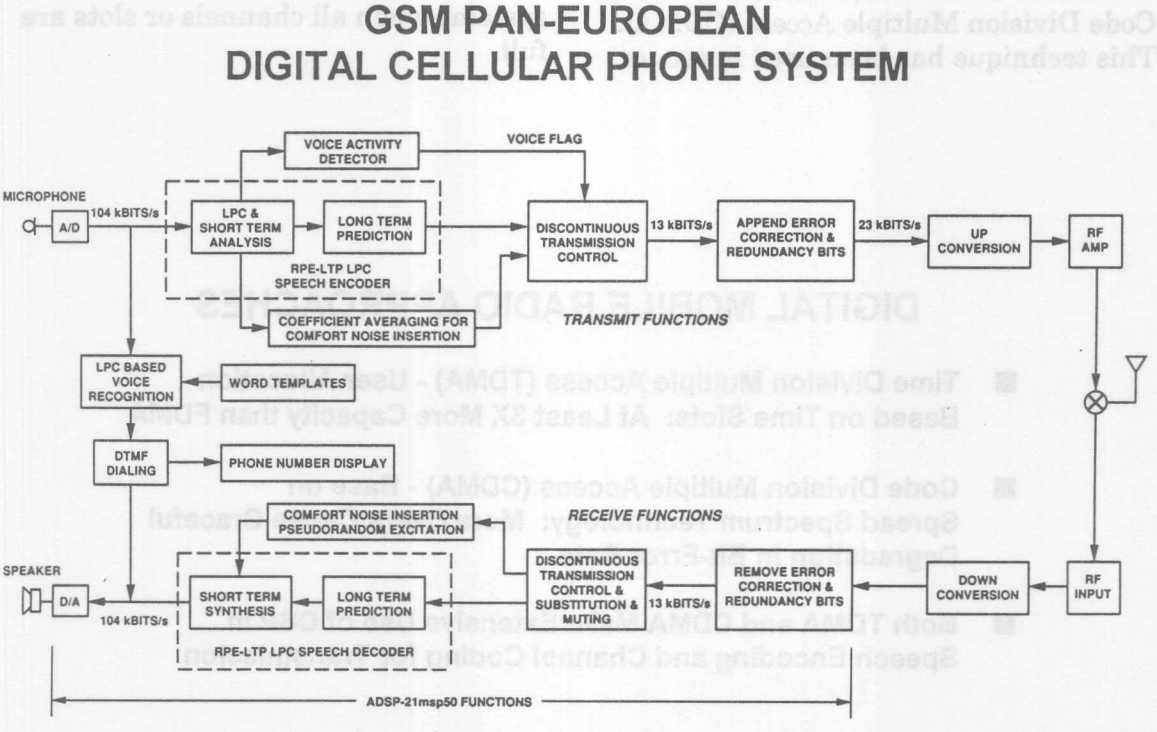


Figure 18.24

Speech Codec

The standard for encoding voice has been set in the T-Carrier digital transmission system. In this system, speech is logarithmically encoded to 8 bits at a sampling rate of 8kSPS. The logarithmic encoding and decoding to 8 bits is equivalent to linear encoding and decoding to 13 bits of resolution. In the GSM system 13-bit linear, 8kSPS encoding produces a bit-rate of 104kb/s. The Speech Encoder portion of the GSM system compresses the speech signal to 13kb/s, and the decoder expands the compressed signal at the receiver. The terms *codec* and *transcoder* are both often used to refer to the entire encoding and decoding speech compression function. The speech encoder is based on an enhanced version of linear predictive coding (LPC). The LPC algorithm uses a model of the human vocal tract that represents the throat as a series of concentric cylinders of various diameters. An excitation (breath) is forced into the cylinders. This model can be mathematically represented by a series of simultaneous equations which describe the cylinders.

The excitation signal is passed through the cylinders, producing an output signal. In the human body, the excitation signal is air moving over the vocal cords or through a constriction in the vocal tract. In a digital system, the excitation signal is a series of pulses for vocal excitation, or noise for a constriction. The signal is input to a digital lattice filter. Each filter coefficient represents the size of a cylinder.

An LPC system is characterized by the number of cylinders used in the model. The GSM system uses eight cylinders so eight reflection coefficients are required.

Early LPC systems worked well enough so the encoded speech could be understood, but often the quality was too poor to recognize the voice of the speaker. The GSM LPC system employs two advanced techniques that improve the quality of the encoded speech. These techniques are *regular pulse excitation* (RPE) and *long term prediction* (LTP). When these techniques are used, the resulting quality of encoded speech is nearly equal to that of logarithmic pulse code modulation (companded PCM as in the T-Carrier system).

The actual input to the speech encoder is a series of 13-bit samples of uniform PCM speech data. The sampling rate is 8kHz. The speech encoder operates on a 20ms window (160 samples) and reduces it to 76 coefficients (260 bits total), resulting in an encoded data rate of 13kb/s.

SPEECH COMPRESSION IN THE GSM SYSTEM

- **Input Data: 13bit Samples at 8kSPS = *104kbits/s***
- **Output Data for Each 20ms Window: 76 Filter Coefficients, 260 bits Total = *13kbits/s***

Figure 18.25

Discontinuous Transmission (DTX)

Discontinuous transmission (DTX) allows the system to shut off transmission during the pauses between words. This reduces transmitter power consumption and increases the overall GSM system's capacity.

Low power consumption prolongs battery live in the mobile station and is an important consideration for handheld portable phones. Call capacity is increased by reducing the interference between channels, leading to better spectral efficiency. In a typical conversation each speaker talks for less than 40% of the time, and it has been estimated that DTX can approximately double the call capacity of the radio system.

The required DTX functions are summarized in Figure 18.26.

The voice activity detector (VAD) is located at the transmitter; its job is to distinguish between speech superimposed on the background noise and noise with no speech present. The input to the voice activity detector is a set of parameters computed by the speech encoder. The VAD uses this information to decide whether or not each 20ms frame of the encoder contains speech.

DISCONTINUOUS TRANSMISSION (DTX) FUNCTIONS

- Voice Activity Detection (VAD) to Detect Speech
- Comfort Noise Insertion (CNI) to Synthesize Artificial Car Noise During Pauses Between Words
- Output Muting When Lost Speech Frames Are Received

Figure 18.26

Comfort noise insertion (CNI) is performed at the receiver. The comfort noise is generated when the DTX has switched off the transmitter; it is similar in amplitude and spectrum to the background noise at the transmitter. The purpose of the CNI is to eliminate the unpleasant effect of switching between speech with noise, and silence. If you were listening to a transmission without CNI, you would hear rapid alternating between speech in a high-noise background (i.e. in a car), and silence. This effect greatly reduces the intelligibility of the conversation.

When DTX is in operation, each burst of speech is transmitted followed by a *silence descriptor* (SID) frame before the transmission is switched off. The SID serves as an end of speech marker for the receive side. It contains characteristic parameters of the background noise at the transmitter, such as spectrum information derived through the use of linear predictive coding.

The SID frame is used by the receiver's comfort noise generator to obtain a digital filter which, when excited by pseudo-random noise, will produce noise similar to the background noise at the transmitter. This comfort noise is inserted into the gaps between received speech bursts. The comfort noise characteristics are updated at regular intervals by the transmission of SID frames during speech pauses.

Redundant bits are then added by the processor for error detection and correction at the receiver, increasing the final encoded bit rate to 22.8kb/s. The bits within one window, and their redundant bits, are interleaved and spread across several windows for robustness.

The ADSP-21msp50 Mixed Signal Processor shown in Figure 18.27 can perform all of the above tasks within the 20ms sampling window because of its optimized DSP architecture and the special on-chip peripherals associated with it. The sigma-delta converters provide the necessary interface to the speaker and microphone. The parallel host interface port communicates with a host processor, which is responsible for loading the ADSP-21msp50 with the appropriate programs during power-up, dialing, and actual conversation phases of a complete call. The ADSP-21msp50 has 1K words of (16-bit) data memory static RAM and 2K words of 24-bit program memory static RAM on chip. The device operates at a 13MHz clock rate and has a low power mode and a power down mode (less than 1mW in power down). The ADSP-21msp50 combines the core ADSP-2100 architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a programmable timer, host interface port, an analog interface (shown in Figure 18.28), and extensive interrupt capabilities. Key features of the ADSP-21msp50 are summarized in Figure 18.29, and the benchmark performance in the GSM system is shown in Figure 18.30.

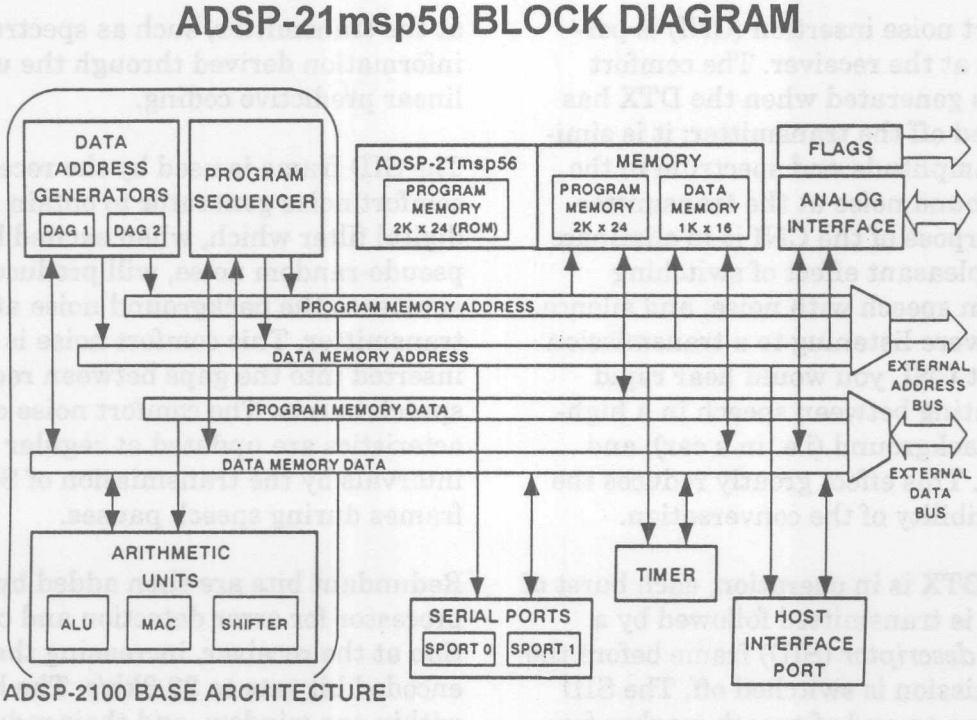


Figure 18.27

ADSP-21msp50 ANALOG INPUT/OUTPUT INTERFACE

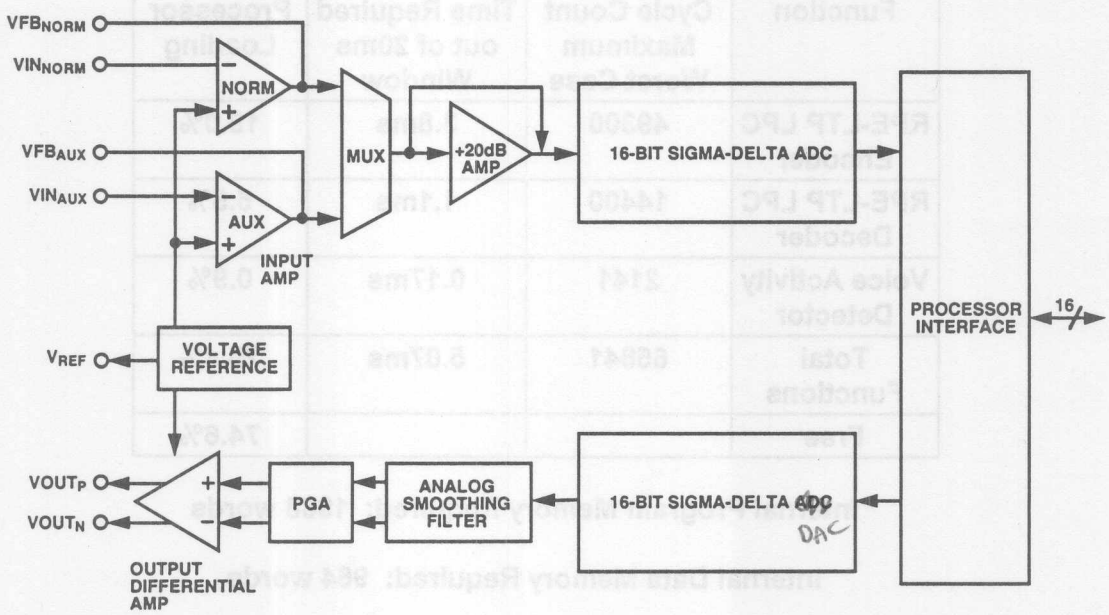


Figure 18.28

ADSP-21msp50 MIXED SIGNAL PROCESSOR KEY SPECS

- On-Chip 16-Bit Sigma-Delta ADC and DAC
- 65dB SNR and THD
- 8kSPS Sampling Frequency, 1MHz Clock (125X Oversampling)
- 2K Words Program Memory Ram (24-bits)
- 1K Words Data Memory Ram (16-bits)
- 13MIPS Performance
- Host Interface Port
- ADSP-2100 Family Compatible Instruction Set
- Low Power and Power Down Mode

Figure 18.29

ADSP-21msp50 GSM BENCHMARKS

Function	Cycle Count Maximum Worst Case	Time Required out of 20ms Window	Processor Loading
RPE-LTP LPC Encoder	49300	3.8ms	19.0%
RPE-LTP LPC Decoder	14400	1.1ms	5.5%
Voice Activity Detector	2141	0.17ms	0.9%
Total Functions	65841	5.07ms	25.4%
Free			74.6%

Internal Program Memory Required: 1988 words

Internal Data Memory Required: 964 words

Figure 18.30

The AD28msp02 Voiceband Signal Port is a complete I/O function for voiceband applications and requires an external DSP processor. A block diagram is shown in Figure 18.31, and key specifications in Figure 18.32.

AD28msp02 VOICEBAND SIGNAL INPUT / OUTPUT PORT

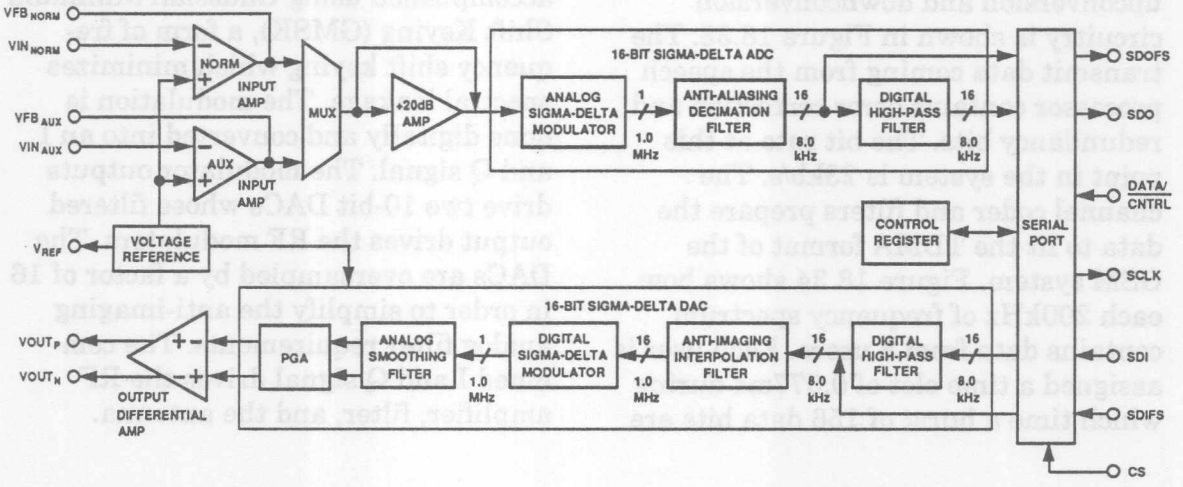


Figure 18.31

KEY FEATURES OF THE AD28msp02 VOICEBAND SIGMA-DELTA CODEC

- 16 bit Sigma-Delta ADC
- 16 bit Sigma-Delta DAC
- On-Chip Antialiasing and Smoothing Filters
- 8kSPS Sampling Rate, 128x Oversampling Ratio
- On-Chip Voltage Reference
- 65dB SNR and THD
- Easy Interface to DSP Chips
- 24-pin DIP/SOIC Package
- Single +5V Supply, 100mW Power Dissipation
- Ideal for Voiceband Applications

Figure 18.32

GSM System Upconversion and Downconversion

A block diagram of the GSM system with particular emphasis on the upconversion and downconversion circuitry is shown in Figure 18.33. The transmit data coming from the speech processor contains error correction and redundancy bits. The bit rate at this point in the system is 23kb/s. The channel coder and filters prepare the data to fit the TDMA format of the GSM system. Figure 18.34 shows how each 200kHz of frequency spectrum contains data from 8 users. Each user is assigned a time slot of 0.577ms during which time a burst of 156 data bits are transmitted at a modulation frequency of approximately 270kHz. Modulation is accomplished using Gaussian Minimum Shift Keying (GMSK), a form of frequency shift keying which minimizes spectral leakage. The modulation is done digitally and converted into an I and Q signal. The modulator outputs drive two 10-bit DACs whose filtered output drives the RF modulators. The DACs are oversampled by a factor of 16 in order to simplify the anti-imaging analog filter requirements. The combined I and Q signal drives the RF amplifier, filter, and the antenna.

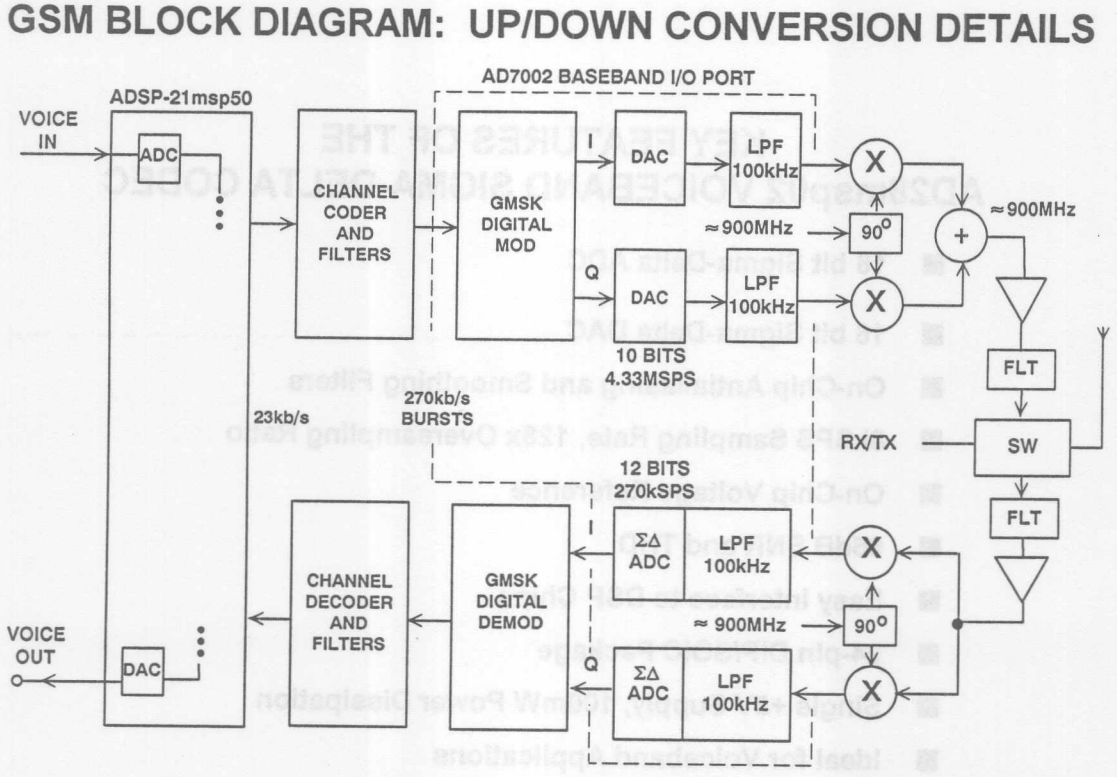


Figure 18.33

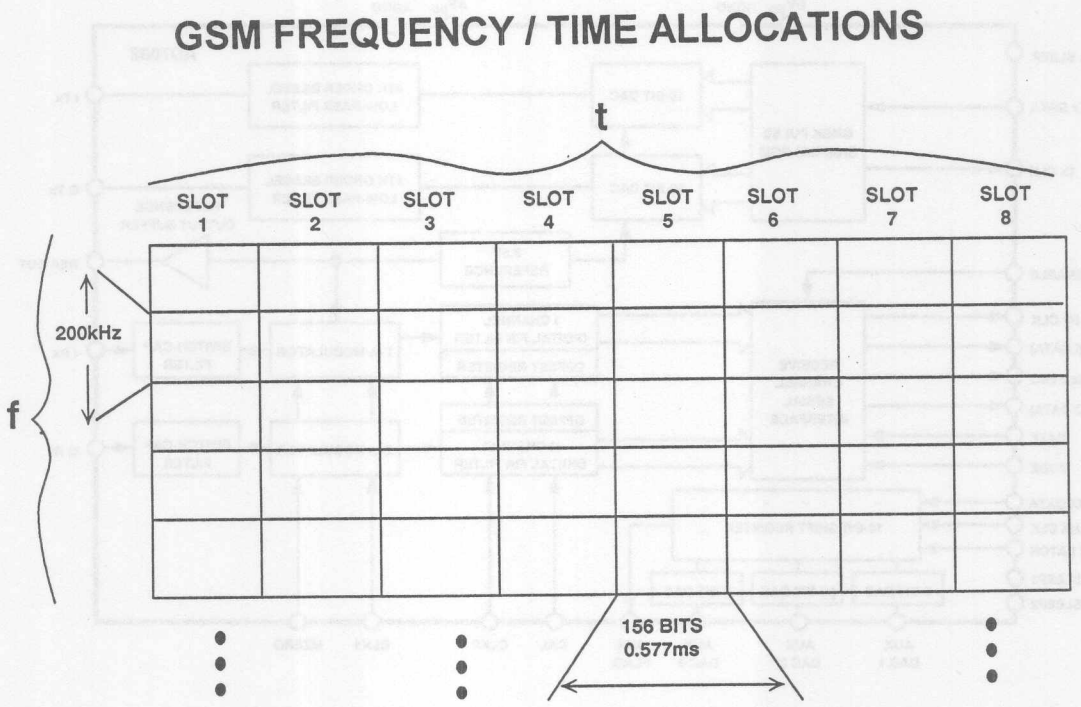


Figure 18.34

The received signal is filtered, amplified, and fed to an I/Q RF demodulator which recovers the I and Q signals. The baseband I and Q signals are converted by two 12-bit DACs at an effective sampling rate of 270kSPS. The I and Q signals are then demodulated by the GMSK digital demodulator. The 270kb/s burst is sent to the channel decoder and filters and then to the speech processor.

The AD7002 is a complete GSM Baseband I/O Port which performs the functions shown in Figure 18.35. The transmit path contains two 10-bit oversampled (16X) DACs followed by fourth-order anti-imaging filters. The DACs are driven by a digital modulator containing a GMSK-coded ROM. The receive path contains two high-performance 12 bit sigma-delta ADCs having a throughput rate of 270kSPS. The sigma-delta ADCs contain a 288-tap FIR filter having linear phase response and a 3dB point of 122kHz. Three auxiliary DACs are included for such functions as AFC, AGC and carrier shaping. The device dissipates approximately 100mW and has flexible power-down or sleep modes. A block diagram is shown in Figure 18.35 and key specifications are summarized in Figure 18.36.

AD7002 GSM BASEBAND I / O PORT

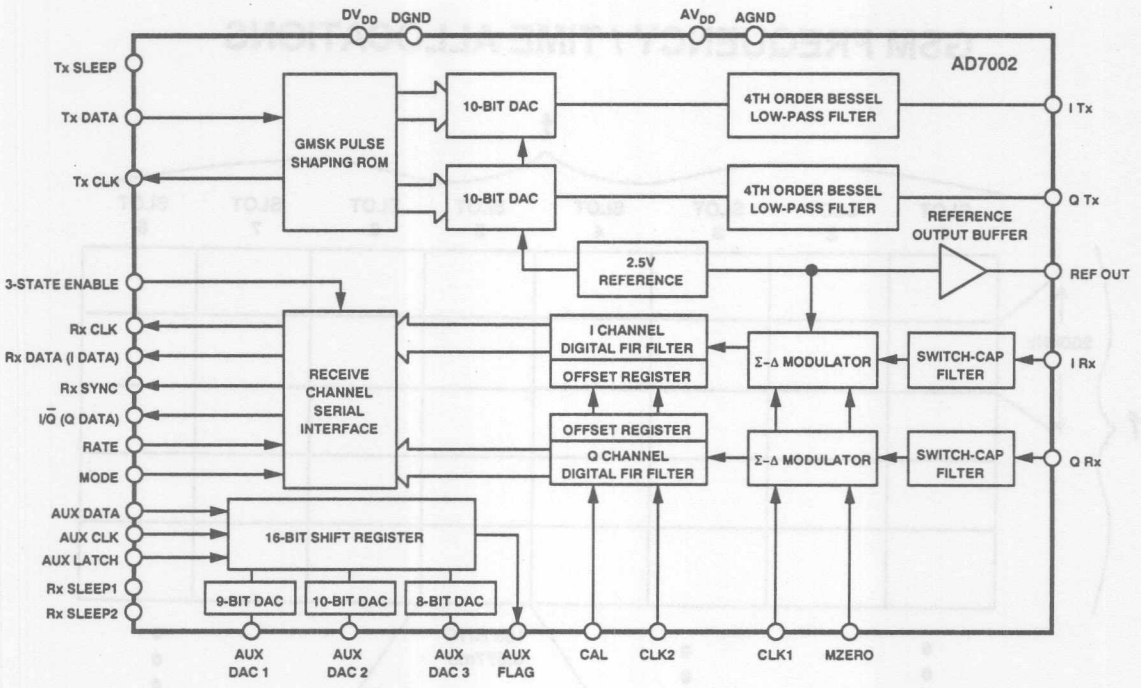


Figure 18.35

AD7002 GSM BASEBAND I/O PORT KEY SPECIFICATIONS

- **Transmit Path:** GMSK I/Q Digital Modulator
  Dual 10 Bit, 4.33MSPS Oversampled DACs
  Dual Anti-Imaging Filters
- **Receive Path:** Dual 12 Bit 270kSPS Sigma-Delta ADCs
  288-Tap 100kHz Linear Phase FIR Filter
- 3 Auxiliary DACs for AFC, AGC
- Low Power: 100mW
- Sleep Mode

Figure 18.36

In order to provide flexibility in system designs, Analog Devices supplies a family of ICs which can be used to perform various functions in the up- and down-conversion paths of a digital mobile radio system.

As described above, the AD7002 is a complete baseband digitization subsystem which performs the signal conversion between the DSP and the IF/RF sections in the GSM system.

The AD7001 is designed to perform the conversion of I and Q signals in the transmit and receive data paths of the GSM system. A block diagram is shown in Figure 18.37 and key specs in Figure 18.38.

AD7001 GSM BASEBAND I/O PORT BLOCK DIAGRAM

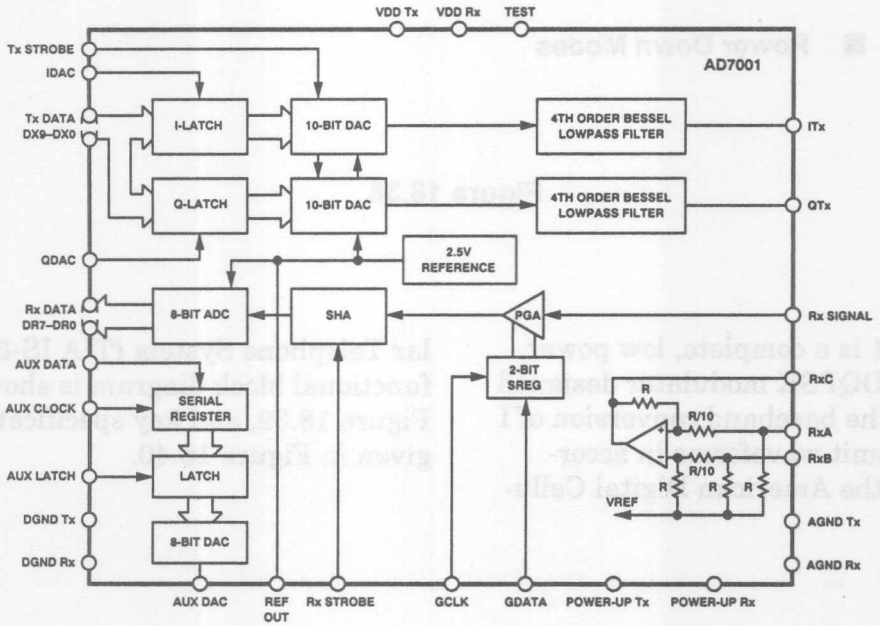


Figure 18.37

AD7001 GSM BASEBAND I/O PORT KEY SPECIFICATIONS

- **Transmit Path:** Dual 2.16MSPS 10-bit DACs with latches
  Dual Output Anti-Imaging Filters
- **Receive Path:** Single 8-bit 2.16MSPS ADC
  Receive Difference Amplifier
  Programmable Gain Amplifier
- Single Serial Auxiliary 8-bit DAC for AFC, AGC, etc.
- Power Down Modes

Figure 18.38

The AD7011 is a complete, low power, CMOS, π/4 DQPSK modulator designed to perform the baseband conversion of I and Q transmit waveforms in accordance with the American Digital Cellular Telephone System (TIA IS-54). A functional block diagram is shown in Figure 18.39, and key specifications are given in Figure 18.40.

AD7011 π/4 DQPSK BASEBAND TRANSMIT PORT FOR AMERICAN DIGITAL CELLULAR TELEPHONE (TIA IS-54)

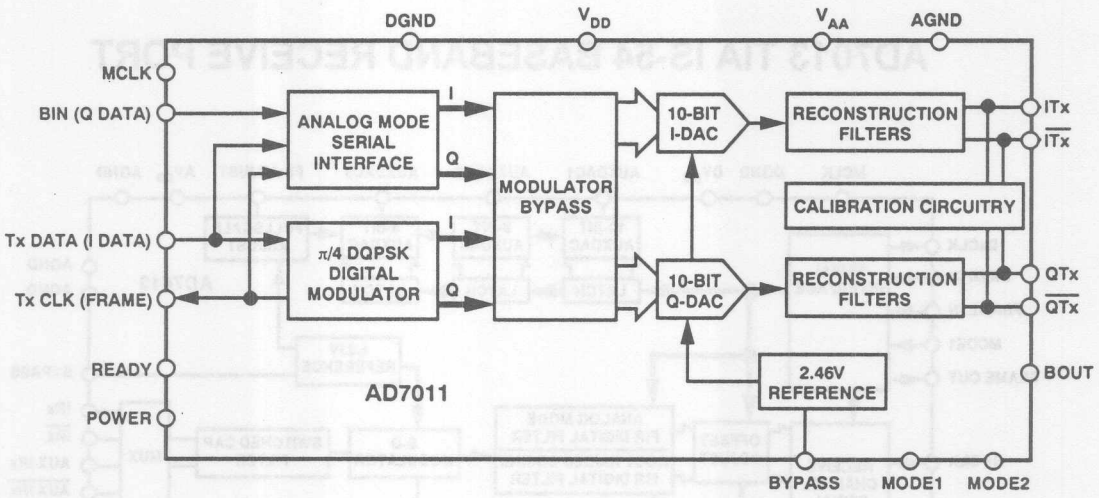


Figure 18.39

AD7011 π/4 DQPSK BASEBAND TRANSMIT PORT FOR AMERICAN DIGITAL CELLULAR TELEPHONE (TIA IS-54) KEY SPECIFICATIONS

- Single +5V Operation, Low Power
- On-Chip π/4 DQPSK Modulator
- Modulator Bypass Analog Mode
- Two 10-bit DACs
- On-Chip 4th Order Reconstruction Filters
- 30mW Typical Power Dissipation, 10μA in Power-Down Mode

Figure 18.40

The AD7013 is a companion part to the AD7011. The AD7013 is a TIA IS-54 baseband receive port. This device is designed to perform the baseband conversion of I and Q waveforms in the American Digital Cellular Telephone System. A functional block diagram of the AD7013 is shown in Figure 18.41, and key specifications are given in Figure 18.42.

AD7013 TIA IS-54 BASEBAND RECEIVE PORT

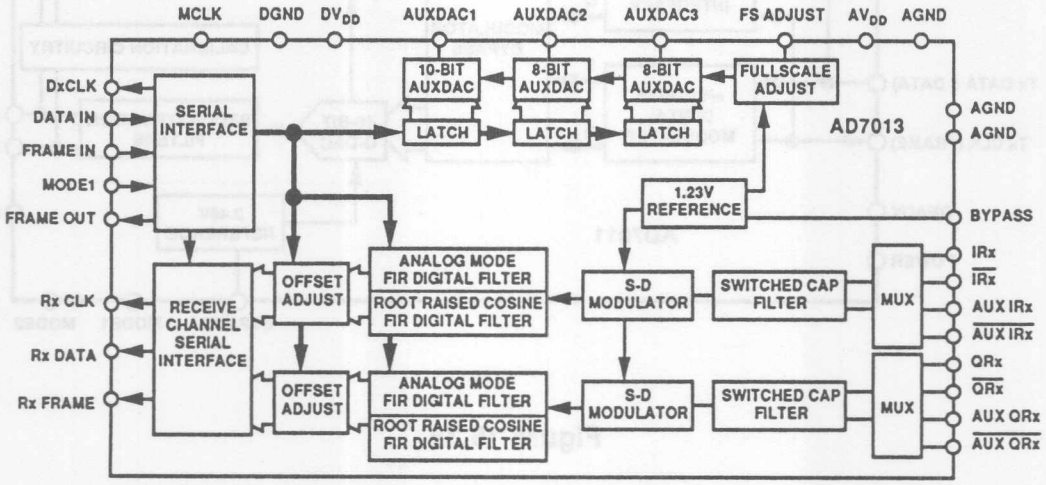


Figure 18.41

AD7013 TIA IS-54 BASEBAND RECEIVE PORT KEY SPECIFICATIONS

- Single +5V Supply Operation
- Differential or Single-Ended Analog Inputs
- Auxiliary Set of Analog I and Q Inputs
- Two Sigma-Delta ADCs
- Choice of Two Digital FIR Filters
- Three Auxiliary DACs
- Less Than 5μA in Power-Down Mode

Figure 18.42

The AD7010 is a complete CMOS π/4 DQPSK Baseband Transmit Port designed to operate in accordance with the Japanese digital cellular telephone system (JDC). A functional block diagram is shown in Figure 18.43, and key specifications are given in Figure 18.44.

AD7010 JAPANESE DIGITAL CELLULAR TELEPHONE (JDC) π/4 DQPSK BASEBAND TRANSMIT PORT

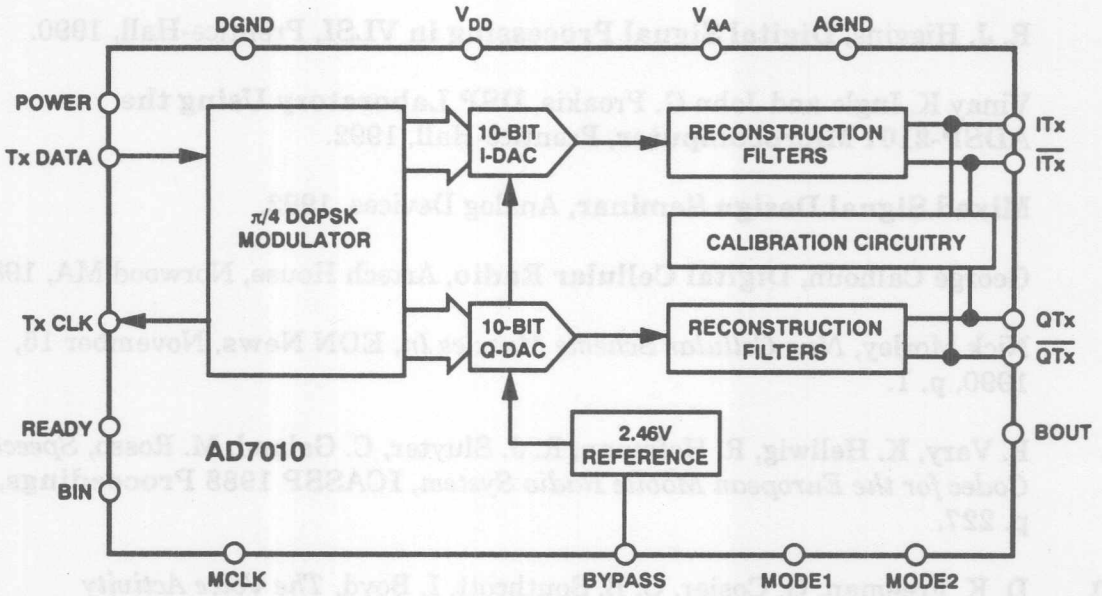


Figure 18.43

AD7010 (JDC) π/4 DQPSK BASEBAND TRANSMIT PORT KEY SPECIFICATIONS

- Single +5V Supply
- On-Chip π/4 DQPSK Modulator
- Two 10-Bit DACs (I and Q Channels)
- Two Reconstruction Filters
- Differential Analog Outputs
- Low Power: 30mW Typical, 5μA in Power-Down Mode

Figure 18.44

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SECTION 19

MOTOR CONTROL CIRCUITS

- BACKGROUND
- AC INDUCTION MOTORS
- VARIABLE VOLTAGE VARIABLE FREQUENCY CONTROL
- VECTOR CONTROL
- SLIP CONTROL
- HIGH PERFORMANCE DYNAMIC CONTROL
- GENERAL DESCRIPTION OF AD2S100/110 AC VECTOR PROCESSORS
- GAMANA - A PROJECT IN MOTION
- GAMANA VT
- GAMANA GMCDS
- CHIPSETS/ALGORITHMS
- APPLICATIONS

SECTION 19

MOTOR CONTROL CIRCUITS

Fred Flett, Matthew Finnie

Long known for its simplicity of construction, low-cost, high efficiency and long-term dependability, the ac induction motor has been limited by the inability to control its dynamic performance in all but the crudest fashion. This has severely restricted the application of ac induction motors where dynamic control of speed, torque and response to changing load is required. However, recent advances in digital signal processing (DSP) and mixed-signal integrated circuit technology are providing the ac induction motor with performance never before thought possible. Manufacturers anxious to harness the power and economy of Vector Control can reduce R&D costs and time to market for applications ranging from industrial drives to electric automobiles and locomotives with a standard chipset/development system .

It is unlikely that Nikola Tesla (1856-1943), the inventor of the induction motor, could have envisaged that this workhorse of industry could be rejuvenated into a new class of motor that is competitive in most industrial applications.

BACKGROUND

Before discussing the advantages of Vector Control it is necessary to have a basic understanding of the fundamental operation of the different types of electric motors in common use.

Until recently, motor applications requiring servo-control tasks such as tuned response to dynamic loads, constant torque and speed control over a wide range were almost exclusively the domain of dc brush and dc permanent magnet synchronous motors. The fundamental reason for this preference was the availability of well understood and proven control schemes. Although easily controlled, dc brush motors suffer from several disadvantages; brushes wear and must be replaced at regular intervals, commutators wear and can be permanently damaged by inadequate brush maintenance, brush/commutator assemblies are a source of particulate contaminants, and the arcing of mechanical commutation can be a serious fire hazard in some environments.

The availability of power inverters capable of controlling high-horsepower motors allowed practical implementation of alternate motor architectures such as the dc permanent magnet synchronous motor (PMSM) in servo control applications. Although eliminating many of the mechanical problems associated with dc brush motors these motors required more complex control schemes and suffered from several drawbacks of their own. Aside from being costly, dc PMSMs in larger, high-horsepower configurations suffer from high rotor moment-of inertia

as well as limited use in high speed applications due to mechanical constraints of rotor construction and the need to implement field weakening to exceed baseplate speed.

In the 1960's, advances in control theory, in particular the development of Indirect Field-Oriented Control, provided the theoretical basis for dynamic control of ac induction motors. Because of the intensive computation required by Indirect Field-Oriented Control, now commonly referred to as Vector Control, practical implementation was not possible for many years. Available hardware could not perform the high-speed precision sensing of rotor position and near real-time computation of dynamic flux vectors. The current availability of precision optical encoders, isolated gate bipolar transistors (IGBTs), high-speed resolver-to-digital converters and high-speed digital signal processors (DSPs) has pushed Vector Control to the forefront of motor development due to the advantages inherent in the ac induction motor. Until now, however, the lack of advanced development tools has limited development to in-house custom designs and restricted Vector Control to the privileged few with the resources necessary to design a DSP based system from the ground up.

POPULAR TYPES OF ELECTRIC MOTORS

- DC Brush
- DC Permanent Magnet
- AC Induction

Figure 19.1

LIMITATIONS OF DC MOTORS

- Power Rating is Limited at High Speeds due to Commutation
- Commutator and Brushes Require Maintenance
- Power-to-Weight Ratio is Much Less than for AC Induction Motor
- Arcing

Figure 19.2

AC INDUCTION MOTORS

With the definition of control algorithms and availability of hardware capable of implementing Vector Control the major problem in using ac induction motors in traditional dc PMSM applications is conceptual, i.e. understanding that the ac induction machine can operate almost identically to a dc machine. This requires understanding the fundamental mechanism underlying the generation and orientation of the rotor magnetic field (flux). In the dc PMSM, rotor flux is produced by permanent magnets and rotates in synchronism with the rotating stator field with a phase lag dependent on load. Figure 19.3 identifies this fixed relationship between the rotor magnets and flux in the dc machine. As load on the rotor increases, the rotor phase lag also increases until torque is at maximum when the stator flux is perpendicular or in time-quadrature (90°) to the rotor flux. Beyond this load the motor will stall.

The same relationship does not occur in the ac induction motor. Induction motor rotors are basically two rings with bars placed between them like a tread wheel for a mouse, hence the name squirrel-cage. Unlike the permanent magnet motor, rotor flux in an ac induction motor is produced by current induced in the bars of the squirrel-cage by the rotating stator field. Because of this there are two components that must be decoupled from the modulus of stator flux. The first is the flux component of current, usually referred to as

direct current (Ids) that must first be manufactured and maintained to create the rotating magnetic field in the air gap between the stator and squirrel cage rotor. The second flux component is the torque producing current induced on the squirrel cage rotor. This is usually referred to as quadrature current (Iqs).

Figure 19.3 depicts the rotating magnetic field that is produced by the circulating flux current in the stator and its interaction with the rotor conductors in the caged rotor which in turn creates the rotating magnetic field.

DC PERMANENT MAGNET MOTOR AND AC INDUCTION MOTOR

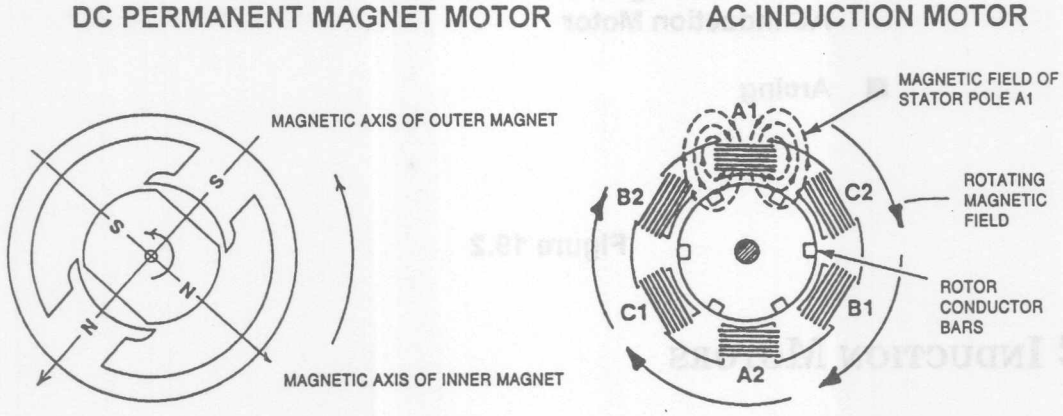


Figure 19.3

Unlike the case with synchronous motors, rotor flux in induction motors is not fixed relative to the rotor position. This is where the analysis of ac induction motors become complicated. As with any inductor, squirrel-cage rotors have a time constant dependent on temperature and saturation of the rotor material. Because of this 'rotor time constant', the rotor acts as a lowpass filter. The delay of the rotor time constant causes the rotor flux to lag behind (rotate slower) than the stator field. This difference in rotational speed is referred to as *slip*. Slip is measured as an angular velocity expressed as a frequency, typically around 3 Hz, and is important in understanding the limitations of the ac induction motor without Vector Control.

When a greater load is placed on the rotor, slip increases and the torque current component (rotor current) of the motor increases as the vector of the rotor flux relative to the stator field moves closer to 90° where maximum torque is produced. Like the PMSM, if the load on the motor is sufficient to force the rotor flux/stator field relationship beyond 90° the motor will stall.

WHY CONTROL IS IMPORTANT

- Velocity Control of Motor Reduces Losses
- More Efficient Use of Energy
- Lower Vibration and Noise
- Eliminates Need for Mechanical Gearing

Figure 19.4

WHAT IS ELECTRIC MOTOR CONTROL?

- Control of Rotational Velocity of the Motor
- Control of Torque (Load)
- Control of Position
- Interpolation and Coordination Between Motors

Figure 19.5

TYPES OF ELECTRIC MOTOR CONTROL

- Simple Control
- Adjustable Speed Drives - ASDs
- Servo Control
- Vector Control

Figure 19.6

VARIABLE VOLTAGE VARIABLE FREQUENCY CONTROL

Central to much of this discussion on motion control is the AD2S100 AC Vector Processor. This device has been developed as a central part of a vector control scheme. Before describing the use of the AD2S100 in vector control of an ac induction motor, the device can also be used to orient and control the phase of an induction motor for the simplest and commonest form of variable speed control called *variable voltage variable frequency control.*

As stated in the section on AC induction motors, the AC induction motor produces torque as a function of the slip, i.e the lag between the rotor frequency and the stator frequency. Inducing slip in the rotor is achieved by driving a load from the rotor. This forces the rotor to lag the stator: the greater the lag, the greater the torque. It is the constant action of the rotor trying to maintain synchronism with the stator which produces the torque.

The speed of the motor is controlled by the rotating frequency of the rotor. One 3 phase electrical cycle would equate to a single mechanical rotation in a single pole motor. For example, a 300Hz stator frequency produces 300 rps rotor velocity.

While varying the speed the voltage has to be controlled to be proportional to the frequency to prevent the motor from stalling. This need to maintain a constant voltage:frequency ratio leads to the name V/F Drive (this name has *no* connection with voltage-frequency converters).

The AD2S100 can be configured for use in V/F drives by simply controlling the update rate of the digital angle.

Figure 19.7 shows how the AD2S100 is used to manipulate the inverter's voltage and input frequency.

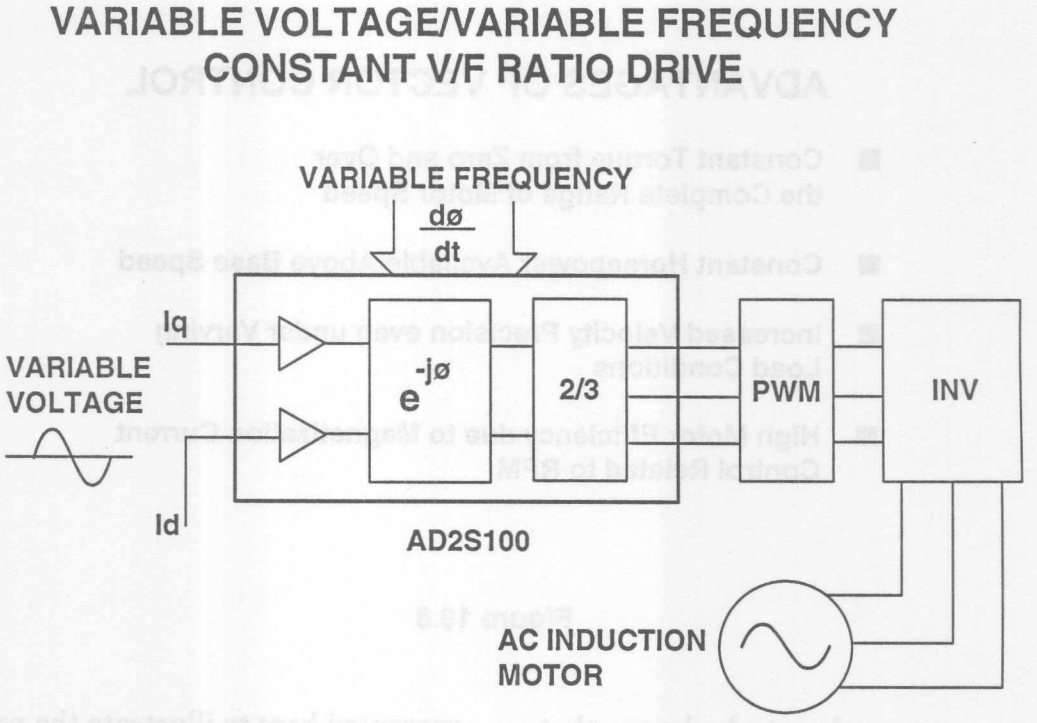


Figure 19.7

VECTOR CONTROL

For an ac induction motor to attain dynamic performance comparable to a dc brushless PMSM motor, the amplitude of the stator mmf vector, as well as its position with respect to the rotor flux vector must be controlled at all times. One of the prime tasks in Vector Control is to decouple the torque and flux based currents from the modulus of stator current and keep them in quadrature to one another at all times in a reference frame that is related to *rotor* coordinates. This requires sensing the three phase stator currents, transforming them into a coordinate frame that rotates in synchronism with the rotor flux and comparing them with set points for direct and quadrature axis components. The required current/voltage reference to be impressed upon the motor is then calculated, and finally a coordinate transformation from the rotating frame to the stationary or stator frame is carried out.

ADVANTAGES OF VECTOR CONTROL

- Constant Torque from Zero and Over the Complete Range of Motor Speed
- Constant Horsepower Available Above Base Speed
- Increased Velocity Precision even under Varying Load Conditions
- High Motor Efficiency due to Magnetization Current Control Related to RPM

Figure 19.8

There are several control schemes that can be implemented using Vector Control. Two common approaches are presented here to illustrate the power and versatility of the technique.

SLIP CONTROL

To illustrate the use of vector rotators, a current and slip control is presented in Figure 19.9. This control strategy offers very high efficiency with good torque control over a wide speed range. Torque control in this configuration is somewhat slow at low torque loads due to the time required for the rotor flux to build up as a function of the rotor time constant. This control scheme works well in applications such as refrigeration compressors, or fans for heating and ventilation, where efficiency is more critical than a fast response to changing loads.

CONSTANT SLIP FREQUENCY CONTROL USING THE AD2S100 VECTOR ROTATION COPROCESSOR

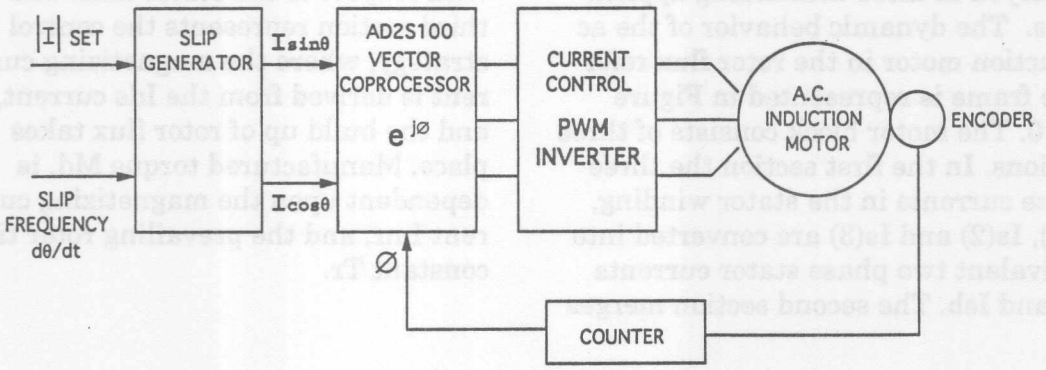


Figure 19.9

Optimal slip frequency depends on rotor resistance, which varies with temperature, and on the saturation characteristics of the motor. To achieve the ideal efficiency, rotor slip should increase with rotor resistance and saturation.

A slip generator calculates the Isinθ and Icosθ parameters from the set point current, |I| set, and the slip frequency demand. This computation can be carried out by the AD2S100 vector processor. The outputs are then vector rotated in the AD2S100 and three sine wave signals are generated for PWM use.

HIGH PERFORMANCE DYNAMIC CONTROL

In contrast to the simplicity of the scheme described above, there are many alternative approaches and more complex control architectures that are employed in more demanding applications. The dynamic behavior of the ac induction motor in the rotor flux reference frame is represented in Figure 19.10. The motor block consists of three sections. In the first section the three phase currents in the stator winding, Is(1), Is(2) and Is(3) are converted into equivalent two phase stator currents Isa and Isb. The second section merges these two phase currents with the rotor flux oriented operators, Ids and Iqs. In Figure 19.10, ρ (Rho), is used to identify the instantaneous position of rotor flux with respect to the stator axis. The third section represents the control strategy, where the magnetizing current is derived from the Ids current, and the build up of rotor flux takes place. Manufactured torque Md, is dependent upon the magnetizing current Imr, and the prevailing rotor time constant Tr.

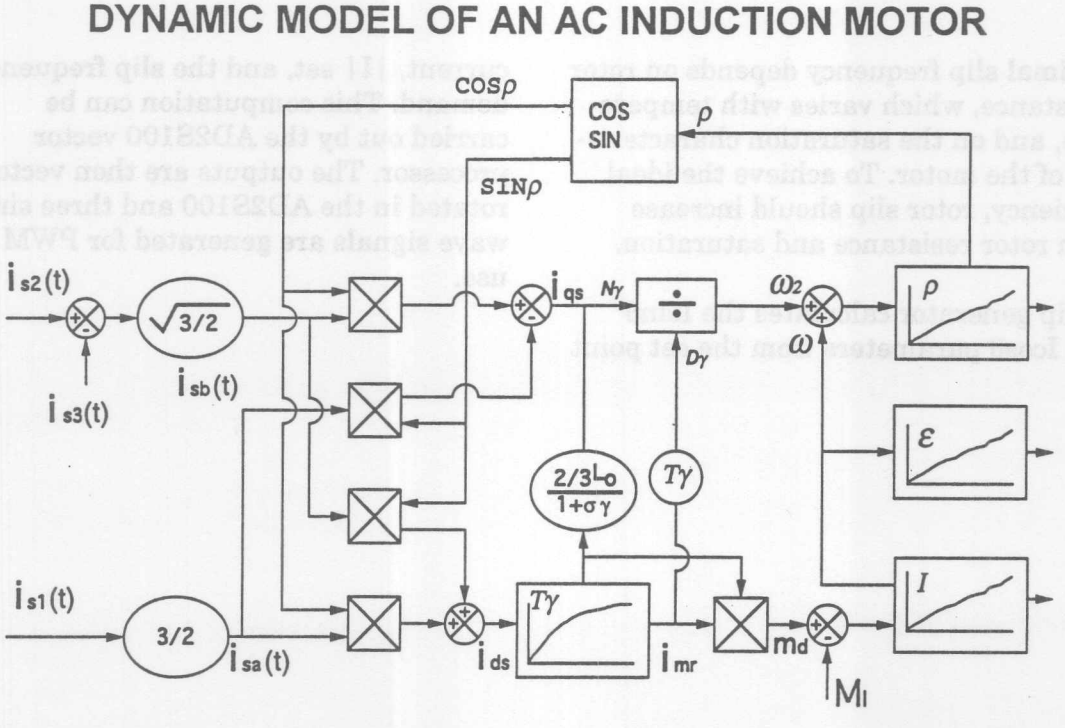


Figure 19.10

COMPLETE DYNAMIC CONTROL SYSTEM FOR AC INDUCTION MOTOR

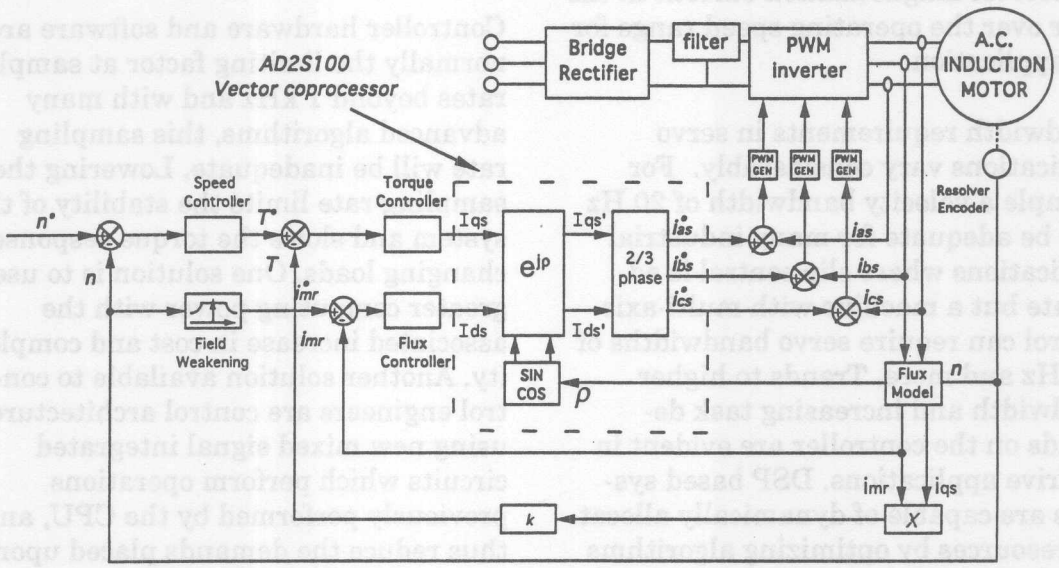


Figure 19.11

One of the major advantages of operating in the rotor reference frame is the ease of calculating magnitude and position of rotor flux and implementing a robust control scheme. In the rotor reference frame, the rotor behaves as a simple low pass filter for the magnetizing current. For example in the area of operation above base speed known as the *field weakening area*, the flux current must be reduced to attain the possibility of speeds above base speed. This creates a desaturated motor, and if a constant magnetization current is used the torque or voltage estimate may have a 100% error! By taking this nonlinearity into account the stability and robustness of control can be greatly improved.

Unlike the simple slip control, high-performance dynamic control in servo applications requires much greater signal processing power to provide fast loop response. The effect that limitations in processor capacity have on system performance is highly dependent on the specific loop involved. The servo-loop most sensitive to processor speed in a Vector Control system is usually the torque control loop. Most control architectures are implemented using nested control loops, commonly referred to as a cascade structure, with the actual controlling functions, in this case the torque and flux control loops, lowest in the hierarchy. In order to react to sudden changes in torque demand the torque loop must be fast enough to maintain the correct rotor flux vector at all times. Gain changes of more than 30% in the torque loop can severely restrict velocity and position performance. These limitations are avoided in the digital Vector Control system by designing the torque loop with sufficient bandwidth to allow precise control of both the torque

component of stator current and of the flux base current necessary to maintain the correct magnetization current in the rotor over the operating speed range for the application.

Bandwidth requirements in servo applications vary considerably. For example a velocity bandwidth of 20 Hz may be adequate for many industrial applications where slip control is adequate but a machine with multi-axis control can require servo bandwidths of 200 Hz and more. Trends to higher bandwidth and increasing task demands on the controller are evident in all drive applications. DSP based systems are capable of dynamically allocating resources by optimizing algorithms to reduce computational overhead in less important areas of performance to free processor time for more precise control of critical parameters.

Controller hardware and software are normally the limiting factor at sampling rates beyond 1 kHz and with many advanced algorithms, this sampling rate will be inadequate. Lowering the sampling rate limits the stability of the system and slows the torque response to changing loads. One solution is to use greater computing power with the associated increase in cost and complexity. Another solution available to control engineers are control architectures using new mixed signal integrated circuits which perform operations previously performed by the CPU, and thus reduce the demands placed upon it.

GENERAL DESCRIPTION OF AD2S100/110 AC VECTOR PROCESSORS

As previously stated, the ability of a system to decouple torque and flux components is critical to the implementation of vector control. The operation required to perform this is an in-line matrix calculation which transforms the 3 phase polar coordinates into the 2 phase rotor Cartesian ones. Practical implementation of the transformation can be performed using DSP or discrete analog solutions. The time taken to perform the task represents a phase lag in the system which effectively translates into a positioning error in the commutation of the motor. Minimizing the error is critical to the bandwidth and performance of the drive.

It is this mathematically intensive task that has hindered the commercial acceptance and use of vector control for ac induction motors.

The AD2S100 is a mixed signal hardware multiplier which performs the acquisition of the three phase currents and performs the coordinate transformation. This three-port device provides a digital input port that accommodates the most popular sensors used for rotor position and velocity measurement.

The AD2S100 has a parallel binary input which accepts a twelve bit digital word derived from a resolver via a

resolver-to-digital converter (RDC) such as the AD2S80A. The AD2S110 accepts incremental A quad B signals from an optical encoder.

A natural by-product of the type-two tracking loop conversion used in monolithic R/D converters is the availability of a velocity signal which can be used to replace a tachogenerator.

The AD2S100 has an analog input port which interfaces to three phase stator currents, normally sensed by hall effect devices. These real time signals may either be three phase 120 degree separated signals or quadrature sine and cosine signals.

These signals undergo coordinate transformation according to the vector equations previously discussed, and are then presented as analog output in either three phase, or, quadrature representation. A complete vector transformation is complete in two microseconds.

The partitioning of the input and output sections allows these blocks to be used for forward or reverse vector transformations. The vector transformations performed by the AD2S100/110 are shown in Figure 19.12.

AD2S100/110 VECTOR TRANSFORMATIONS



Stationary to Rotating Frame
Forward Rotation

Rotating to Stationary Frame
Reverse Rotation

Figure 19.12

Additional decode logic has been incorporated in the vector control chips to allow the user to select only two of three 120 degree phases at the input. This assumes that the sum of the three phases is zero, and that the third phase can be deduced from knowledge of the other two.

AD2S100 AC VECTOR PROCESSOR BLOCK DIAGRAM

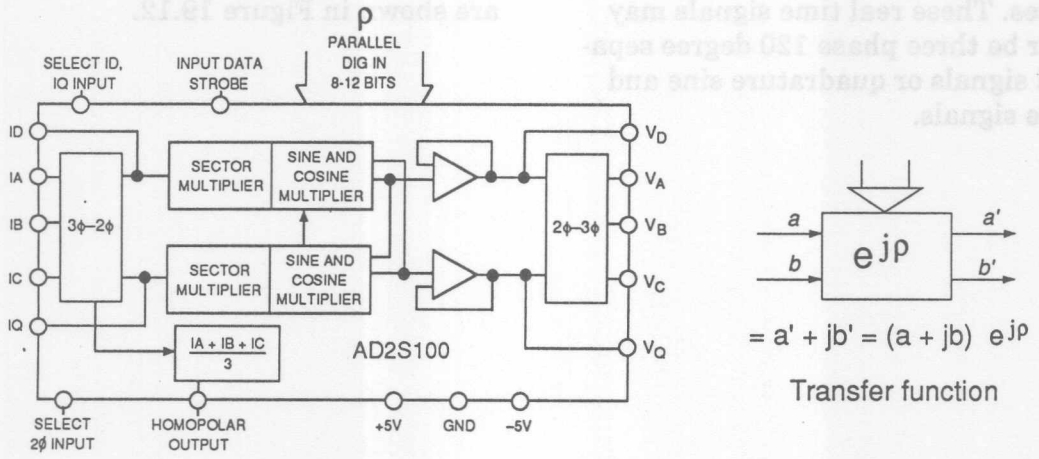


Figure 19.13

The AD2S100 has a homopolar output which senses if there is an imbalance between any of the three phase inputs, and therefore requires that all three inputs are used in a three phase system. Therefore the economy of using only two hall effect devices is made at the expense of the homopolar output. This output can be very useful in the detection and prediction of a dielectric breakdown resulting in an earth leakage condition.

The AD2S110 differs from the AD2S100 in ways which reflect the different functions required to process information from an optical incremental encoder rather than a resolver, when it is used as a rotor position sensor.

AD2S110 AC VECTOR PROCESSOR BLOCK DIAGRAM

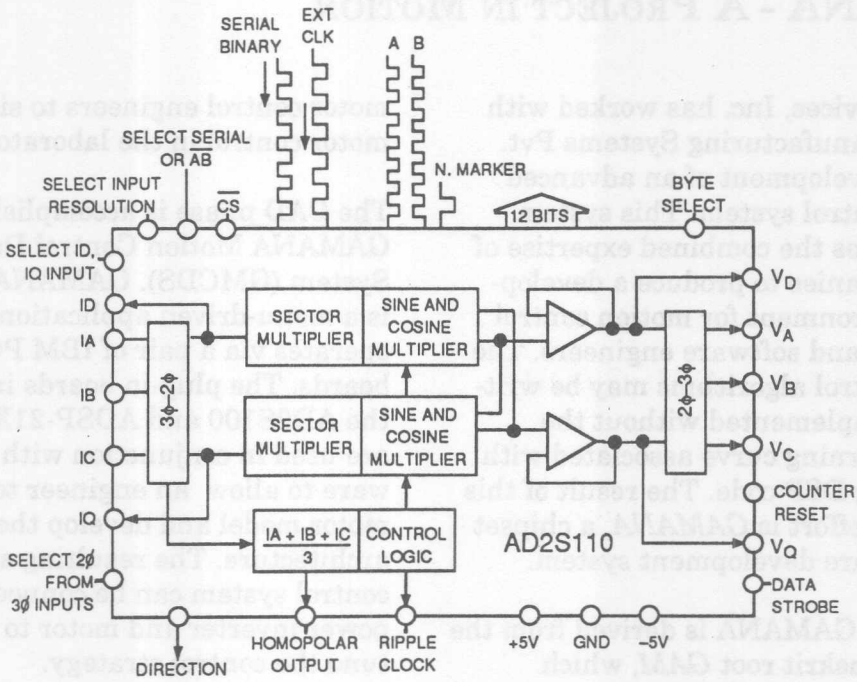


Figure 19.14

Inputs to the AD2S110 can have either absolute serial binary or incremental encoder format. The parallel digital port is an output in this case. The instantaneous incremental position input is converted to a parallel digital number which can be sent in that format to a peripheral device. Two other signals, direction sense, and a ripple clock which senses a once-per-revolution marker, are also available as output logic states.

GAMANA - A PROJECT IN MOTION

Analog Devices, Inc. has worked with Infosys Manufacturing Systems Pvt. Ltd. on development of an advanced motion control system. This system incorporates the combined expertise of both companies to produce a development environment for motion control hardware and software engineers. The vector control algorithms may be written and implemented without the typical learning curve associated with developing DSP code. The result of this combined effort is *GAMANA*, a chipset and software development system.

The name GAMANA is derived from the Indian Sanskrit root *GAM*, which means *go* or *move*. GAMANA is a revolutionary project that provides motion control engineers with a development system comparable in complexity to those which computer system designers have been using for many years. GAMANA reduces the complexity of implementing vector control for motors. This is done in three phases: Simulation/Training phase; CAD phase; and the Implementation phase.

The simulation and training phase uses GAMANA VT, a vector control tutorial program. GAMANA VT is a WINDOWS-based application that allows motor control engineers to simulate motor control in the laboratory.

The CAD phase is accomplished with GAMANA Motion Control Development System (GMCDS). GAMANA GMCDS is a menu-driven application that operates via a pair of IBM PC plug-in boards. The plug-in boards incorporate the AD2S100 and ADSP-21XX which are used in conjunction with the software to allow an engineer to create a motor model and develop the control architecture. The resulting simulated control system can be connected to a power inverter and motor to verify and tune the control strategy.

The implementation phase occurs once the control strategy is ready to be put into production. The software algorithms that were created with GAMANA GMCDS can be burnt into EPROM and run with the DSP device. The control algorithms for the system have been developed without the designer having to write any DSP code. The GAMANA code development process is illustrated in Figure 19.15. The corresponding hardware architecture for the advanced motion control engine is shown in Figure 19.16.

GAMANA MOTOR CONTROL CODE DEVELOPMENT PROCESS

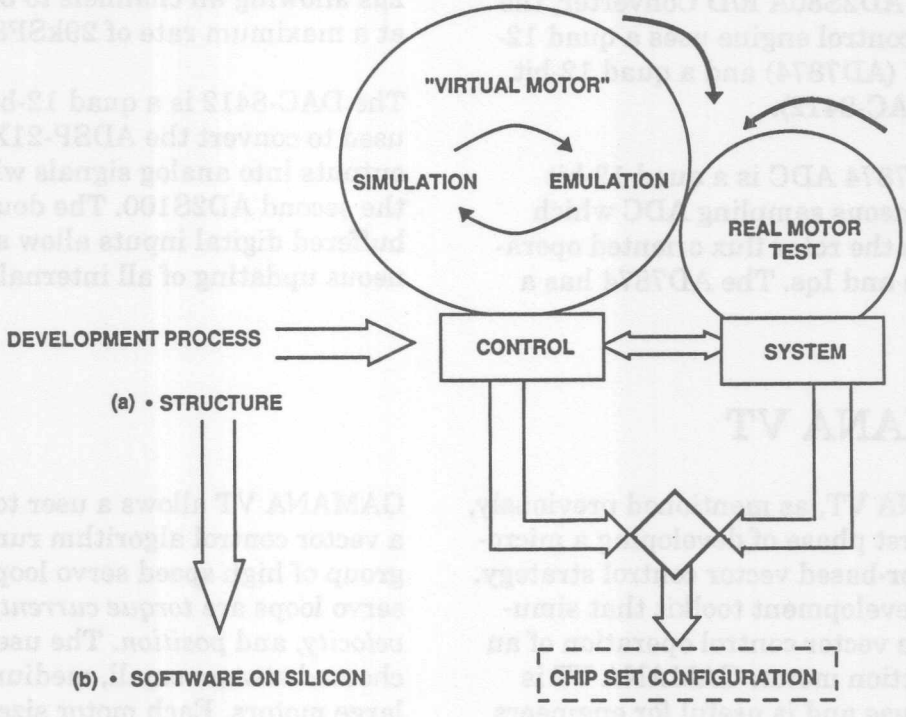


Figure 19.15

ADVANCED MOTION CONTROL ENGINE OF GMCDS HARDWARE

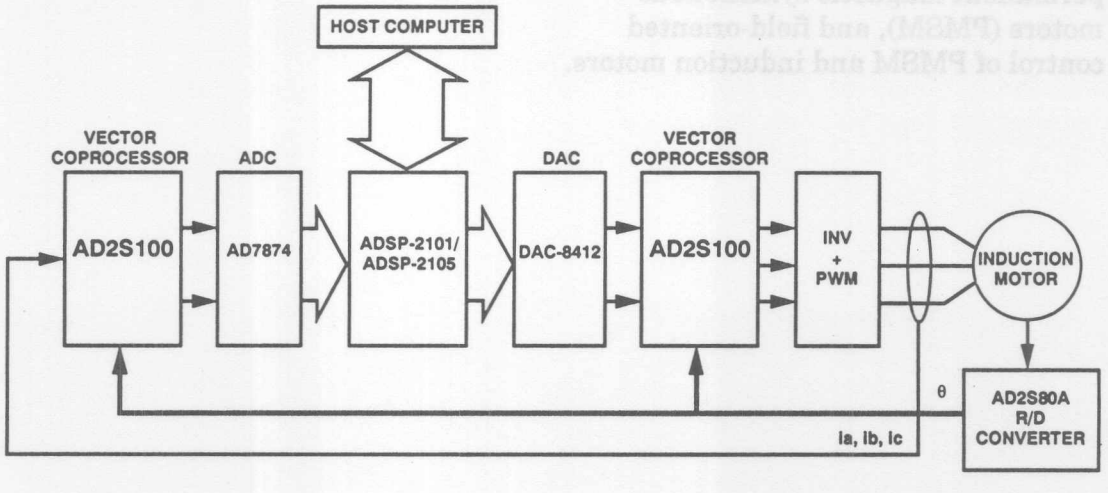


Figure 19.16

In addition to the AD2S100 Vector Coprocessors, the ADSP-21XX DSP, and the AD2S80A R/D Converter, the motion control engine uses a quad 12-bit ADC (AD7874) and a quad 12-bit DAC (DAC-8412).

The AD7874 ADC is a quad 12-bit simultaneous sampling ADC which digitizes the rotor flux oriented operators, Ids and Iqs. The AD7874 has a conversion time of 8μs per channel and a sample-and-hold acquisition time of 2μs allowing all channels to be sampled at a maximum rate of 29kSPS.

The DAC-8412 is a quad 12-bit DAC used to convert the ADSP-21XX digital outputs into analog signals which drive the second AD2S100. The double-buffered digital inputs allow simultaneous updating of all internal DACs.

GAMANA VT

GAMANA VT, as mentioned previously, is the first phase of developing a microprocessor-based vector control strategy. It is a development toolkit that simulates the vector control operation of an ac induction motor. GAMANA VT is easy to use and is useful for engineers whatever their background in vector control. Included with GAMANA VT is an extensive users manual that contains a detailed tutorial on vector control including detailed discussions of ac drives, synchronous machine operation, induction motors, pulse with modulation (PWM) inverter fed drives, permanent magnetic synchronous motors (PMSM), and field-oriented control of PMSM and induction motors.

GAMANA VT allows a user to simulate a vector control algorithm running as a group of high speed servo loops. The servo loops are *torque current, flux, velocity,* and *position*. The user can also choose between small, medium, and large motors. Each motor size has individual locked-rotor test parameters, which can be viewed and altered if necessary. The user can also access and change the gain, integral, and derivative parameters of each control loop. Figure 19.17 illustrates the software partitioning which is shown in greater detail in Figure 19.18.

GMCDS SOFTWARE PARTITIONING

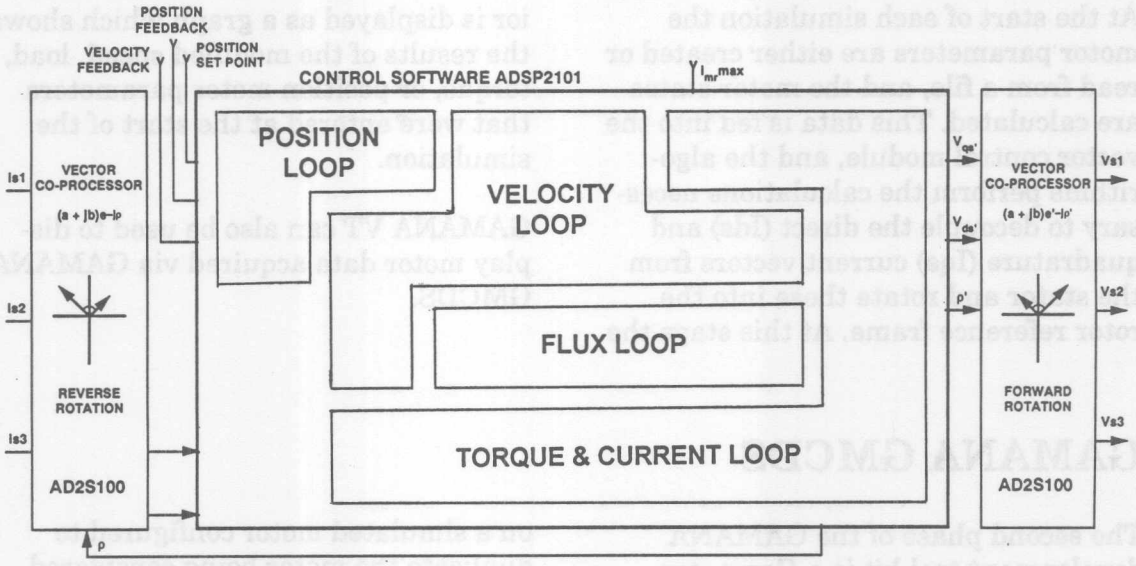


Figure 19.17

GAMANA ROTOR REFERENCE FRAME ARCHITECTURE

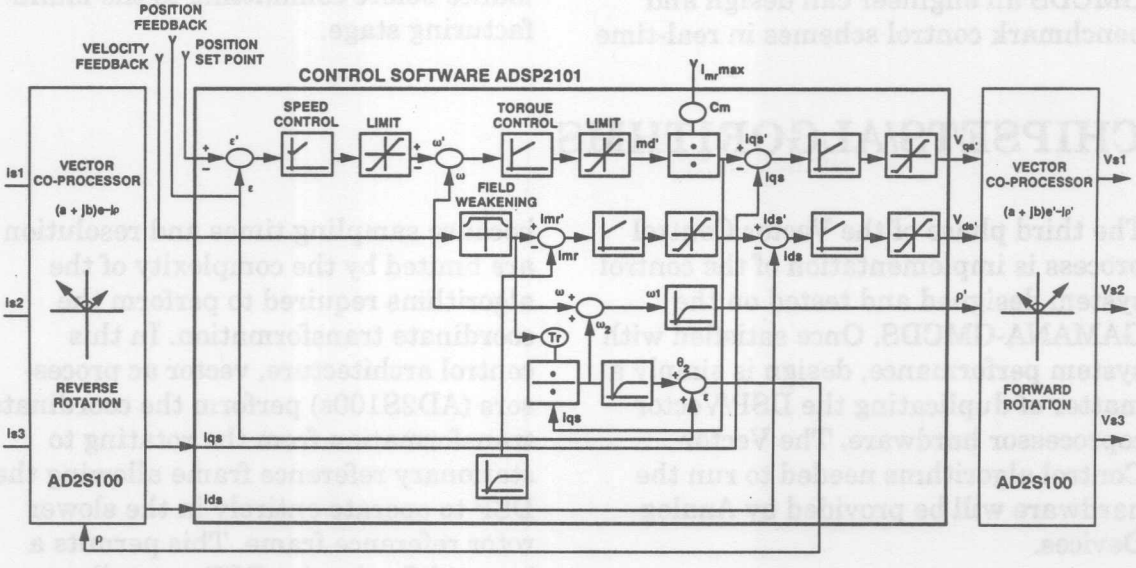


Figure 19.18

The vector control algorithm drives the ac induction motor software model and graphically displays the dynamic characteristics of the motor being controlled. At the start of each simulation the motor parameters are either created or read from a file, and the motor states are calculated. This data is fed into the vector control module, and the algorithms perform the calculations necessary to decouple the direct (Ids) and quadrature (Iqs) current vectors from the stator and rotate these into the rotor reference frame. At this stage the active control loops are invoked, and the modified current vectors are rotated back into the stator frame and fed to the motor model. The resultant behavior is displayed as a graph which shows the results of the modified speed, load, torque, or position motor parameters that were entered at the start of the simulation.

GAMANA VT can also be used to display motor data acquired via GAMANA GMCDS.

GAMANA GMCDS

The second phase of the GAMANA development tool kit is a Computer Aided Design CAD and development package for motion control. This consists of two plug-in boards for PC compatibles with a hardware architecture consisting of the Analog Devices ADSP-21XX series DSP and AD2S100 vector coprocessors as the computing core (see Figure 19.16). With GAMANA-GMCDS an engineer can design and benchmark control schemes in real-time on a simulated motor configured to duplicate the motor being considered. Once satisfied with the stability and performance of the control algorithms, the designer can connect an inverter and motor to verify the results of the simulation. Not only does this approach drastically shorten the design cycle, it allows the designer to verify the system software/hardware and motor performance before committing to the manufacturing stage.

CHIPSETS/ALGORITHMS

The third phase of the Vector Control process is implementation of the control system designed and tested on the GAMANA-GMCDS. Once satisfied with system performance, design is simply a matter of duplicating the DSP/Vector coprocessor hardware. The Vector Control algorithms needed to run the hardware will be provided by Analog Devices.

In purely DSP based Vector Control systems, performance limitations occur because sampling times and resolution are limited by the complexity of the algorithms required to perform the coordinate transformation. In this control architecture, vector ac processors (AD2S100s) perform the coordinate transformation from the rotating to stationary reference frame allowing the DSP to operate entirely in the slower rotor reference frame. This permits a low-end fixed-point DSP controller to work with torque current loop execution times under 75 microseconds. By

off-loading application specific operations to the AD2S100, the subsequent cost effective architecture provides the capability for expansion via new software algorithms or enhanced user interfaces.

The higher Pulse Width Modulation frequencies that can be accommodated by power devices such as IGBT's will mean even faster sampling times may be necessary to maintain control in a flux reference frame. The vector coprocessors are extremely fast computing the complete d-q transformation in under 3 microseconds. The sampling period is extended by approximately ×4 because all currents and fluxes are rotating at the slip frequency. Torque response does not have any limiting time constants under this type of control and therefore torque response is almost instantaneous.

APPLICATIONS

Vector Control promises to bring a new level of sophistication to industrial motor control as well as to consumer applications where precision motor control was previously thought to be too expensive or too difficult to implement.

Although added performance is a strong inducement, the energy savings that result from the increased efficiency afforded by Vector Control will most likely be the driving force behind replacement or modification in many current installations. The energy saved by converting to a flux Vector Control depends on the application but will be greatest in applications where induction motors are operated under less than full load conditions such as compressors and HVAC fans.

A 1989 U.S. Department of Commerce report on energy consumption states that electric motors use more than half of all electricity generated worldwide. The report continues that a 1% increase in efficiency for motors of 1 HP or greater in the U.S. would equal the output of a 1 M Watt generating plant. Considering that a typical industrial motor consumes 10 to 20 times its acquisition cost in electricity per year the payback for switching to Vector Control is obvious financially as well as ecologically.

Another area of research where there is great interest in Vector Control is electric vehicles (EVs). Because of their inherent dependability and low-cost, ac induction motors are ideal for EVs. However, the lack of inexpensive control hardware/software capable of operating under the wide range of conditions required has prevented their use. The availability of design tools and low-cost silicon will make Vector Controlled ac induction motors the preferred choice in future EV design.

ADVANTAGES OF VECTOR CONTROL FOR AC INDUCTION MOTORS

- Energy Savings -- Especially Compressors and HVAC Fans
- Enhanced Performance
- Ideal for Electric Vehicles
- Expands Use of AC Induction Motors in Industrial Drives

Figure 19.19

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